

I/O Design Flexibility with the FPGA Mezzanine Card (FMC)

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The FPGA's inherent flexibility has proven indispensable for the creation of external I/O interfaces. However, unless I/O is implemented on a daughter card (mezzanine module), replacing the physical I/O components and connectors requires changing the FPGA board design. To avoid these costs, designers have historically relied on the PCI[™] Mezzanine Card (PMC) and Switched Mezzanine Card (XMC) standards. The problem is that these were developed years ago for general purpose solutions such as single-board computers—not FPGAs.

The FPGA Mezzanine Card (FMC) standard, developed by a consortium of companies ranging from FPGA vendors to end users, specifically targets FPGAs, increasing I/O flexibility and lowering costs in a broad range of applications.

Introduction

Facing a seemingly endless stream of new and evolving I/O standards, it is not surprising that today's embedded system designers continue to rely on FPGAs to perform the increasingly critical role of external I/O interface for their systems. FPGAs offer a large number of configurable I/Os that support a virtually limitless variety of highly complex I/O standards, given the right IP. The designer can also use an FPGA to perform in-stream data processing, even on protocols running at multi-gigabit signaling speeds and bandwidths.

FPGAs are highly adaptable to changes in I/O requirements. After reconfiguring an FPGA to implement a new protocol, little more is required than replacing the physical I/O components and connectors. Unless the I/O was implemented on a mezzanine module, this means changing the board's design. To avoid the costs and effort associated with a design change, designers have historically relied on the PCI Mezzanine Card (PMC) and Switched Mezzanine Card (XMC) standards. However, these standards were developed years ago for general purpose solutions such as single-board computers (SBCs)—not FPGAs. That changed in July of 2008 with the ratification and release of the VITA 57 FPGA Mezzanine Card (FMC) standard by the American National Standards Institute (ANSI).

Developed by a consortium of companies ranging from FPGA vendors to end users, the FMC standard was created to provide a standard mezzanine card form factor, connectors, and modular interface to an FPGA located on a base board (carrier card). Decoupling the I/O interfaces from the FPGA in this manner simplifies I/O interface module design while maximizing carrier card reuse. Unlike the PMC and XMC standards that use complex interfaces like PCI, PCI-X™, PCIe®, or Serial RapidIO to interface to the carrier card, the FMC standard requires only the core I/O transceiver circuitry that connects directly to the FPGA on the carrier card.

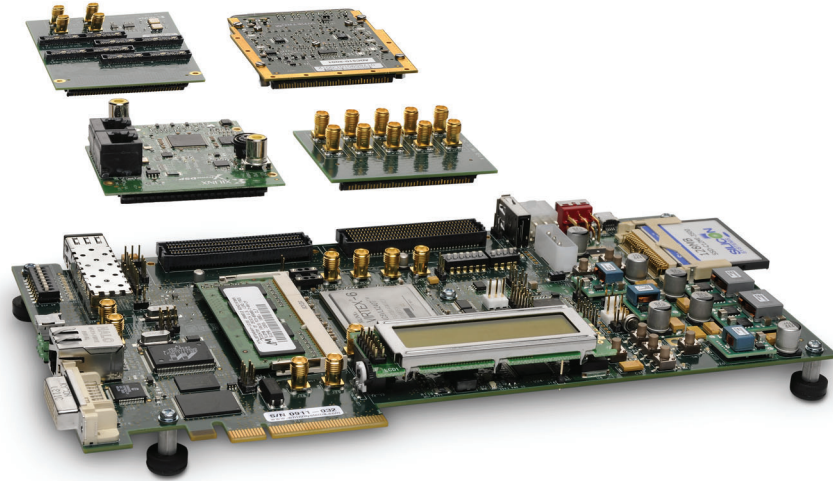
The resulting efficiencies translate to substantial benefits:

- **Data throughput:** Individual signaling speeds up to 10 Gb/s are supported, with a potential overall bandwidth of 40 Gb/s between mezzanine and carrier card.
- **Latency:** Elimination of protocol overhead removes latency and ensures deterministic data delivery.
- **Design simplicity:** Expertise in protocol standards such as PCI, PCI Express®, or Serial RapidIO are not required.
- **System overhead:** Simplifying the system design reduces power consumption, IP core costs, engineering time, and material costs.
- **Design reuse:** Whether using a custom in-house board design or a commercial off-the-shelf (COTS) mezzanine or carrier card, the FMC standard promotes the ability to retarget existing FPGA/carrier card designs to a new I/O. All that is required is swapping out the FMC module and slightly adjusting the FPGA design.

FMC Standard Highlights

The FMC standard defines both a single-width (69 mm x 76.5 mm) and double-width (139 mm x 76.5 mm) form factor. The single-width module supports a single connector to the carrier. The double-width module is designed for applications requiring additional bandwidth, more front panel space, or a larger PCB area, and supports up to two connectors. Having two form factors for the FMC standard

provides additional flexibility to optimize the board for space, I/O requirements, or both. [Figure 1](#) shows an FMC carrier card and multiple FMC mezzanine card options.



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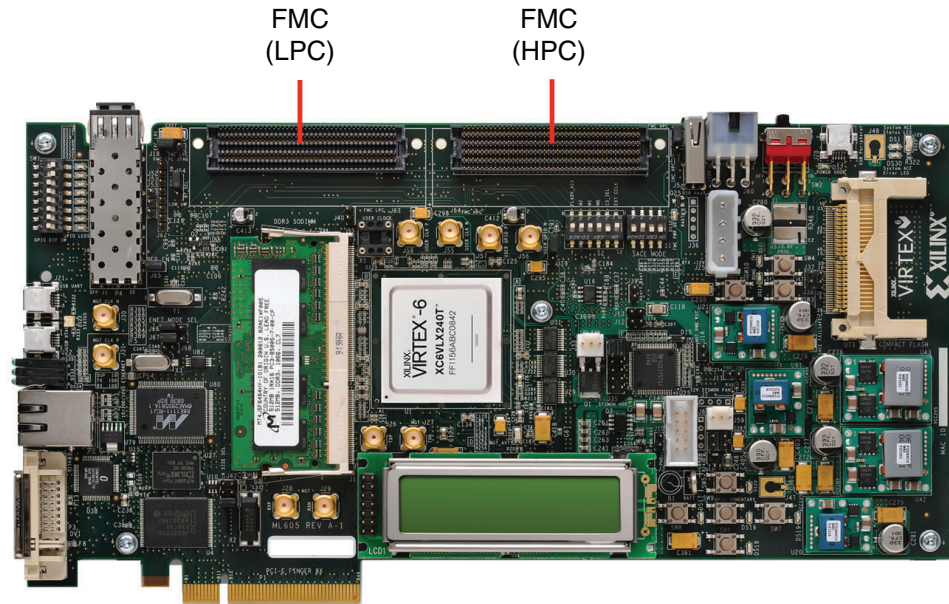
Figure 1: FMC Carrier Card and Multiple FMC Mezzanine Card Options

Once the form factor is selected, board designers can choose from two different connectors to use as an interface from the FMC standard to an FPGA on a carrier card: a Low Pin Count (LPC) connector with 160 pins and a High Pin Count (HPC) connector with 400 pins. Both support single-ended and differential signaling up to 2 Gb/s and signaling to an FPGA's serial connector at up to 10 Gb/s.

The LPC connector provides 68 user-defined, single-ended signals or 34 user-defined, differential pairs. It also provides one serial transceiver pair, the clocks, a JTAG interface, and an I2C interface as optional support for base Intelligent Platform Management Interface (IPMI) commands. The HPC connector provides 160 user-defined, single-ended signals (or 80 user-defined, differential pairs), 10 serial transceiver pairs, and additional clocks.

The HPC and LPC connectors use the same mechanical connector. The only difference is which signals are actually populated. Thus, cards with LPC connectors can be plugged into HPC sites, and if properly designed, HPC cards can offer a subset of functionality when plugged into an LPC site.

[Figure 2](#) shows an example board from Xilinx featuring a Virtex®-6 FPGA and both FMC connectors (one LPC and one HPC).



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Figure 2: ML605 Evaluation Board

The FMC standard supports a number of existing industry-standard carrier card form factors, including VME, CompactPCI, VXS, VPX, VPX-REDI, CompactPCI Express, AdvancedTCA, and AMC. The FMC standard also defines a range of environmental configurations, from low-cost commercial-grade form factors to "ruggedized" conduction-cooled options.

FMC Market Opportunities

Combining the versatility of the FMC standard and FPGAs creates an interesting spectrum of market and application opportunities. Typically, markets such as aerospace and defense, medical, industrial, telecommunications, video, and others rely heavily on FPGAs for their digital signal processing (DSP) price/performance benefits and for their ability to accommodate a broad assortment of I/O requirements. In the past, however, every market and every application within a given market required a different board design.

The emergence of the FMC standard has essentially modularized the board design effort into a processing engine (the carrier card) and an I/O engine (the FMC module). Designers can now reuse a single carrier card—comprising one or more FPGAs and an appropriate number and type of FMC connectors and boards—as the foundation for any number of markets and applications. Moreover, with new FPGAs offering enhanced performance and function, the designer can easily upgrade to a new carrier card while retaining full compatibility to the existing FMC modules.

A cursory examination of the range of form factor, I/O, and processing requirements for a few of the aforementioned markets illustrates the scope of the problem. Broadcast video applications, for example, generally need access to four or more SDI connectors, along with 10 Gigabit Ethernet and other transceiver connectors. In wireless base station applications, baseband processing typically involves ATCA/AMC form-factor boards processing at 3.125–10 Gb/s. This typically involves a combination of FPGAs

and traditional DSPs, with high-speed I/O (100–500 MHz, 12–16 bit resolution) on the radio front-end.

The aerospace and defense market prefers VME and cPCI form factors, but with widely varied processing requirements. For example, radar processing employs sampling rates similar to those used in wireless radio applications, but generally at higher resolutions. Military satellite base station applications typically involve higher sampling frequencies at lower bit resolutions (8–14 bits).

Clearly, with the range of processing and I/O requirements so widely varied for just this small subset of applications, one can imagine the extent of the problem across the entire range of applications served by FPGAs. Although the various processing requirements for these applications are fairly well understood—and served by a rich variety of hardware solutions from a mature board industry—engineers have historically spent precious design cycles creating custom hardware or dealing with complex (and frequently unnecessary) bus protocols.

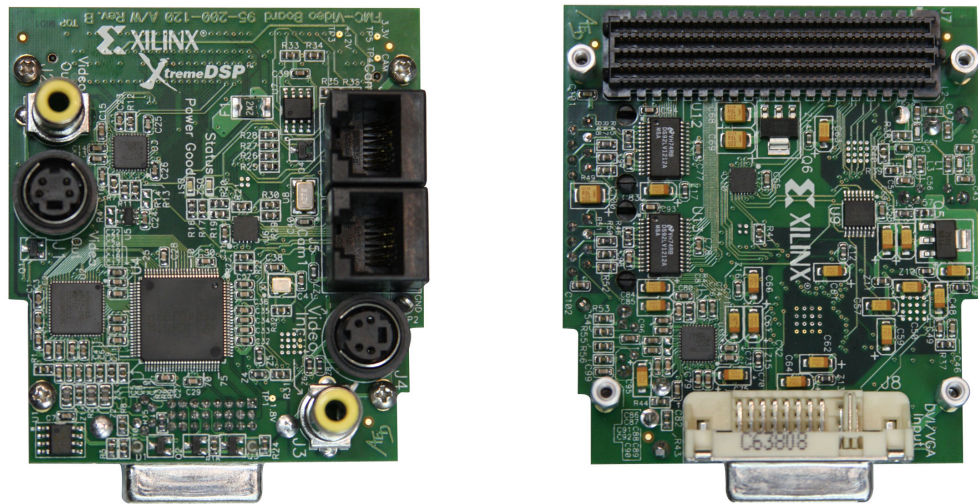
By decoupling FPGAs from the I/O engines, the FMC standard solves this problem. It enables designers to select the right processing engine in the right form factor and the right I/O engine from a plethora of COTS offerings that specifically support their end application. Additionally, the FMC standard makes it feasible for vendors to create a single system for evaluation and development that they can also deploy in production, thereby significantly reducing cost and time to market.

FMC Modules and the Xilinx Targeted Design Platform

Xilinx is committed to providing its customers simpler, smarter, and more strategically viable design solutions for a wide variety of industries—what Xilinx calls *Targeted Design Platforms*. Targeted Design Platforms provide the optimum in flexibility, accessibility, applicability, and time to market, enabling customers to spend less time developing application infrastructure and more time creating their unique value in the design.

A key enabler of the Targeted Design Platform is a unified board strategy that produces a standardized and coordinated set of carrier cards available both from Xilinx and ecosystem partners—a non-trivial feat made possible in large part by adoption of the FMC standard. Beginning with the release of the Virtex-6 and Spartan®-6 families, all future carrier cards, development kits, and market-specific solutions incorporate the FMC standard. This enables the creation of a unified, scalable, and extensible delivery mechanism for all Targeted Design Platforms.

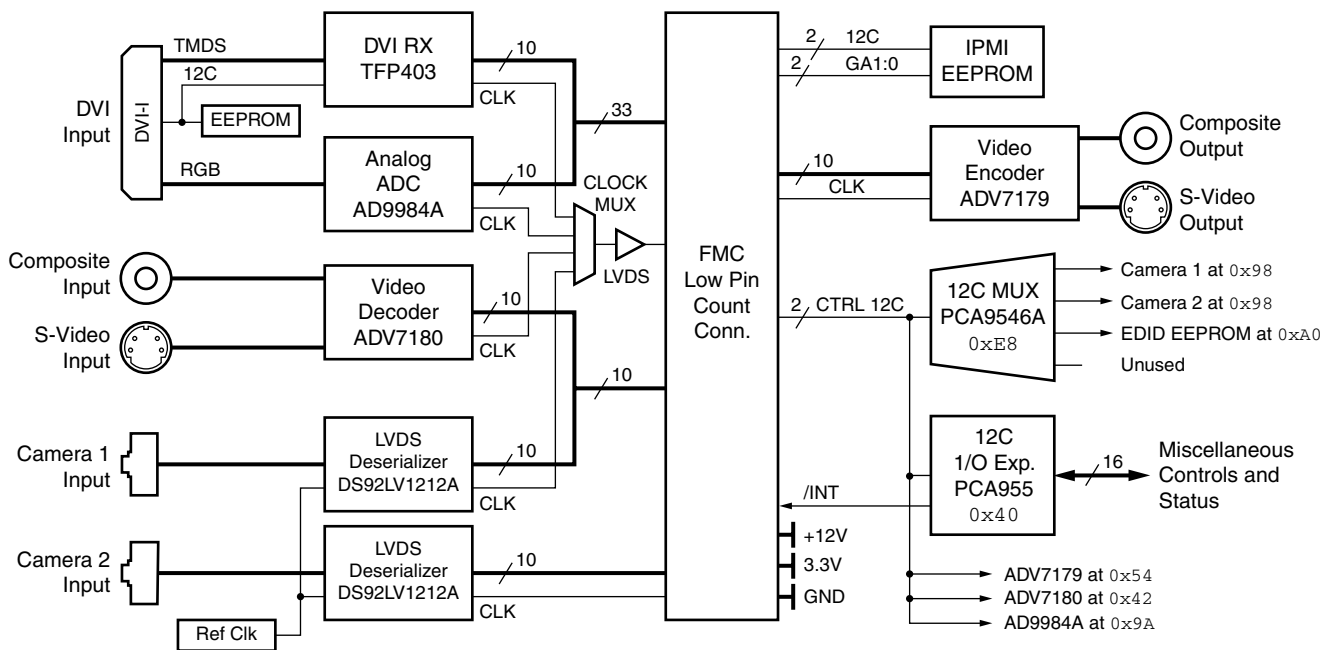
Xilinx has successfully verified a subset of the Targeted Design Platform concept with the introduction of the Spartan-3A DSP FPGA and the Video Starter Kit. The Spartan-3A DSP FPGA Video Starter Kit includes a Spartan-3A DSP 3400A FPGA and base IP. To this, Xilinx has added functionality important to the video surveillance and analytics markets by providing an FMC-Video I/O mezzanine card ([Figure 3](#)), a CMOS camera module, video-specific reference designs, and a comprehensive set of Xilinx® development tools.



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Figure 3: FMC-Video Mezzanine Board (Front and Back)

Figure 4 shows a high-level block diagram of the FMC-Video mezzanine board.



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Figure 4: FMC-Video Mezzanine Board Block Diagram

The FMC-Video mezzanine board includes several video interfaces. A DVI connector supports both analog and digital video data. SDTV input is supported through S-Video and composite inputs. Two 8P8C modular connectors provide the interface to two cameras. Typically, Xilinx customers use the other (LPC) FMC connector on the carrier card for a second mezzanine card that adds custom video interfaces like their own sensor cameras.

Summary

The FMC standard represents a major change in development options available to FPGA developers. Designers working with microprocessors and traditional DSPs have enjoyed the flexibility of scalable development solutions for decades. The FMC standard brings the power of modular design to developers in the FPGA domain.

COTS board vendors can accelerate and simplify product design by reusing hardware designs, significantly reducing product overhead. These efficiencies translate into better product offerings for more applications, allowing customers to focus on their unique differentiation and accelerate deployment of their solutions to market.

To learn more about the FMC standard, ecosystem offerings, and roadmaps, see the VITA website:

<http://www.vita.com/fmc.html>.

To learn more about FMC plans and products from Xilinx, see the Xilinx website:

<http://www.xilinx.com/fmc>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
08/19/09	1.0	Initial Xilinx release.

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