Integrating compute acceleration into embedded system design using Vitis

Date & Time: October 8, 2021 (9:30 AM – 1:00 PM EDT)

Important Notes:

- You must register separately for this tutorial through https://www.xilinx.com/support/university/workshops/schedule.html. A confirmation email will be sent upon receiving your registration. Please register ONLY if you are sure to attend the tutorial since the number of seats are limited due to hardware board resources.
- This tutorial will involve the use of online hardware resources located on ECELabs site. The design compilation will occur on AWS instances and hence require good and stable network connection. You will use Remote Desktop (RDP) and Chrome browser. Further instructions will be sent couple of days before the tutorial. The AWS instances will have all necessary tools installed to run the labs.
- It will be hard to catch on with the tutorial in the middle. So, it is highly recommended that you join from the start. Joining in the middle is discouraged or prohibited.

Instructor: Parimal Patel (Xilinx University Program)

Abstract

Xilinx is the inventor of the FPGA, programmable SoCs, and now, the ACAP. Our highly flexible programmable silicon, enabled by a suite of advanced software and tools, drives rapid innovation across a wide span of industries and technologies - from consumer to cars to the cloud.

The goal of this tutorial is to introduce the Xilinx Vitis software development environment for designing accelerators for embedded systems using Vitis. Vitis supports C/C++ and OpenCL.

Attendees will have the opportunity to learn how to use these tools, test the tutorial examples on the target boards, and understand how to build their own custom embedded systems.

Topics to be covered:

- Xilinx Vitis development framework and design flows
- Vitis HLS project creation flow, profiling and design analysis
- Integrating Vitis HLS developed IP using Vivado IPI
- Exporting generated hardware to Vitis embedded software development flow (including Linux and Python)
- Introduction to a compossible pipeline architecture

Target audience

Embedded hardware and software developers. This is an introductory tutorial, but it is expected that attendees have some programming experience and basic understanding of computer architecture.

Xilinx will provide remote access to cloud instances which will be enabled with Xilinx tools. Attendees will also be provided hardware board access either remotely or locally. Attendees must have their own laptop with reasonable screen size to effectively try the tutorials. (Tablet, and Netbook type devices may not be suitable).