SDSoC Development Environment Release Notes

UG1185 (v2015.2.1) September 30, 2015

Feature Summary

For licensing and installation information, refer to the document *SDSoC Environment User Guide: Getting Started*, (UG1028). For a hands-on introduction to the SDSoC™ environment refer to the Tutorial Labs in the document *SDSoC Environment User Guide: Getting Started,* (UG1028), (prebuilt labs are found in the `<sdsoc_install_root>/docs/labs directory`). For additional reference and tutorial information, refer to *SDSoC Environment User Guide*, (UG1027). All user guides can be found on the web http://www.xilinx.com/products/design-tools/software-zone/sdsoc.html#docstraining.

Release Summary

- Integrated installer including SDSoC 2015.2.1 and the Vivado Design Suite 2015.2 (System Edition with Vivado® HLS) for Zynq® family devices
  - Complete installation environment containing tools, data files, and patches for supported targets
  - Web-based installer option
- Windows 64-bit support
  - Windows 7, 7 SP1 (64-bit), English
- Linux 64-bit host support
  - Red Hat Enterprise Workstation 6.4-6.6 and 7.0 (64-bit)
  - Ubuntu Linux 14.04 LTS (64-bit) - separate xsltproc install no longer required
- Target OS support
  - Linux (kernel 3.19, Xilinx branch Xilinx-v2015.2.02), bare-metal and FreeRTOS 8.2.1
  - Example PetaLinux BSP for ZC702 platform with documentation in *SDSoC Environment User Guide: Platforms and Libraries* (UG1146)
- Updated documentation, including tutorial labs and a platform and libraries methodology guide
  - *SDSoC Environment User Guide*, (UG1027)
  - *SDSoC Environment User Guide: Getting Started,* (UG1028), Tutorial Labs 1-5 - Includes updated content for AXI Performance Monitor usages.
  - *SDSoC Environment User Guide: Platforms and Libraries,* (UG1146) - Updated sample platform tutorials.

- SDSoC Eclipse UI with project creation, implementation and debug
  - Debugger updated to connect to target using xsdb
  - Usability updates, for example the build flags unsaved files in the source editor
  - Critical warnings when timing is not highlighted and includes additional information
  - Highlighted error messages
  - Online SDSoC help
- Flow enhancements
  - Additional error checking for Vivado HLS functions with arguments using `#pragma HLS PARTITION`
  - Incremental builds supported in performance estimation flows
  - Vivado implementation step uses `opt_design -directive` Default
- Platform updates
  - OSD platform included with full release support
- Enhanced platform deployment support
  - New tutorial for simple LED platform for standalone BSP
  - Updated step by step tutorials for platform creation updated in UG1146
  - Improved error checking for hardware platform XML files
  - Support to specify content to add to SD card images generated for users
  - Support for standalone BSP configuration file (MSS) and standalone BSP software repository
- New and updated sample applications
- Bug fixes and infrastructure updates
  - Improved stability and ease of use, including improved error checking
  - Source code with multi-line macros supported on Windows
  - For standard platforms Linux boot enables clocks used by ILA IP cores used for hardware debugging
  - Enhanced error messaging when hardware function latency cannot be determined or is not specified
  - Assign AXIMM ports with the same bus name to the same system port
  - Stub file issue corrected for INOUT argument passed by reference
  - Updated platform qualification checklist
- Advanced User features
  - New `-impl-tcl` command-line option for sdscc/sds++ `-impl-tcl` to override default Vivado synthesis and implementation commands

Additional Licensing Requirements and constraints

The SDSoC `samples/platforms/zc702_hdmi` platform requires licenses for the following Xilinx IP cores, available as part of the SDSoC license.

- LogiCORE, Chroma Resampler
- LogiCORE, Video Timing Controller
- LogiCORE, Test Pattern Generator
- LogiCORE, YCrCb to RGB Color-Space Converter

This video platform includes evaluation licenses for IP from Xilinx partners. You must obtain a full license to use any of these IP in a product. For more information refer to *Zynq-7000 All Programmable SoC: ZC702 Evaluation Kit and Video Imaging Kit (v5.0)* (UG926).

Known Issues

See Answer Record 65472.

Revision History

The following table shows the revision history for this document:

Date	Version	Revisions
09/30/2015	2015.2.1	Updated entire text for current release.
07/26/2015	2015.2	Fixed minor formatting error. No content changes.
07/20/2015	2015.2	Initial Xilinx release.

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