I/O Pin Planning Tutorial

PlanAhead Design Tool

UG674 (v 14.1) May 8, 2012

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I/O Pin Planning Tutorial

This tutorial introduces the Xilinx® PlanAhead™ software capabilities and benefits when performing I/O pin assignment for FPGA devices. It describes the procedure for creating and assigning I/O ports to physical package pins. The I/O Planning view environment enables you to create, import, and configure the initial list of I/O ports. You can group the related ports into Interfaces and then assign them to package pins.

The objective of this tutorial is to familiarize you with the I/O pin planning process using the I/O Planning functionality in the PlanAhead tool. There are two parts to this tutorial that can be performed independently. The first part briefly describes I/O planning capabilities prior to having a synthesized netlist or RTL Sources with I/O ports defined. The second part describes I/O planning functionality after synthesis. Most of the PlanAhead I/O planning features are described in Part2. However, many of them are available at prior to running synthesis as well.

The capabilities include semi-automated interactive modes to allow controlled I/O port assignment. Fully automatic pin placement is also available for some device architectures. The I/O Planning view environment shows the relationship of the physical package pins and banks with their corresponding I/O die pads. Intelligent decisions can be made to optimize the connectivity between the PCB and the FGPA device.

You can perform I/O pin assignment at various stages of the design cycle. You can perform I/O exploration and assignment with an I/O Planning project even before the design source files are available. You can import a Comma Separated Value (CSV) format file for I/O planning, or export it for use in PCB schematic symbol or Hardware Description Language (HDL) header generation.

The PlanAhead tool also enables you to I/O pin plan in the elaborated Register Transfer Level (RTL) design or in the synthesized netlist design. The PlanAhead tool performs more comprehensive I/O and clocking DRCs when using a netlist design.

Not all commands or command options are covered in this tutorial. This tutorial uses the features contained in the PlanAhead tool, which is bundled as a part of ISE® Design Suite version 14.1.

Software Requirements

The PlanAhead tool is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead tool is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite: Installation and Licensing Guide (UG798)* at http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/iil.pdf.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller xc7k70t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Tutorial Design Description

The small sample design used in this tutorial includes:

- A RISC processor CPU core
- A pseudo FFT
- Four gigabit transceivers (GTs)
- Two USB interfaces

The design targets an xc7k70t device. A small design is used to:

- Allow the tutorial to be run with minimal hardware requirements
- Enable timely completion of the tutorials
- Minimize data size

Locating Tutorial Design Files

Copy the files from the ISE software installation area:

<*ISE_install_area*>/ISE_DS/PlanAhead/testcases/PlanAhead_Tutorial.zip

Extract the zip file contents into any write-accessible location.

The unzipped `PlanAhead_Tutorial` data directory is referred to in this tutorial as the `<Extract_Dir>`.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data is required each time you run the tutorial.

Part 1: Using I/O Pin Planning Projects (pre-synthesis)

The PlanAhead tool provides an I/O Pin Planning view layout that displays views more applicable to placing I/O Ports and clock logic. You can open the I/O planning layout without a design to analyze device resources.

These first few I/O Pin Planning steps involve pre-synthesis techniques to begin I/O Planning early prior to a synthesized netlist. Most of the features are also available for an Elaborated RTL, Synthesized or Implemented Design. I/O Pin Planning can be performed at any stage of the design process. Post-synthesis I/O Planning enables a much more robust set of DRCs and clock placement capabilities.

Step 1: Creating a New Project and Exploring the Views

1. Open the PlanAhead tool and create the project_pinout I/O Pin Planning project.
2. On Windows, double-click the **Xilinx PlanAhead 14.1** Desktop icon, or select: **Start > All Programs > Xilinx Design Tools > ISE Design Suite 14.1 > PlanAhead > PlanAhead**.
3. On Linux, go to `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data` directory and type **planAhead**.
4. In the Getting Started page, select **Create New Project**.
5. Click **Next** to confirm the project creation and to display the Project Name dialog box.

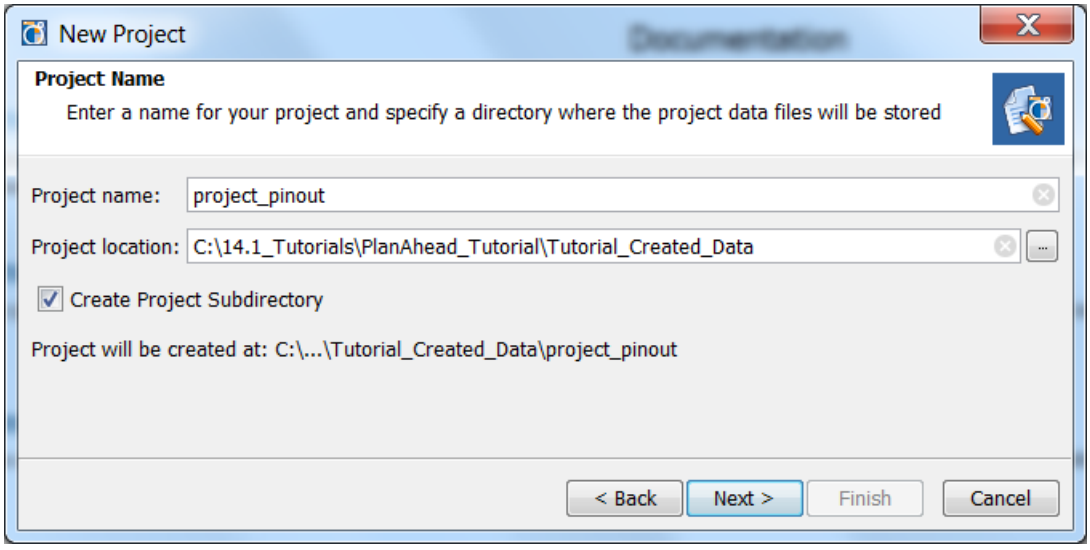

Figure 1: New Project Name and Location Dialog Box

6. Type the Project name, **project_pinout**.
7. Enter the Project location:

   <*Extract_Dir*>/PlanAhead_Tutorial/Tutorial_Created_Data.
8. Click **Next** to open the Design Source dialog box.
9. Select **I/O Planning Project**.

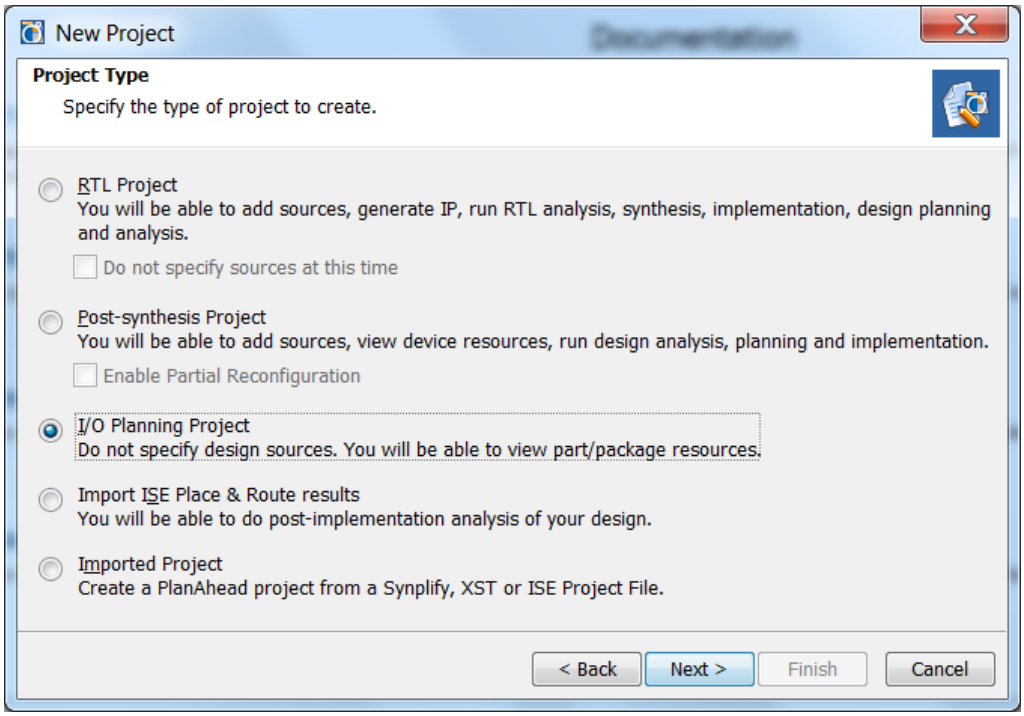

Figure 2: Specifying an I/O Pin Planning Project

10. Click **Next** to open the Import Ports dialog box.
11. Select **Do not import I/O ports at this time**.

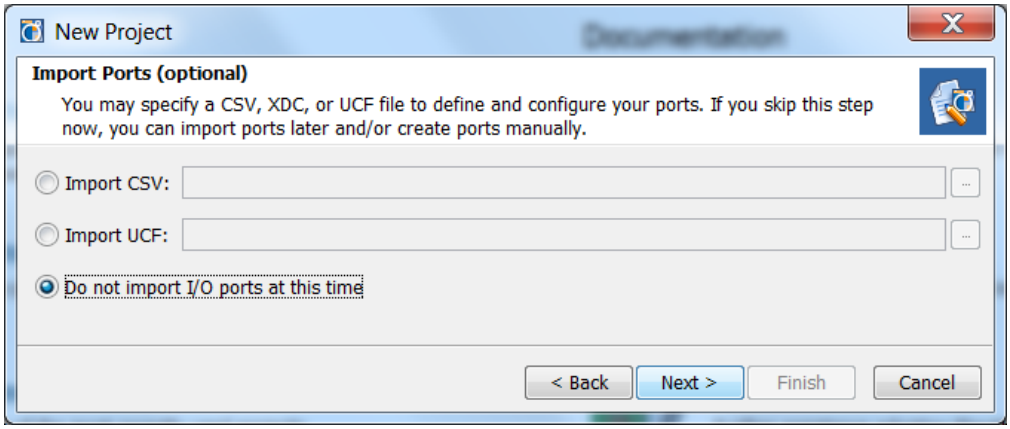

Figure 3: Import Ports from Existing UCF or CSV Files

12. Click **Next** to open the Default Part selector dialog box.
13. In the Filter section, click the **Family** pull down menu and select **Kintex-7**. Notice the list is filtered to show those devices.
14. In the Search field, type **70T**. Notice the 70T devices.

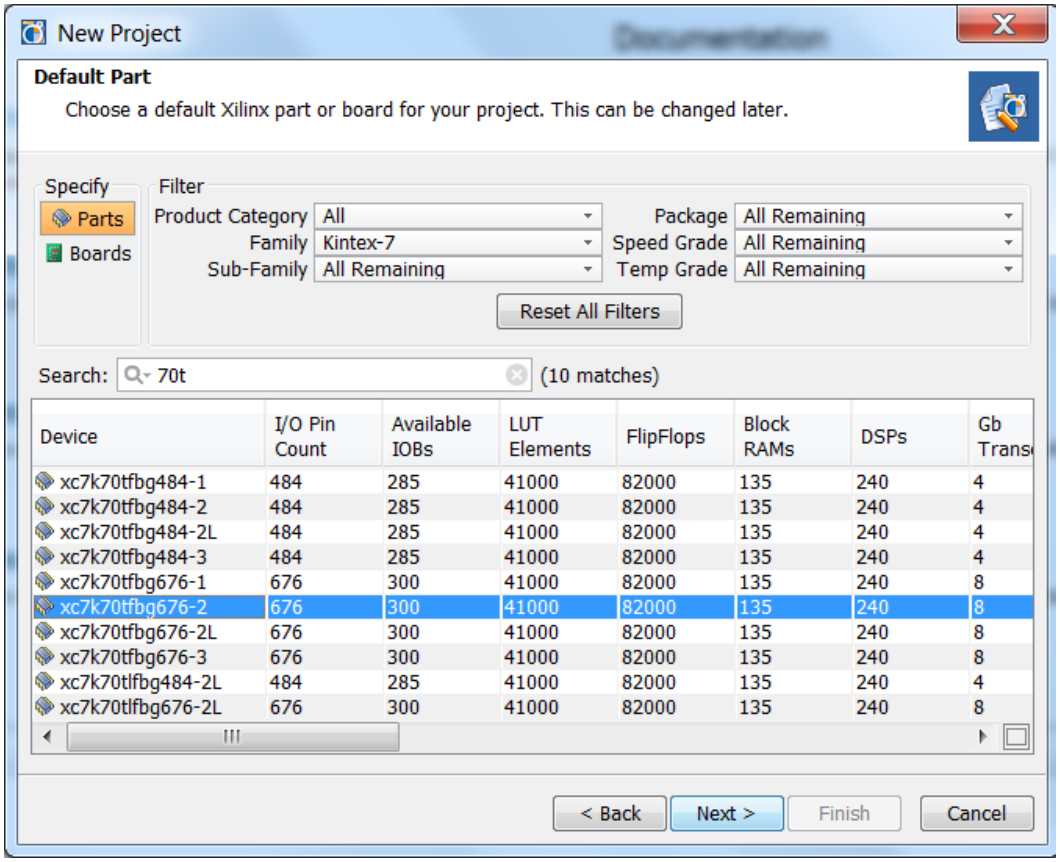

Figure 4: Selecting a Family and Default Part

15. Select the **xc7k70tfbg676-2** device and click **Next**.
16. Click **Finish** to create the project.

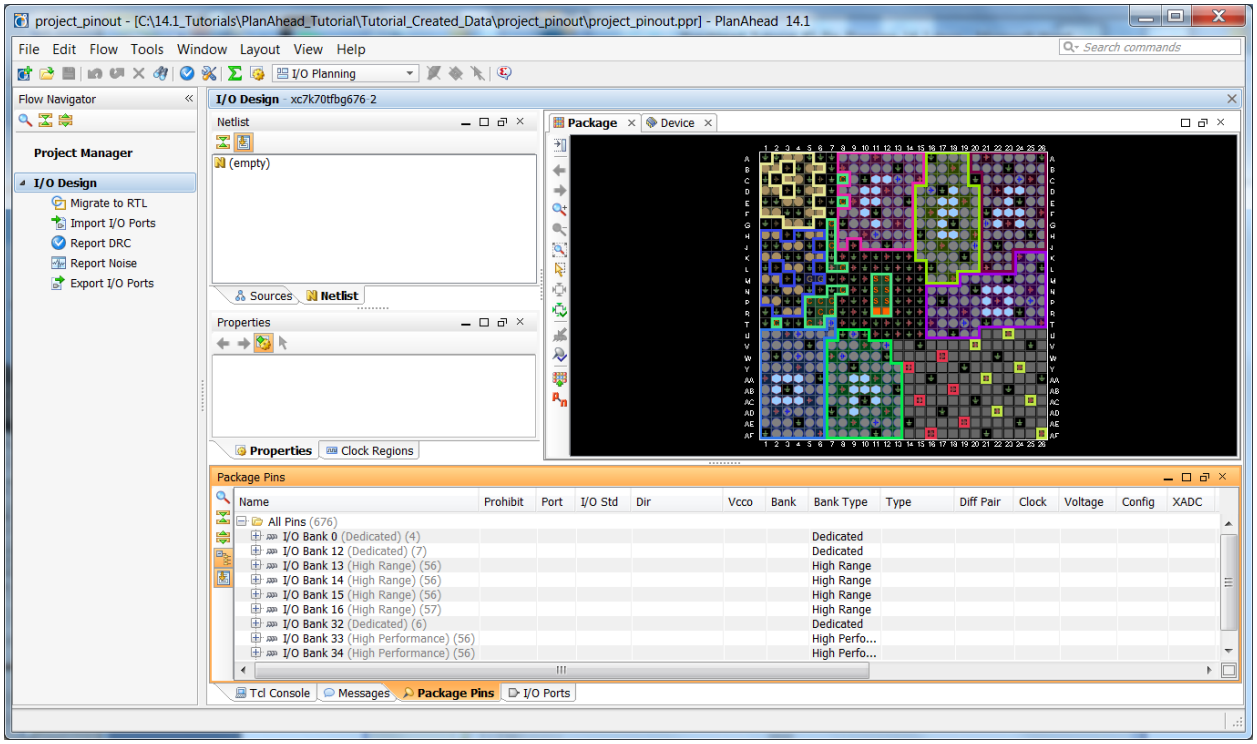

Figure 5: I/O Pin Planning Environment

17. Explore the various views in the I/O Planning layout. Many are empty because I/O Ports are not yet defined.

18. Right-click on either the Device or Package view tabs to select **New Vertical Group**.

    Notice that the Device and Package views are now both displayed. Being able to visualize the I/O bank locations both internally on the die and externally on the package helps you plan for an optimal I/O port assignment.

Step 2: Examining Device I/O Resources

The PlanAhead tool I/O pin planning environment lets you explore various device resources.

The different views graphically display and cross-select the location of various I/O, clock, and logic objects to help you make I/O and device-related design decisions. The Package Pins view and I/O Bank Properties view provide some I/O related information typically found in the device data sheets.

Next, you:

- Select several I/O banks to show the package-to-die relationship
- View I/O bank properties
- Select and expand the I/O Bank 14 to view package pin specifications

Examining I/O Banks

1. In the Package Pins view, select an I/O Bank such as **I/O Bank 33**.

   Notice that I/O Bank 33 is selected in the Device and Package views.

2. To select a bank in the Package view, double-click any pin from the I/O bank. The first click selects the pin, and the second click selects the I/O bank in which that the pin is a part of.

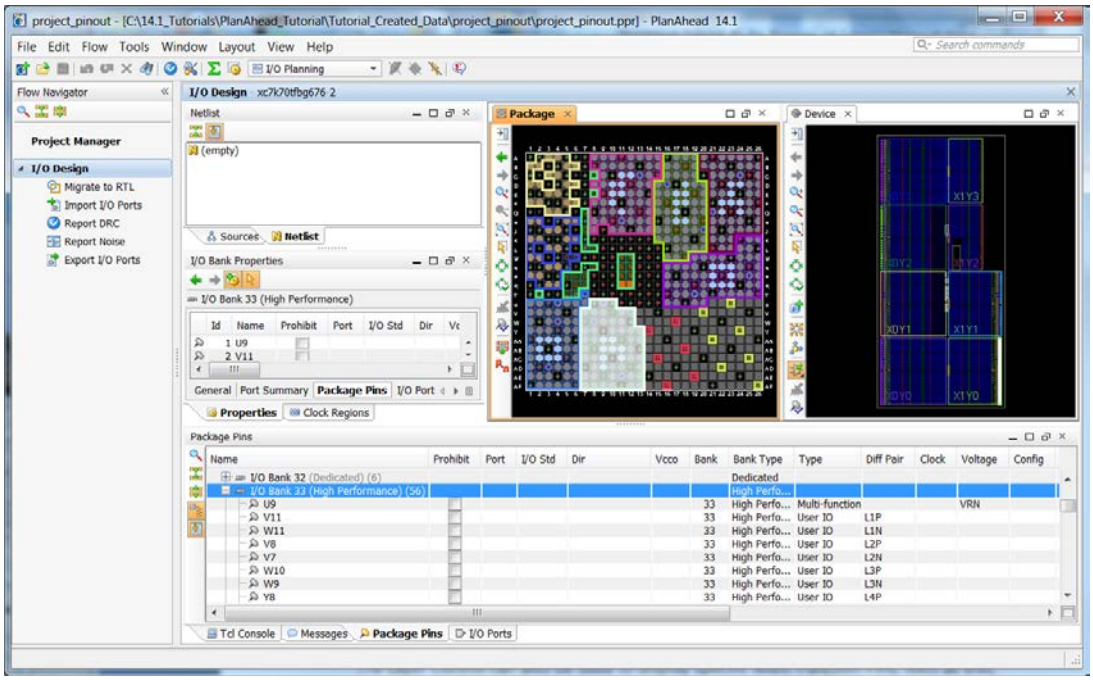

Figure 6: Cross Highlighting I/Os and I/O Banks

An alternate method is to click the **Package View Layers** button, located in the Package View toolbar. Expand the I/O Banks, select any I/O Bank, right click it and choose **Select Objects**.

The Layer Control can also be used to display specific Multi-Function Pins, such as Vref, adjust the look of the Package view, highlight specific bank types, or hide transceiver banks.

The selected I/O bank location is highlighted in the Package view.

3. Expand the selected **I/O Bank** in the Package Pins view to display the package pin information for each pin in the I/O Bank. The internal package trace min and max delays are shown also (scroll the view to the right to see them). These are the routing delays between the pin on the package and the pad on the die.

4. Scroll down the list and select any I/O Bank.

5. Select the **General** tab in the I/O Bank Properties view.
6. Review the I/O count and voltages. This information is populated as I/O Ports are assigned to the I/O bank. This allows you to search for compatible I/O banks to place the remaining I/O Ports.
7. Select the various tabs in the I/O Bank Properties view.
8. Click the **Maximize** button in the Package Pins view banner.

   The Package Pins view is maximized.
9. Select the **Expand All** button in the Package Pins view.
10. Scroll to the right and view the pin information in the table.
11. Unselect the **Group by I/O Bank** button in the Package Pins view to expand and flatten the list.

Step 3: Prohibiting Pins from I/O Assignment

You can prohibit I/O package pins from having I/O Ports assigned to them. In the following sequence, you will sort the Package Pins view by Voltage to select all VREF I/O pins, then use the Set Prohibits popup command to prohibit placement on those pins.

1. Click the Voltage column header twice and scroll to the top of the list to locate the VREF values.
2. Use the Shift key to select all VREF Voltage pins.
3. Right-click and select Set Prohibit.
4. In the Package Pins view header, click the Restore button .
5. The Package Pins view is restored. The Package view now displays prohibited pins.
6. In the main toolbar, click Unselect All .
7. Zoom in to an area of the Package view to view the Prohibited pins marked with red s, as shown in the following figure. To zoom, click and drag a rectangle in the Package view starting with a click at the upper left of the zoom area and drag to the lower right zoom area.

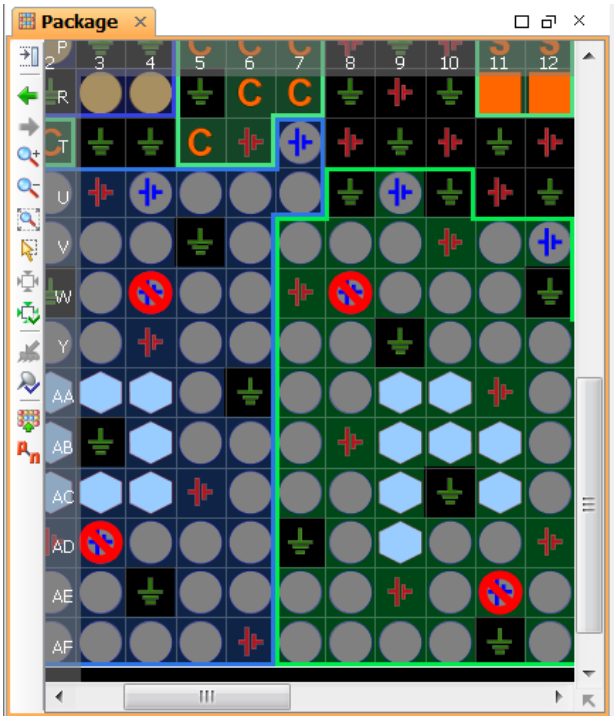

Figure 7: Examining Prohibited VREF Package Pins

8. Zoom Fit the Package view. Click and drag the cursor from the lower right to the upper left in a diagonal motion.

Step 4: Creating and Configuring I/O Ports

In this step you will create and configuring a new I/O bus port called **mybus**.

1. Click the **I/O Ports** view tab.
2. Right-click in the I/O Ports view and select **Create I/O Ports**.

   The Create I/O Ports dialog box opens.

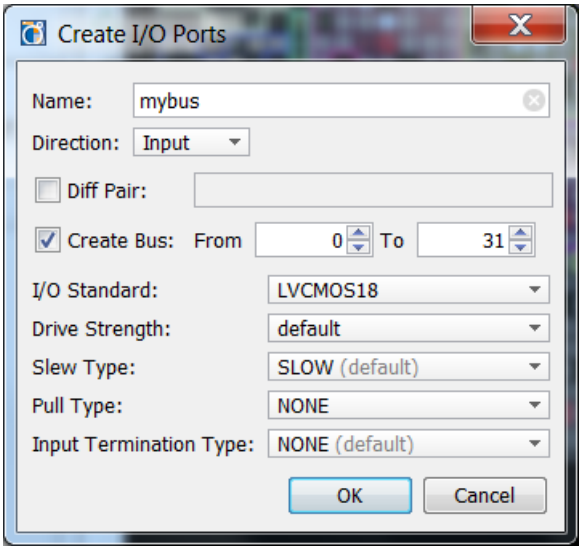

Figure 8: Create I/O Ports

Note: The Configure I/O Ports command opens a similar dialog box that enables you to configure existing I/O Ports.

3. Type **mybus** in the Name field.
4. Click the checkbox for **Create Bus**.
5. Select the default I/O Standard **LVCMOS18** from the drop down menu.
6. Review the other options and click **OK**.

   The new I/O Ports display in the I/O Ports view.

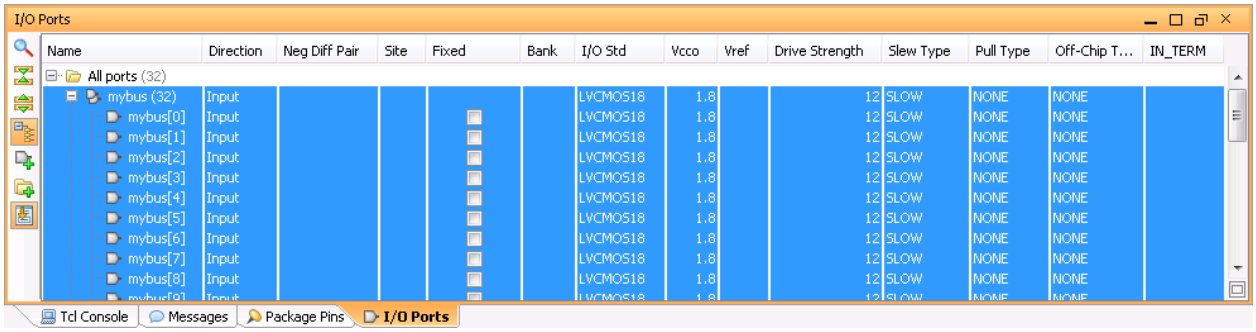

Figure 9: Displaying Newly Added I/O Ports

7. Select **Edit > Undo** to remove the recently added mybus I/O ports.

Step 5: Importing an I/O Port List

The PlanAhead tool can import a variety of file formats to begin the I/O pin planning process. You can import CSV, UCF, or RTL format files and perform I/O pin exploration and assignments. You can also create I/O Ports interactively, which was covered in the last step.

Use care with early input methods for I/O pin planning. Without a synthesized netlist, the I/O Ports placement and DRC routines do not take clocks, clock relationships, or GT logic into account in their calculations. When possible, perform I/O pin assignment after importing a synthesized netlist. Legal I/O pinouts are guaranteed only after the design has run through the ISE implementation tools, and after DRCs for I/O and clock placement are run without error.

Importing and Examining the CSV Format I/O Port List

1. In Windows Explorer, open the following I/O Ports CSV file:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/IO_Ports_import.csv`

2. Examine the I/O ports spreadsheet format and content, and exit without saving.

3. In the PlanAhead tool environment, select **Import I/O Ports** from the Flow Navigator, located on the left side.

4. Select CSV File and browse to select:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/IO_Ports_import.csv`

5. Click **OK**.

   The Device and Package views display the assigned Ports, and the I/O Ports view is now populated with the imported I/O Ports, as shown in the following figure. If you are going to import a CSV file, do this before defining ports with the Create I/O Ports command because they will be overwritten.

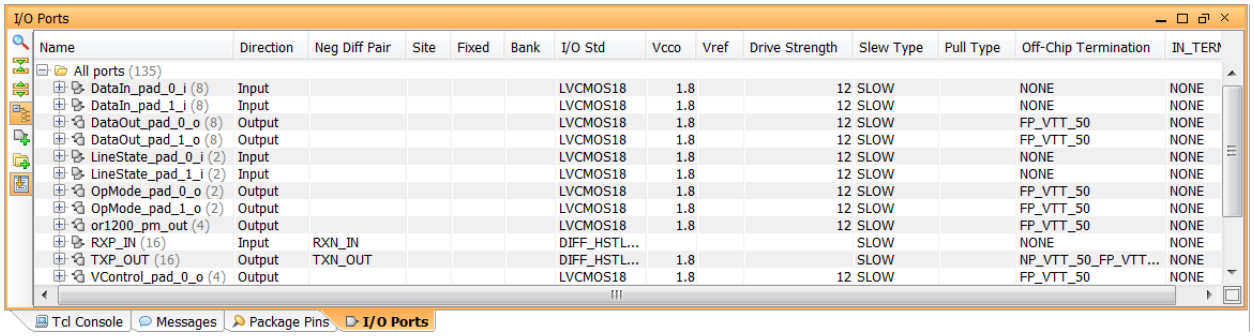

Figure 10: I/O Bus Ports are Grouped by Bus

The buses are grouped together and are expandable.

Step 6: Exporting the Device and I/O Pin Assignments

You can export the I/O Port assignments to UCF, CSV, VHDL or Verilog format files. This is useful for creating HDL headers and PCB schematic symbols. The CSV format output file contains package information for all pins, which can be used to begin I/O Port assignments.

Exporting the I/O Ports List Using the Export I/O Ports Command

1. Select **File > Export > Export I/O Ports**.
2. Select CSV, UCF, Verilog, and VHDL in the Export I/O Ports dialog box.

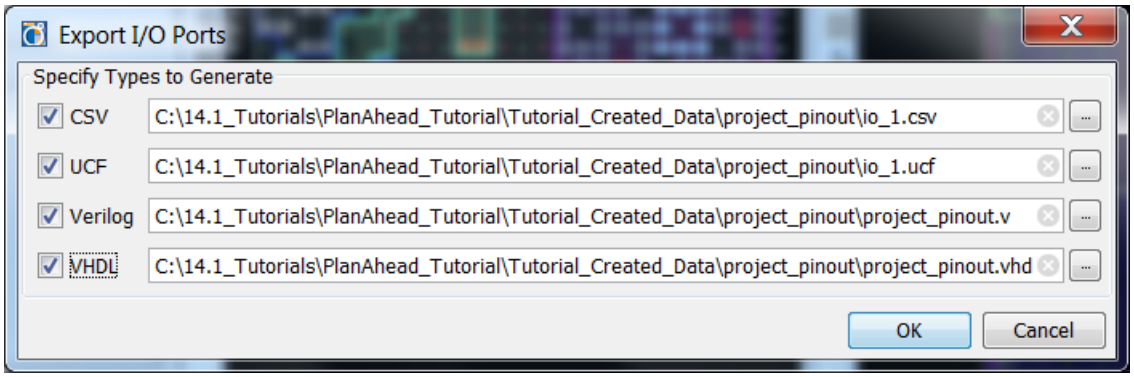

Figure 11: Exporting I/O Ports to a CSV Spreadsheet and UCF File

3. Click **OK** to accept the default file names and locations.
4. Open an Explorer window and browse to, and open the exported files located in:

   <*Extract_Dir*>/PlanAhead_Tutorial/Tutorial_Created_Data/project_pinout

   If defined, the Interface group names are included in the spreadsheet. Printed circuit board designers can use this spreadsheet to create Interface-specific schematic symbols. Creating I/O Port Interfaces is covered in an upcoming step.

Step 7: Migrating the I/O Planning Project to an RTL Project

You can migrate the I/O Port assignments made in I/O Planning Projects to an RTL Project. This enables additional Sources to be added and a path through to implementation. The I/O Port assignments and names will be translated into an RTL header and UCF Source files in an RTL Project.

Note: Once you migrate an I/O Planning Project to an RTL Project, you cannot go back to the original I/O Project.

1. Select **Migrate to RTL** in the Flow Navigator.

   The Migrate to RTL dialog box appears.

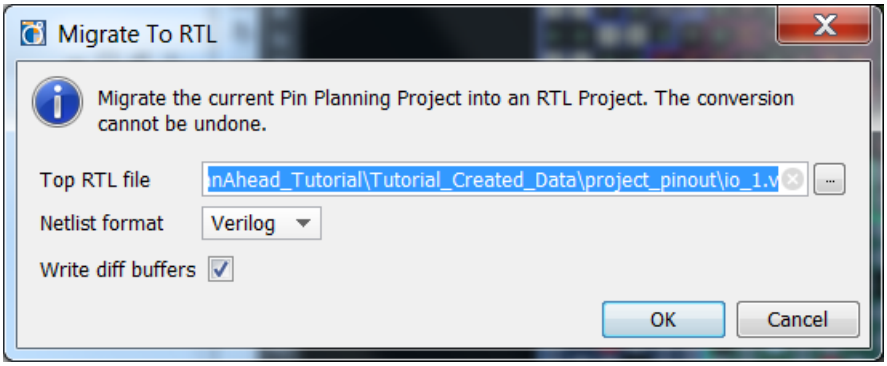

Figure 12: Migrating an I/O Planning Project to an RTL Project

2. Click **OK** to accept the default file names and locations.
3. Notice the RTL Project is now displayed. The Sources view contains the newly created source files.

Closing the Newly Created RTL Project

4. Select **File > Close Project**.
5. Click **OK** in the **Confirm Close Project** dialog box.

Part 2: I/O Planning Features using a Synthesized Design

Many of the features presented in this tutorial are available in several places during the design flow. As Part 1 describes, an I/O Planning Project can begin the I/O assignment process well before any RTL or synthesized netlist is available. In RTL Projects, I/O Planning can also be performed pre-synthesis by opening the elaborated RTL design. The most comprehensive set of features and DRCs are available after synthesis by opening the synthesized design.

The I/O Planning features provide several ways to analyze, group and place the I/O ports onto package pins or the I/O die pads.

For control over I/O port placement, you can drag the selected I/O Ports into the Package or Device views interactively using one of the following semi-automatic placement modes:

- Place I/O Ports in an I/O Bank
- Place I/O Ports in an Area
- Place I/O Ports Sequentially

In addition, the I/O Planning features enables you to toggle DRCs on and off during I/O placement.

Step 8: Opening the Synthesized Netlist-Based Project

1. Click the **Open Project** link in the Getting Started view, or select **File > Open Project**.
2. Browse to select the following project file:

   `<Extract_Dir>/PlanAhead_Tutorial/Projects/project_cpu_netlist/project_cpu_netlist.ppr`

   Alternately, select **Open Example Project > CPU (Synthesized)** from the Getting Started page. If needed, use **File > Save Project As...** to save a local writeable copy of the project at <*Extract_Dir*>`/PlanAhead_Tutorial/Tutorial_Created_Data`
3. In the Sources view, expand the Constraints **constr_1** folder and double-click on the **top.ucf** file.
4. Notice this UCF file only contains timing constraints and no I/Os yet.
5. Close the top.ucf file.
6. Select the **constr_1** folder and right-click to select **Make Active**.
7. Select **Open Synthesized Design** in the Flow Navigator to open the synthesized design.

   Alternately, you can select **Flow > Open Synthesized Design** from the main menu.
8. From the Layout pull-down located in the main toolbar, select **I/O Planning**.
9. The I/O Planning view layout displays.

Step 9: Examining the I/O Ports in the Design

10. In the I/O Ports view banner, click the **Maximize View** button .

11. Click **Expand All** in the I/O Ports view.

12. In the I/O Ports view, click to unselect **Group by Interface and Bus** .

13. Scroll down the list of buses and signals.

    The I/O Ports now display as a flat list rather than grouped by bus.

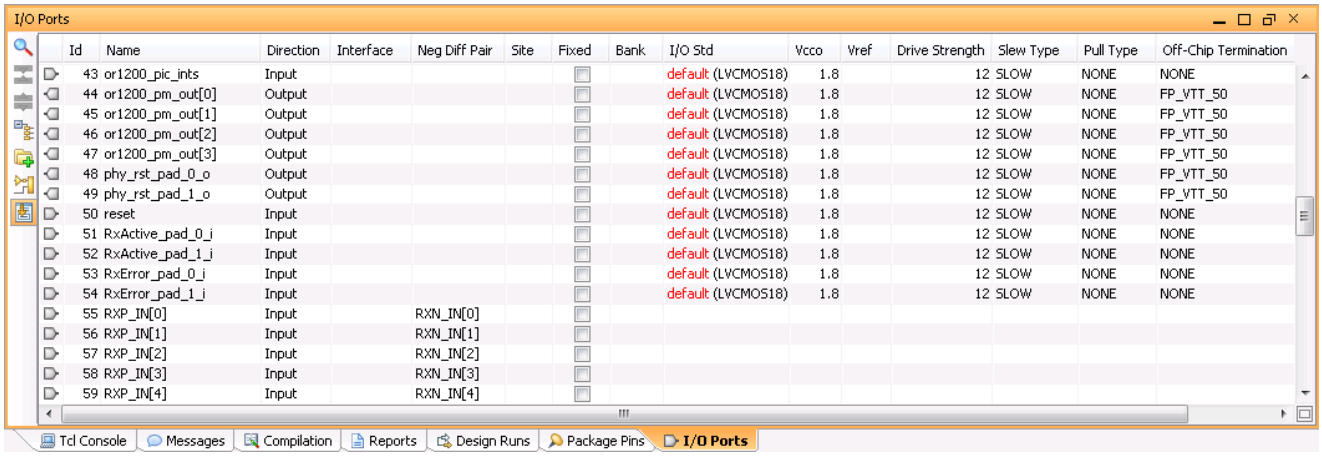

Figure 13: Examining I/O Standard and Diff Pair Requirements

The Neg Diff Pair fields are populated for some of the buses indicating that they are differential pair buses.

Step 10: Configuring I/Os and Setting I/O Standards

PlanAhead can be used to interactively sort and select I/O Ports to assign the proper I/O standard, drive strength, slew type, pull type and input termination constraints.

Note: For 7-Series devices, all I/O Ports must have explicit values for the IOSTANDARD constraint in order to generate a bitstream file. The word "default" is displayed in red to indicate that these values must be applied manually. The reason for this is that 7-Series devices have low and high voltage I/O Banks and extra care must be applied when assigning I/O standards.

Setting the I/O Standard Constraints

1. Click on the **Neg Diff Pair** column header to sort by diff pair port type.

2. Scroll to the top of the list and you should see no Neg Diff Pair ports, select the first port.

3. Use the Shift key and scroll to select all I/O Ports that are not diff pair ports.

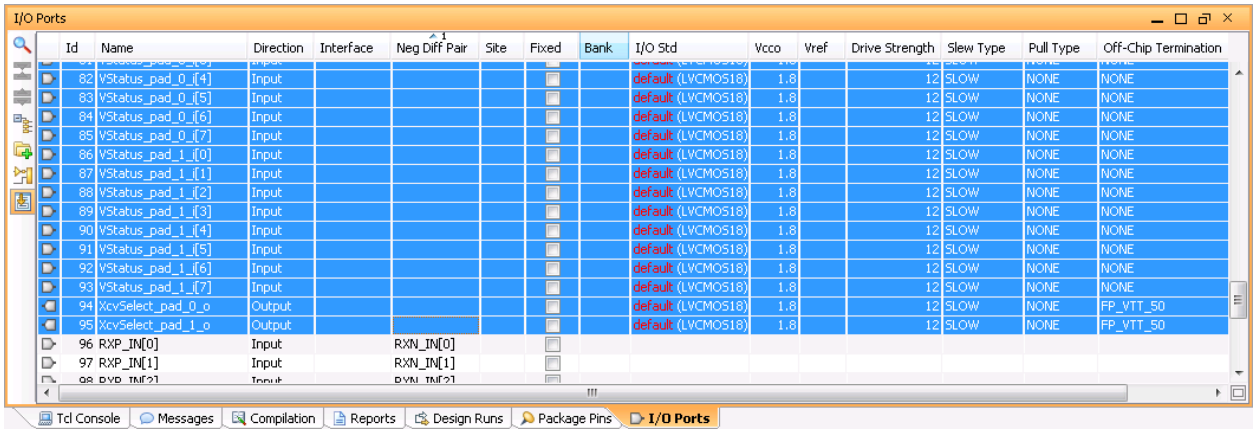

Figure 14: All Single Ended Ports Selected

4. Right-click and select **Configure I/O Ports**.

   Notice the various drop-down menus to set I/O Configuration constraints. The I/O standard field displays the default value.

5. Click in the **I/O Standard** drop-down menu to scroll to select **LVCMOS18** and click **OK**.

   Notice the I/O Std column entries are now set to LVCMOS18.

   The Neg Diff Pair signals are associated with GT pins, so an I/O standard is not applicable. Once these Ports are placed on GT pins, these fields will be empty.

Step 11: Creating I/O Port Interfaces

It can be beneficial to group I/O Ports associated with various I/O interfaces. The I/O Planning layout lets you define groups of pins, buses or other interfaces together as an "Interface." This ability helps with I/O Port management and with generating interface-specific PCB schematic symbols. It also forces the I/O Port automatic placement command to group the entire interface together on the device (where possible).

Creating Interfaces for Similar I/O Port Groups

The design used in this tutorial has two USB interfaces, each containing many I/O ports. The I/O port names are differentiated by `_0_` and `_1_`. You will create Interfaces for all signals in `USB0` and `USB1`.

1. Click the **Show Search** button  in the I/O Ports view.
2. Type **_0_** in the Search field.

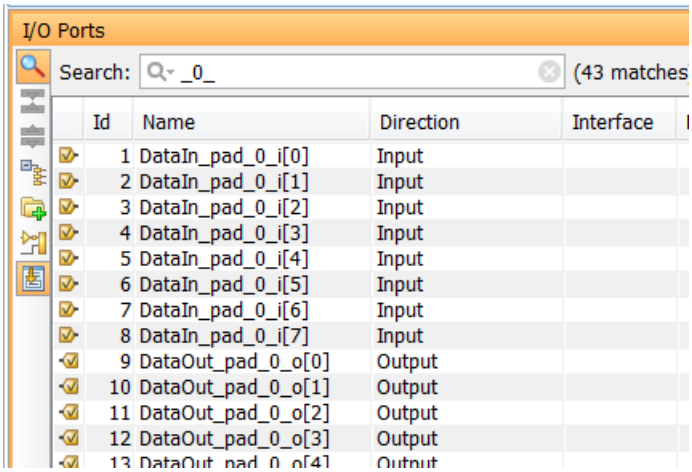

Figure 15: Selecting USB_0_ Related Ports

3. Select one of the ports in the filtered list.
4. Press **Ctrl+A** to select all ports in the filtered list.
5. Right-click and select **Create I/O Port Interface...**.

   The Create I/O Port Interface dialog box opens.
6. Type **USB0** in the Name field.

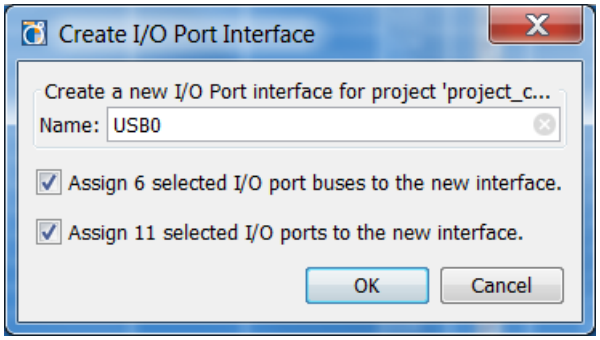

Figure 16: Create I/O Port Interface

7. Click **OK**.
8. In the Search field, change **_0_** to **_1_** and follow the same steps to create a USB1 I/O Port Interface.
9. Click the **Show Search** button to remove the Search filter.
10. Click the **Group by Interface and Bus**, and the **Collapse All** buttons.

    The I/O ports list is condensed with all of the USB related ports in Interface groups.

11. Expand the **Scalar ports** folder to view the clocks resets and other ports.

12. Click the **Restore** button in the view banner.

    The I/O Ports view is restored to the original location, shown in the following figure.

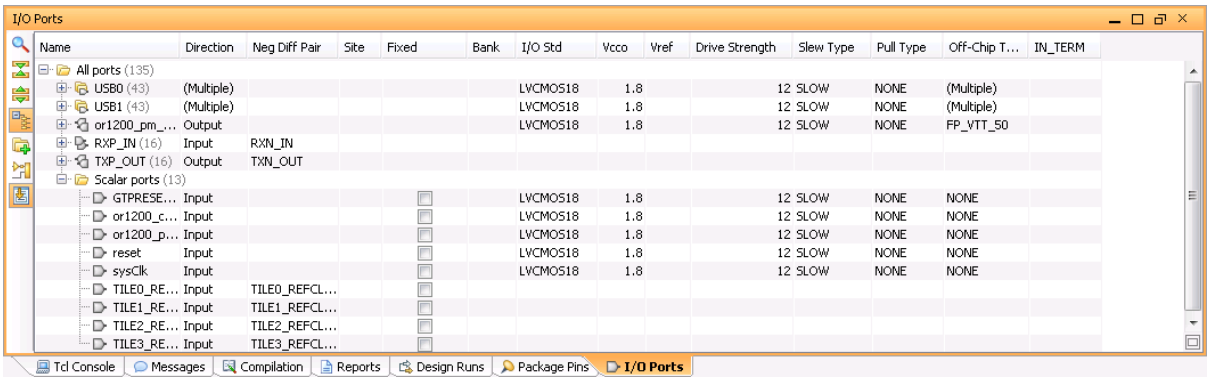

Figure 17: Viewing I/O Port Interface Groups and Scalar Ports

Step 12: Viewing Multi-function Package Pins

Some Xilinx devices have a set of package pins that can be used for a variety of purposes depending on the design configuration. These are referred to as Multi-function pins. The mode in which you intend to configure the device or the use of memory controllers or a PCI interface can require use of some of these pins. The Package Pins view can be examined to ensure that no conflicts exist. In this step you will view the package pins data and multi-functional pins.

1. Click the **Package Pins** view tab.

2. In the Package Pins view banner, click the **Maximize View** button .

3. Click **Expand All** in the Package Pins view

4. Scroll down and to the right to examine the pins information such as Bank Type, Clock, Voltage, Config, and Site Type. The information displayed in the Package Pins view is dynamically updated as I/O Ports are placed in the design.

5. In the Package Pins view, click to unselect **Group by I/O Bank** .

   The Package Pins now display as a flat list rather than grouped by I/O Bank.

6. Click the **Type** column header to sort based on the Type field.

7. Scroll to view the Multi-function pins

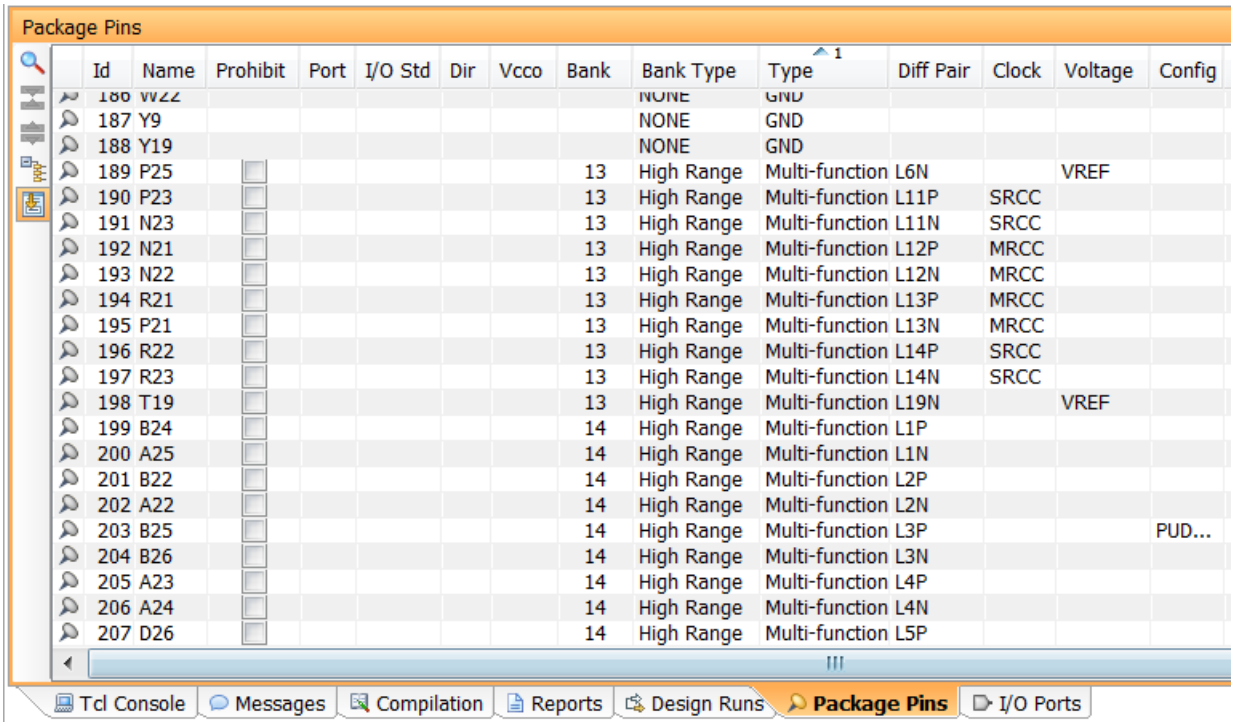

Figure 18: Viewing Multi-Function Pins

8. Examine the following columns:
   - Device Configuration pins (Config)
   - XADC
   - Gigabit I/O

   These logic objects can impact I/O assignment because many of them rely on multi-function pins and have fixed I/O requirements. If the design used in this tutorial contained these logic objects, this table would be filled out accordingly, allowing you to examine multi-function pins.

Restore the Package Pins view.

9. In the Package Pins view, click the **Group by I/O Bank** button .

10. Click **Collapse All** to return the tree table display to the default display structure.

Note: The PlanAhead tool has several tree table style views. There are search and filtering capabilities available in these views. See "Using Tree Table Style Views" in the *Using the Viewing Environment* chapter of the *PlanAhead User Guide (UG632)*for more information.

Step 13: Setting Device Configuration Modes

In the PlanAhead tool you can set one or more device configuration options. Some configuration modes can have an impact on multi-function I/O pins also. The related pins display this information in the **Config** column of the Package Pins view.

1. Select **Tools > I/O Planning > Set Configuration Modes...**. The Set Configuration Modes dialog box opens.

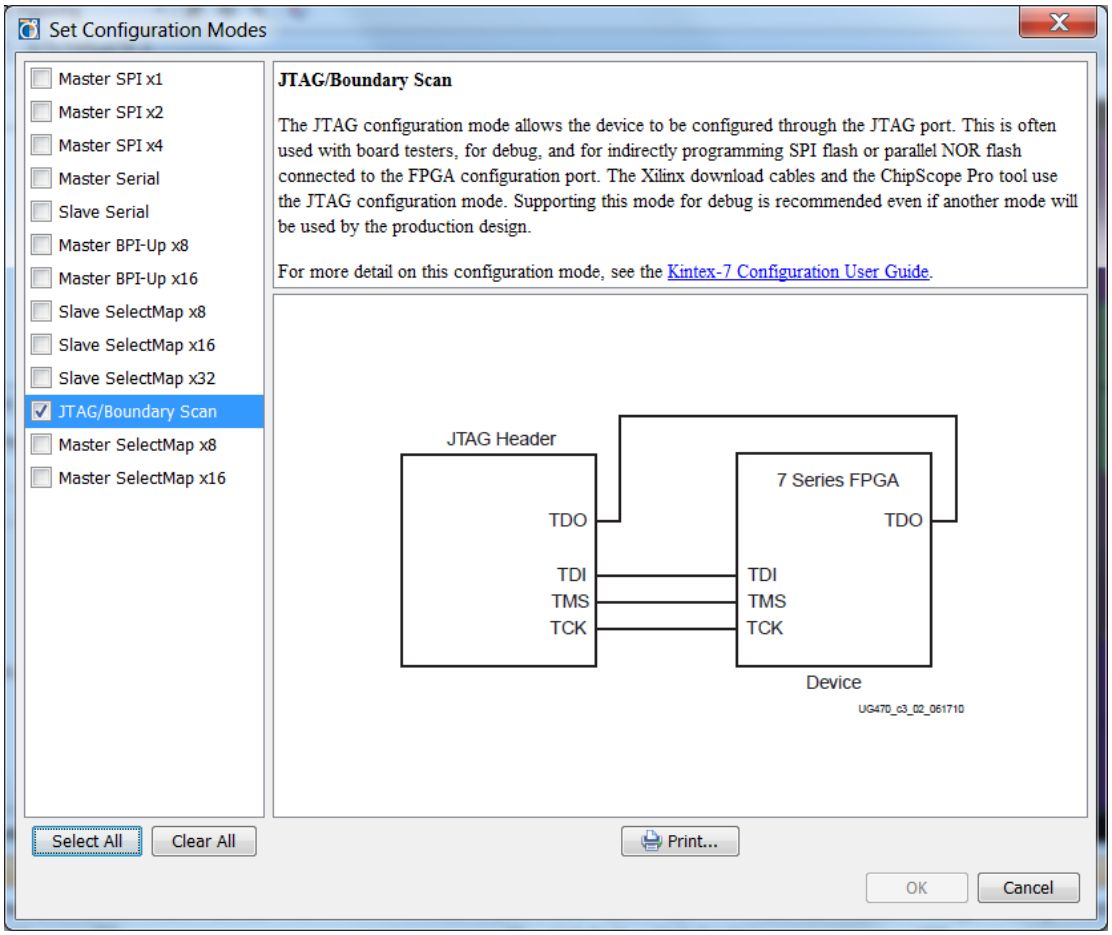

Figure 19: Selecting Device Configuration Modes

2. In the **Set Configuration Modes** dialog box, select one or two of the other modes to view the descriptions, schematics, and related data sheets.
3. Leave it set on **JTAG/Boundary Scan** and click **Cancel**.

   Setting a Configuration Mode results in the pins associated with it to be displayed at the top of the Package Pins view allowing you to examine potential multi-function pin conflicts.

Step 14: Defining Alternate Compatible Devices

During the FPGA design process, you can change the target device when a design decision calls for a larger or different type. The PlanAhead tool lets you define alternate compatible devices up-front so I/O assignments can work across the selected set of devices. This capability is typically limited to devices that use a common package.

This step ensures that the I/O pinouts work across the selected set of devices.

1. Select **Tools > I/O Planning > Set Part Compatibility...**.

   The Set Part Compatibility dialog box opens.

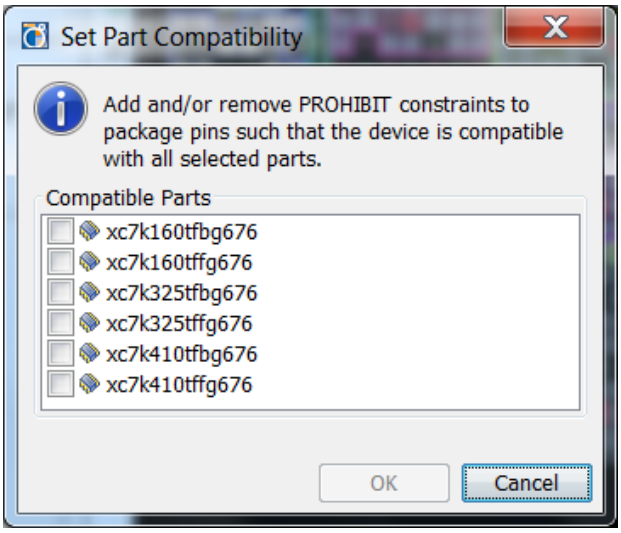

Figure 20: Defining Compatible Parts

2. Select the top **xc7k160tfbg676** device.
3. Click **OK**.
4. In the confirmation dialog box, click **OK** to indicate that no Prohibits were placed.

   The Prohibits are assigned based on the most restrictive parts. In this example you are targeting the smallest device for this package, so no prohibits are placed.

Step 15: Placing I/O Ports

The PlanAhead tool provides several ways to place the I/O Ports onto either package pins or I/O die pads. The automatic placement command tries to place the entire selected group of I/O Ports, adhering to I/O bank rules while grouping buses and Interfaces together.

By default, the PlanAhead tool uses interactive Design Rule Checks (DRCs) during I/O placement.

For more control over I/O port placement, you can drag the selected I/O Ports into the Package or Device views using one of the following semi-automatic placement modes:

- Place I/O Ports in an I/O Bank
- Place I/O Ports in an Area
- Place I/O Ports Sequentially

Placing the USB0 Port Interface using Place Ports in an I/O Bank

1. In the I/O Ports view, select the **USB0 Interface**.
2. In the Package view, click to expand the **Place Ports** button  .
3. Select **Place I/O Ports in an I/O Bank**.

   As you drag the cursor over the Package Pins, the assignment pattern displays the number of pins to be placed shows in the tooltip.

   The Information bar at the bottom of the PlanAhead tool displays information about the objects being dragged over, including I/O Banks and Package Pins.

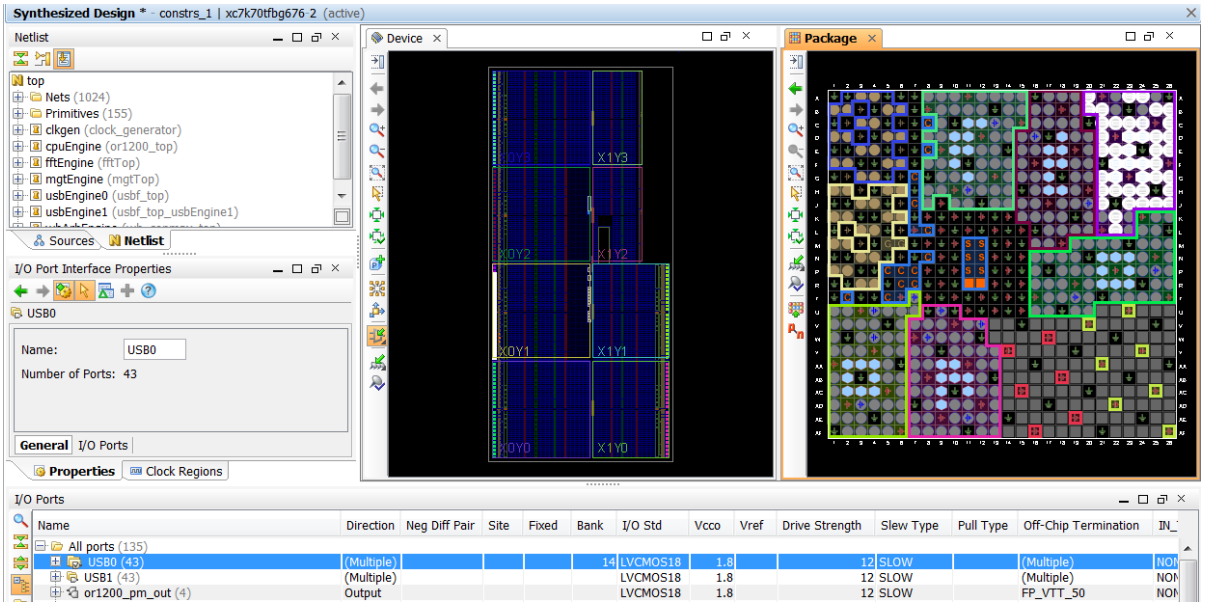

Figure 21: Place I/O Ports in an I/O Bank

4. Click **I/O Bank 14** on the top, right side of the package to drop the I/O Ports.

   The I/O Ports are assigned in the order in which they appear in the I/O Ports view. Assignment locations are vectored out from the initial pin selected.

Placing the USB1 I/O Port Interface using Place Ports in Area

5. In the Device view, zoom in to the upper half of the device.
6. In the I/O Ports view, select the **USB1 Interface**.
7. In the Device view, click to expand the **Place Ports** button .
8. Select **Place I/O Ports in Area**.

   The cursor displays a cross indicating that you can draw a rectangle.
9. Draw a rectangle starting at the bottom of the first I/O bank in the top half of the device and drag it up and to the right until all I/O Ports are placed in the rectangle within the top clock region.

Figure 22: Placing USB1 I/O Ports in an Area

Placing the RXP_IN Differential Pair Bus

10. Select the **RXP_IN** bus in the I/O Ports view.
11. In the Device view, click to expand the **Place Ports** button .

12. Select **Place I/O Ports Sequentially**.

13. Drag and click to place the first diff pair I/O Port into one of the GT I/O Banks on a designated pin. (Hint: the GT banks are the two upper left ones.)

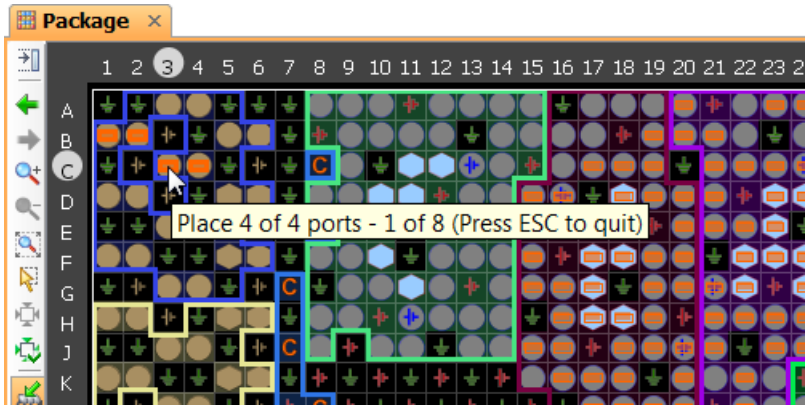

Figure 23: Placing Diff Pair I/O Bus Ports Sequentially

Both diff pairs associated with the GTs were placed on legal sites. You might see a tool tip indicating that the selected site is not legal and stating why it is not legal.

You can manually enter a pin location in the Site field in the I/O Port Properties view.

After placing the first set of GT diff pair pins, PlanAhead queues up the next group of pins to place.

14. Place all 8 RXP_IN GT Port groups in the two upper left I/O Banks. The cursor Tooltips will help guide you to legal pin selections to place the I/O Banks.

Note: GT logic objects are automatically grouped by PlanAhead to ensure proper behavior when I/O Ports are placed or moved. Both sets of Diff Pair I/O Ports as well as the GT itself are all placed and moved as a group.

Removing the Split Workspace View for the Device and Package Views

Now that the I/O Ports are placed, the Package view is no longer needed to share the Workspace view. The split view can be removed easily. To remove the split view:

15. Right-click on the Package or Device view tab to select Move to Previous Tab Group.

16. Select the Device view tab to bring it to the front.

17. Adjust the view size, and Zoom fit the view, if needed.

Step 16: Placing Clock Logic

The PlanAhead tool lets you place critical clock or I/O related logic. After a synthesized netlist is imported, clocks and clock relationships can be explored and used to lock down these logic objects onto specific device sites. The PlanAhead tool automatically groups some logic, such as GTs and their associated I/O pin pairs. This makes selection and placement of GTs and other related logic less prone to errors.

Searching for the Global Clock Logic in the Design

1. Click the Find button or select **Edit > Find**.

   The Find dialog box opens.

2. Adjust the selection filters to match the following figure (Type is Clock).

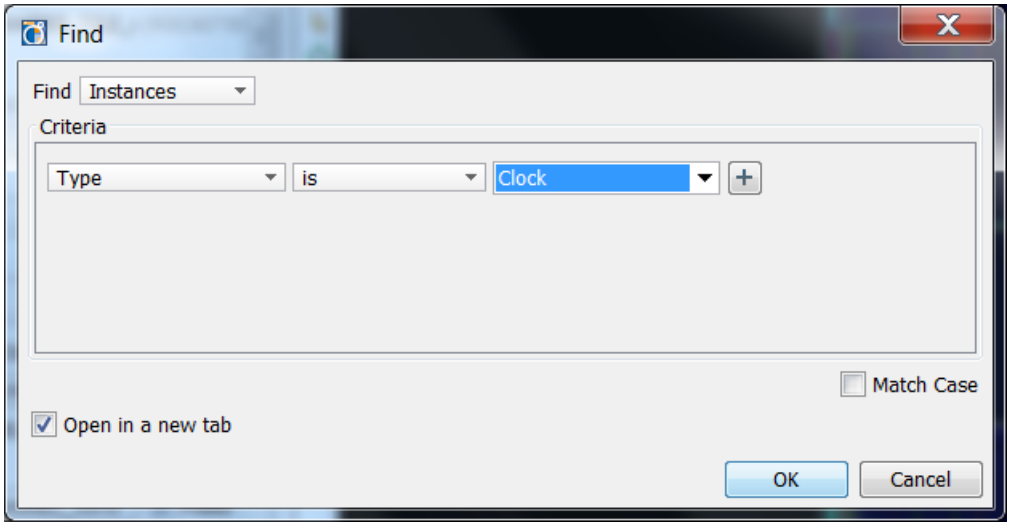

Figure 24: Using Find to Search for Clock Logic

3. Click **OK**.

   The Find Results view opens.

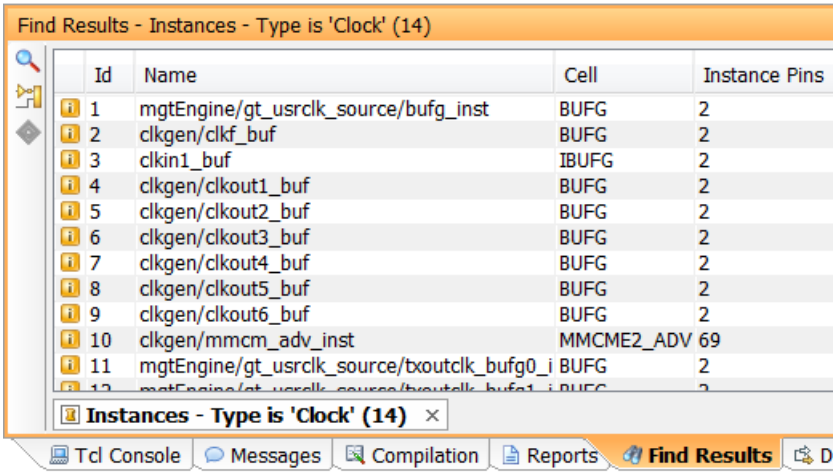

Figure 25: Viewing the Clock Objects Found

4. Scroll down the list of objects, and observe the following:
   - BUFG
   - MMCME2_ADV

Step 17: Using the Schematic to Trace Clock Logic

The Schematic view can be used to expand and explore any logic in the design. Placement constraints can be applied from the Schematic view.

1. In the Find Result view, select the first **MMCME2_ADV** Cell.

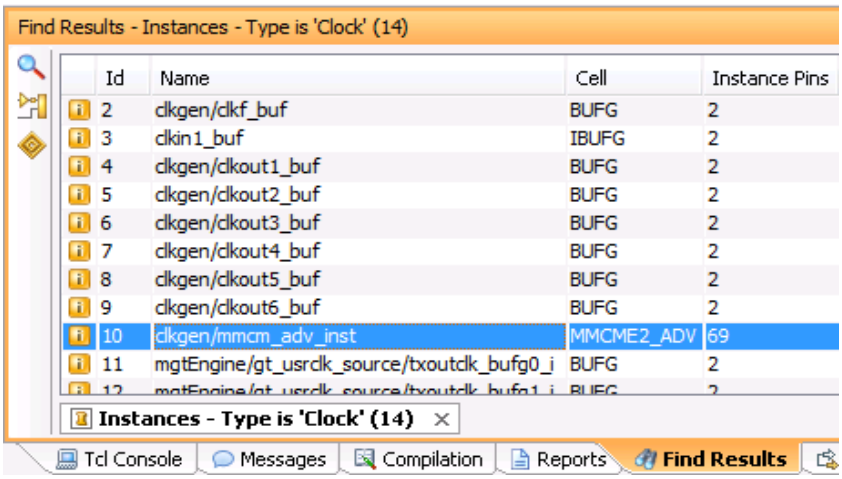

Figure 26: Selecting Clock Logic to Trace in the Schematic

2. In the Find Results view, click the **Schematic** button .

3. In the Schematic view, double-click the **CLKIN1** input port on the upper left of MCM module
4. Double-click to expand the **CLKFBIN** input pin on the MCM module.
5. Double-click on the 5 MCM output pins **CLKOUT1-5** to expand the BUFGs.
6. Clean up the connections by clicking the **Regenerate Schematic** button in the Schematic view .

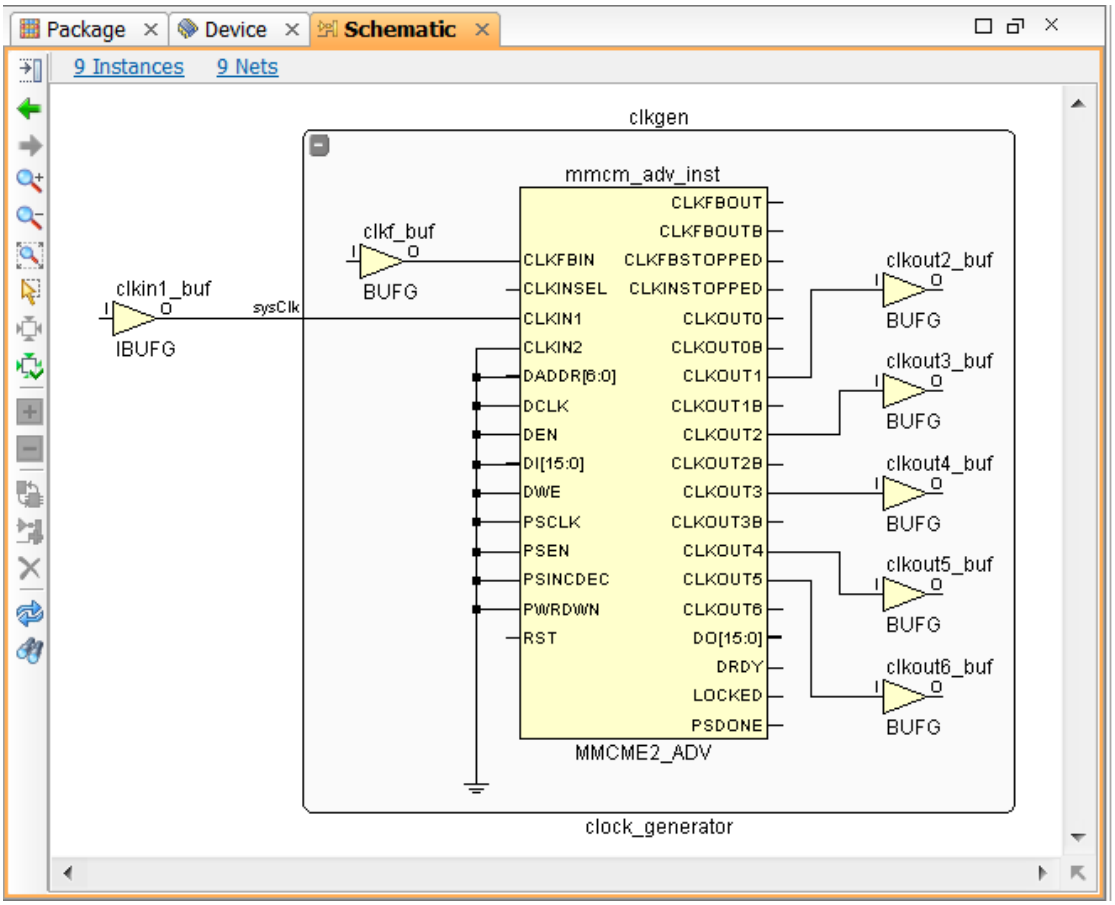

Figure 27: Exploring Clock Logic Connectivity

You can easily expand and explore logic in the Schematic view. Select or highlight logic in the Schematic view to cross-select or highlights it in all other views.

You can also drag logic directly out of the Schematic for placement into the Device, Package or Clock Resources view.

7. Close the Schematic view tab.

Step 18: Exploring the Clock Resources View

1. In the Workspace, select the **Clock Resources** view tab.
2. If no view tab exists, select **Window > Clock Resources** to display the view.
3. Click the **Maximize Workspace** button ☐ in the view banner to display the view full screen.
4. Scroll around and examine the Clock Resources view.

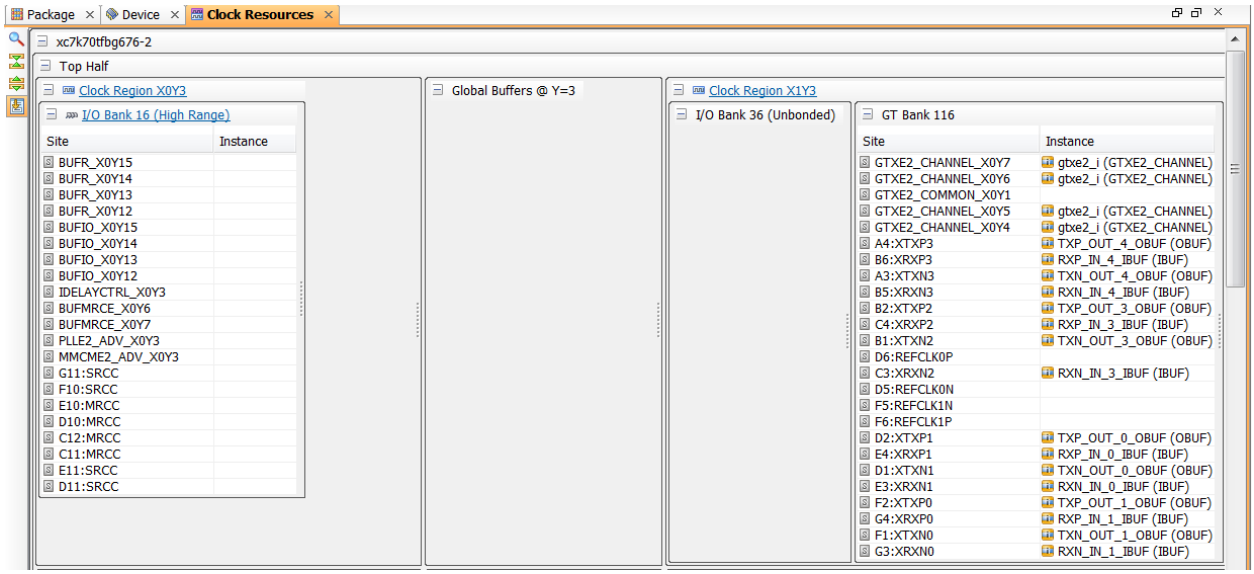

Figure 28: Viewing Clock Resources in the Clock Resources View

The Clock Regions, I/O Banks, and various device resources display in their relative location as found on the device.

You can expand or collapse sections of the Clock Resources to hide or display the resources as needed. Logic that is placed is displayed under the Instance columns.

Placed clock resources such the GTXE2s and their associated Diff Pair ports are displayed in the chart along with BUFGs and MMCMs

Step 19: Placing the MCM Instance

1. Click the **Find Results** view tab on the bottom of the screen to display the view.
2. Select the MMCME2_ADV instance and drag it into the Clock Resources view on the Instance field next to one of the MMCME2_ADV Sites.

Note: If the instance does not drag out of the Find Results view, click the Netlist view tab and drag to place it from there.

Notice how you can place clock and related I/O logic in the Clock Resources view.

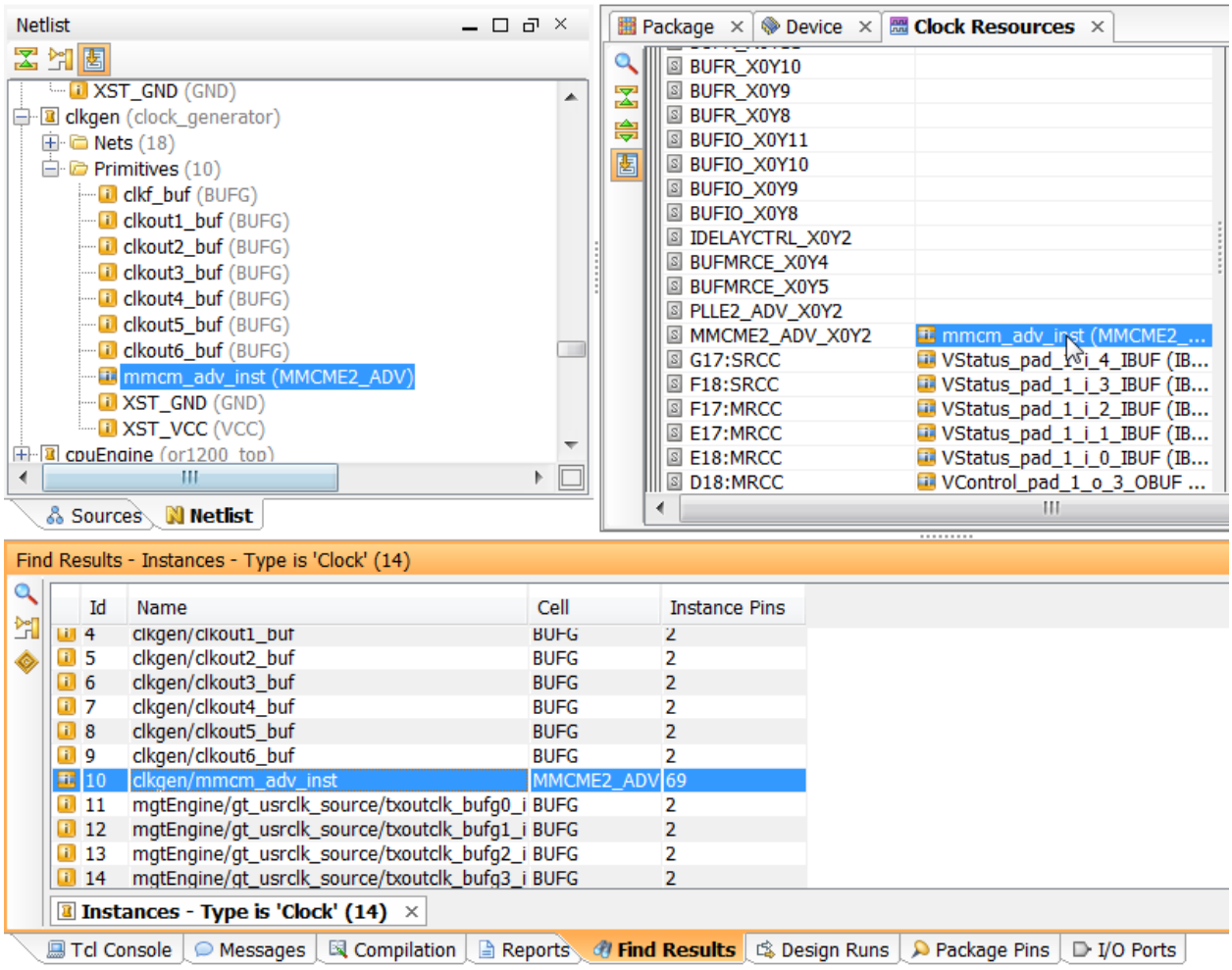

Figure 29: Displaying Placed MMCM_ADV Logic Instance

3. Close the Find Results view.
4. In the Clock Resources view, click the **Restore Workspace** button in the view banner to return the view layout.
5. Click the **Device** view tab in the Workspace.

Step 20: Running Design Rule Checks - "DRC"

The PlanAhead tool has an extensive set of I/O related DRCs to be sure that I/O Ports are assigned accordingly. You can explore and resolve any violations interactively.

Reporting the I/O Related DRC Checks

1. Click **Report DRC** in the Flow Navigator.
2. Deselect the **Placer, Netlist**, **Floorplan**, **DSP48**, and **RAMB** rule categories.

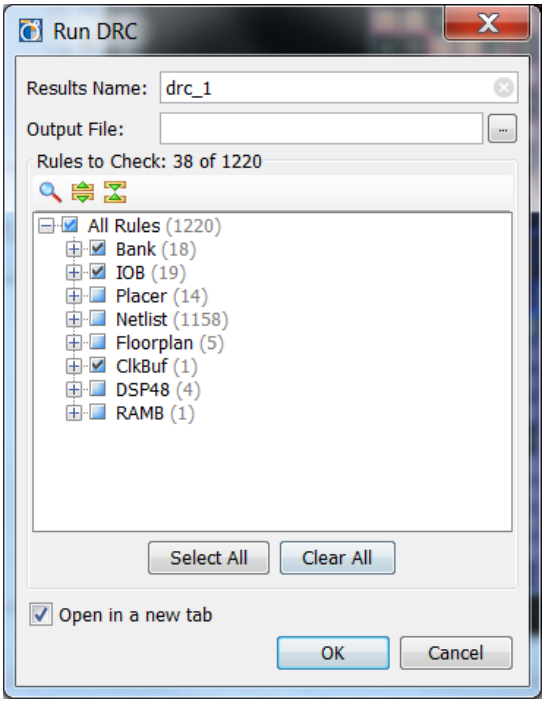

Figure 30: Run I/O Related DRCs

3. Expand the selected rules to examine the rule types.
4. Click **OK**.

   The DRC violations view now opens.

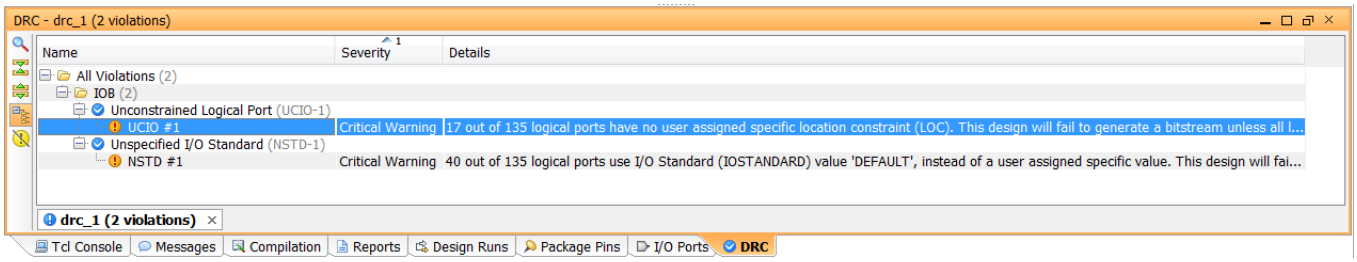

Figure 31: Reporting DRC Violations

The Violations indicate that I have several I/O Ports missing LOC and IOSTANDARD constraints. The design will fail to create a bitstream file as is. We could use the techniques describe in this tutorial to place and configure the remaining I/O Ports.

5. Select one of the Violations and examine the Violation Properties view

   Notice that links in the Violations Properties view allowing you to select the offending logic objects.

6. Close the DRC view.

Step 21: Running Simultaneous Switching Noise Analysis - "SSN"

Simultaneous Switching Noise (SSN) analysis can also be performed to help identify potential signal integrity concerns.

1. In the Flow Navigator, click **Report Noise**.
2. Click **OK** in the Run SSN Analysis dialog box.

   The Noise report view opens.

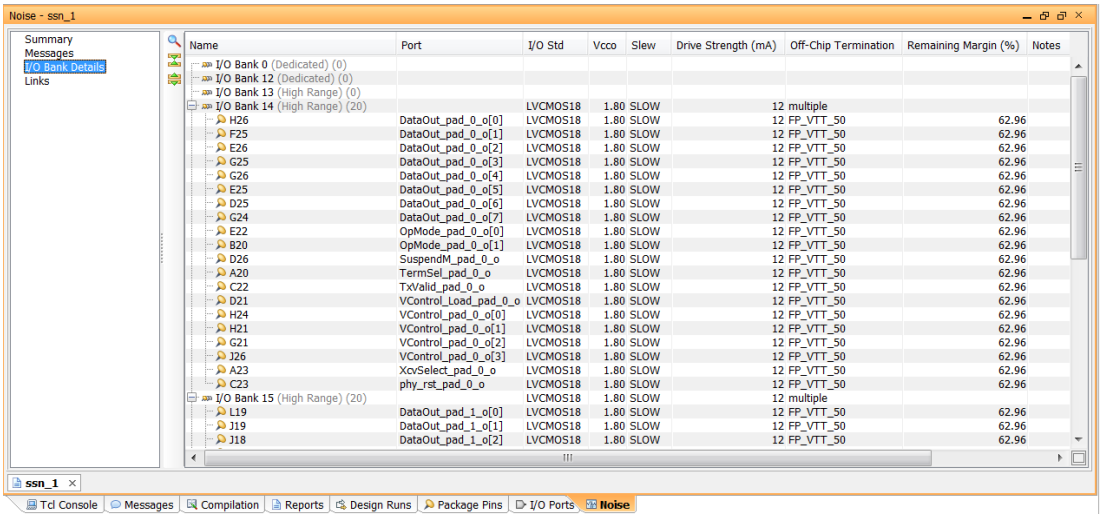

Figure 32: Noise Results View

Examining the SSN Results View

3. Maximize the Noise view and
4. Scroll down and expand the list of I/O Banks.
5. Select **Summary** in the upper left categories list and examine the information.
6. Select **Messages** and **Links** to examine the information.
7. Restore the Noise View.

Simultaneous Switching Noise (SSN) analysis can also be performed to help identify potential signal integrity concerns.

Step 22: Updating the Constraint Files with Interactive Assignments

PlanAhead is an interactive constraint assignment environment. Through the course of performing this Tutorial, we have made numerous modifications to the physical constraints in the design. These changes are currently stored in memory. Use the Save Design command to write the changes back to the project constraint files. The Save Design As command can be used to create a new Constraints Set containing all of the currently assigned constraints.

Save the Design

1. Select **File > Save Design**.
2. In the Sources view double-click the **top.ucf** file under Constraint folder constr_1.

   Notice the new physical constraints applied.
3. Close the top.ucf file.

Close the PlanAhead Tool

4. Select **File > Exit**.
5. Click **OK** to close PlanAhead.

Conclusion

In this tutorial, you:

- Used the I/O pin planning environment to explore device resources and define alternate compatible devices for the design.
- Imported, created, and configured I/O Ports.
- Created Interfaces by grouping the related I/O Ports together.
- Used the semi-automatic placement modes to assign critical I/O Ports to package pins. Placement of the remaining I/O Ports was done using automatic placement.
- Exported and examined the I/O Ports list, which can be used for HDL header or PCB schematic symbol generation.
- Opened a netlist-based project and placed GTXE, MMCM_ADV, and BUFG objects using logic connectivity as a guide for correct placement.
- Ran DRCs and Noise Analysis to validate legal I/O placement.
- Updated the constraint files with the interactive assignments.