

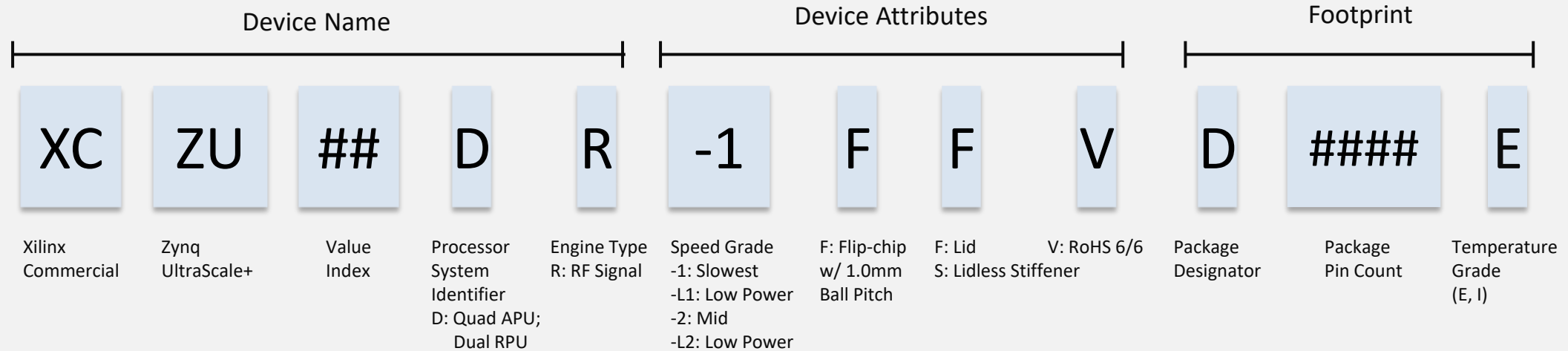
Zynq UltraScale+ RFSoc Product Tables and Product Selection Guide



PS	Device Name		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR		
	Gen 1							Gen 2		Gen 3						
	Quad-core Arm® Cortex®-A53 MPCore™ up to 1.3GHz, Dual-core Arm Cortex-R5F MPCore up to 533MHz															
RF Data Converter	12-bit RF-ADC w/DDC	# of ADCs	0	8	8	8	16	16	-	-	-	-	-	-		
		Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	-	-	-	-	-	-		
14-bit RF-ADC w/DDC	# of ADCs	-	-	-	-	-	-	-	8	2	4	8	4	8	8	16
	Max Rate (GSPS)	-	-	-	-	-	-	-	2.5	5.0	5.0	2.5	5.0	5.0	5.0	2.5
14-bit RF-DAC w/DUC	# of DACs	0	8	8	8	16	16	16	8	4	12	8	8	8	16	
	Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	6.554	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	
	SD-FEC	8	0	0	8	0	0	0	0	0	8	0	8	0		
	Number of DDCs per RF-ADC ⁽¹⁾	0	1	1	1	1	1	1	1	2	1	1	1	1		
	RF input Freq max. GHz	4						5		6						
	Decimation / Interpolation	1x, 2x, 4x, 8x						1x, 2x, 4x, 8x		1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x						
	System Logic Cells (K)	930	678	930	930	930	930	930	489	930	930	930	930	930		
	CLB LUTs (K)	425	310	425	425	425	425	425	224	425	425	425	425	425		
	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0		
	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0		
	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5		
	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272		
	GTY Transceivers	16	8	16	16	16	16	16	8	16	16	16	16	16		
	PCIe® Gen3 x16	2	1	2	2	2	2	2	-	-	-	-	-	-		
	PCIeGen3 x16/Gen4 x8 / CCIX ⁽²⁾	-	-	-	-	-	-	-	0	2	2	2	2	2		
	150G Interlaken	1	1	1	1	1	1	1	0	1	1	1	1	1		
	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	2	0	2	2	2	2	2		
	System Monitor	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI		
	Package Footprint	Package Dimensions		PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC		
	D1156	35x35		214, 72, 208 4, 16 0, 0												
	E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			
	G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8			
	F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16		
	H1760	42.5x42.5									214, 48, 312 4, 16 12, 12					

1. This value applies when all RF I/O of an RF-ADC tile are used.
2. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
3. For operation up to 10GSPS, contact your local Xilinx Sales Representative.

Zynq® UltraScale+™ RFSoc Ordering Information



E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = -40°C to +100°C)

Note: -L2E (Tj = 0°C to +110°C); -L2I (Tj = -40°C to +110°C)
Refer to [DS889](#), Zynq UltraScale+ RFSoc Data Sheet: Overview for additional information