LogiCORE IP 3GPP LTE Channel Estimator v1.0

XMP119 August 15, 2011 **Product Brief**

Overview

The Xilinx LogiCORE™ IP 3GPP LTE Channel Estimator v1.0 implements AXI4-Stream compliant, channel estimation functionality suitable to support decoding of the Physical Uplink Shared Channel (PUSCH) in LTE eNodeB applications as defined in the 3GPP TS 36.211 specification [Ref 1]. It represents one IP component in the Xilinx broader LTE Baseband Targeted Design Platform (TDP).

Features

- Drop-in module for Virtex®-6 devices
- AXI4-Streaming-compliant interfaces
- Support of channel estimation for 3GPP LTE Physical Uplink Shared Channel (PUSCH) with Single-Input, Single-Output (SISO) and Single-Input, Multiple-Output (SIMO) communication modes, Multi-User Multiple Input Multiple Output (MU-MIMO) communication modes
- Compliance with 3GPP-LTE TS 36.211 v.8.9 (Release 8) and v9.0 (Release 9) standard specifications
- Support of Xilinx LTE Uplink Targeted Design Platform (TDP)
- Parameterizable input/output data precision
- Bit accurate C-Language simulation model for system level modeling
- Optimized for Xilinx high performance Virtex-6 FPGAs

Applications

Base station applications implementing eNodeB following the LTE specifications [Ref 1]. The 3GPP LTE Channel Estimator v1.0 can perform the channel estimation function required for decoding of the PUSCH uplink data transmission in SISO and MU-MIMO modes of communication.

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/chest_lte_eval/index.htm.

References

1. 3rd Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 8), 3GPP TS 36.211 V8.9.0 (2009-12).
2. 3rd Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 9), 3GPP TS 36.211 V9.0.0 (2009-12).
3. XAPP1072: Target Platform Design for 3GPP LTE Uplink Receiver Application Note
4. DS749: LogiCORE IP 3GPP LTE MIMO Decoder v1.0 Product Specification

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Refer to the IP Release Notes Guide (XTP025) for more information on this core. There will be a link to all DSP IP and then to the relevant core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License and the core is generated using the Xilinx ISE® CORE Generator™ software. The CORE Generator software is shipped with the Xilinx ISE Design Suite software. For full access to all core functionality in simulation and in hardware, you must purchase a license for the core. Please contact your local Xilinx sales representative for information on pricing and availability of Xilinx LogiCORE IP modules. Information about additional modules is also available at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
09/21/10	1.0	Initial Xilinx release.
08/15/11	1.1	Updated to include web registration information.

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