LogiCORE IP Multiply Adder v2.0

DS717 March 1, 2011 **Product Specification**

Introduction

The Xilinx® LogiCORE™ IP Multiply Adder core provides implementations of multiply-add using XtremeDSP™ slices. It performs a multiplication of two operands and adds (or subtracts) the full-precision product to a third operand. The Multiply Adder module operates on signed or unsigned data. The module can be pipelined.

Features

- Drop-in module for Virtex®-7, Virtex-6, Kintex™-7, Virtex-5, Virtex-4, Spartan®-6, Spartan-3A DSP
- Generates mult-add and mult-subtract functions
- Supports twos complement-signed and unsigned operations
- Supports multiplier inputs ranging from 1 to 52 bits unsigned or 2 to 53 bits signed and an add or subtract operand input ranging from 1 to 105 bits unsigned or 2 to 106 bits signed
- Optional clock enable and synchronous clear
- Optional pipelined operation
- For use with Xilinx CORE Generator™ v13.1 or later

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Kintex-7, Virtex-7, Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3A DSP/XA
Supported User Interfaces	N/A
Provided with Core	
Documentation	Product Specification
Design Files	Netlist
Example Design	Not Provided
Test Bench	No Provided
Constraints File	Not Provided
Simulation Model	Verilog/VHDL
Tested Design Tools	
Design Entry Tools	CORE Generator 13.1
Simulation	Mentor Graphics ModelSim 6.6d, Cadence Incisive Enterprise Simulator (IES) 10.2, Synopsys VCS and VCS MX 2010.06, ISIM 13.1
Synthesis Tools	N/A
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.

Pinout

Signal names for the core symbol are shown in Figure 1 and described in Table 1.

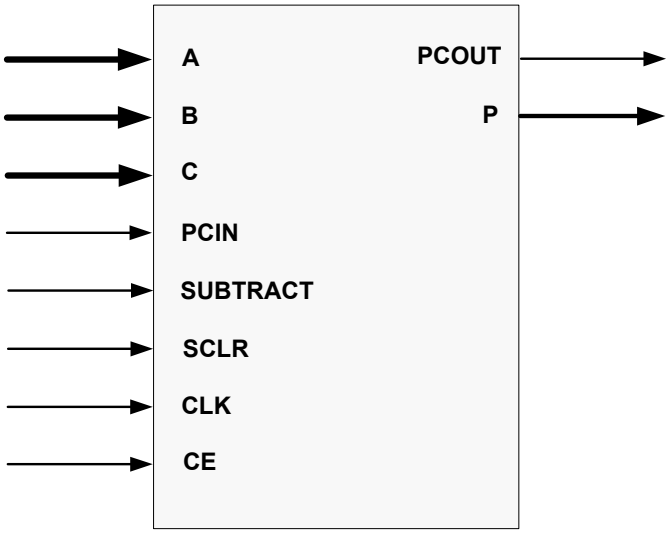

Figure 1: **Core Symbol**

Table 1: **Core Signal Pinout**

Name	Direction	Description
A[N:0]	Input	A Input bus (multiplier operand 1)
B[M:0]	Input	B Input bus (multiplier operand 2)
C[L:0](1)	Input	C Input bus (operand 1 of add/sub operation)
PCIN(2)	Input	Cascade Input
SUBTRACT	Input	Controls Add/Subtract operation (High = subtraction, Low = addition)
CE	Input	Clock Enable (active high)
CLK	Input	Clock (rising edge)
SCLR	Input	Synchronous Clear (active high)
PCOUT(2)	Output	Cascade Output
P[Q:0]	Output	Output bus

1. The multiplier output is added to or subtracted from the C port add/sub operand.
2. Cascade ports are described in Pipelined Operation.

CORE Generator Graphical User Interface Parameters

The CORE Generator GUI parameters for this module are described below:

- **Component Name**: The name of the core component to be instantiated. The name must begin with a letter and be composed of the following characters: a to z, 0 to 9, and "_".
- **A Input Width**: Sets the width of the Port A (multiplier operand 1) input. The valid range is 1 to 52 unsigned and 2 to 53 signed. The default value is 18.
- **B Input Width**: Sets the width of the Port B (multiplier operand 2) input. The valid range is 1 to 52 unsigned and 2 to 53 signed. The default value is 18.
- **C Input Width**: Sets the width of the Port C (add/subtract operand 2) input. The valid range is 1 to 105 unsigned and 2 to 106 signed. The default value is 48.
- **A Input Type**: Sets the type of the Port A data. 0 = signed, 1 = unsigned. The default value is 0.
- **B Input Type**: Sets the type of the Port B data. 0 = signed, 1 = unsigned. The default value is 0.
- **C Input Type**: Sets the type of the Port C data. 0 = signed, 1 = unsigned. The default value is 0.
- **Output MSB**: Output MSB. The default value is 47. See the section, Data Alignment for more information.
- **Output LSB**: Output LSB. The default value is 0. See the section, Data Alignment for more information.
- **Use PCIN**: When this parameter is set to 1, the PCIN port will be used. The PCIN port is the cascade input port for an adder/subtracter operand. When set to 0, the PCIN port is ignored. When set to 1, **C Input Width** is limited to 48 bits. The default value is 0.
- **Sync Control CE Priority**: This parameter controls whether or not the SCLR input is qualified by CE. When **Sync Control CE Priority** = 0, SCLR overrides the CE signal. When **Sync Control CE Priority** = 1, SCLR has an effect only when CE is high. The default value is 0.
- **A:B - P Latency**: Latency from the A and B Ports to the output port P. Valid values are: -1, 0; See the section, Pipelined Operation for more information. The default value is -1.
- **C - P Latency**: Latency from the C or PCIN Port to the output port P. Valid values are: -1, 0; See the section, Pipelined Operation for more information. The default value is -1.

Table 2 is a cross-reference table from the GUI parameters listed above to the XCO parameter names in the XCO file. The ranges and default values are also shown to facilitate data retrieval from the text above.

Table 2: **CORE Generator GUI and XCO Parameters**

GUI Name	Default Value	Valid Range	XCO Parameter
Component Name	xbip_multadd_v2_0_gui	..	Component_Name
A Input Width(1)	18	1..53	c_a_width
A Input Type	0 (signed)	0,1	c_a_type
B Input Width(1)	18	1..53	c_b_width
B Input Type	0 (signed)	0,1	c_b_type
C Input Width(1)	48	1..106	c_c_width
C Input Type	0 (signed)	0,1	c_c_type
Output MSB	47	0..106	c_out_high
Output LSB	0	0..106	c_out_low
A:B - P Latency	-1 (max speed)	-1,0	c_ab_latency
C - P Latency	-1 (max speed)	-1,0	c_c_latency
Use PCIN	0 (false)	0,1	c_use_pcin
Sync Control CE Priority	0 (false)	0,1	c_ce_overrides_sclr

1. See section above for exact ranges allowed for signed and unsigned data types.

Core Use Through CORE Generator

The CORE Generator GUI performs error-checking on all input parameters. Resource estimation and latency information are also available.

Several files are produced when a core is generated, and customized instantiation templates for Verilog and VHDL design flows are provided in the .veo and .vho files, respectively. For detailed instructions, see the CORE Generator software documentation.

Simulation Models

The core has a number of options for simulation models:

- VHDL behavioral model in the xilinxcorelib library
- VHDL UniSim structural model
- Verilog UniSim structural model

Xilinx recommends that simulations utilizing UniSim-based structural models are run using a resolution of 1 ps. Some Xilinx library components require a 1 ps resolution to work properly in either functional or timing simulation. The UniSim-based structural models might produce incorrect results if simulation with a resolution other than 1 ps. See the "Register Transfer Level (RTL) Simulation Using Xilinx Libraries" section in *Synthesis and Simulation Design Guide* for more information. This document is part of the ISE® Software Manuals set available at: www.xilinx.com/support/software_manuals.htm.

Pipelined Operation

The Multiply Adder takes into consideration two different latency paths; one from the A and B inputs to the P output and the other from the C/PCIN input to the P output. These latencies are defined as **A:B - P Latency** and **C - P Latency** and shown schematically in Figure 2.

These latencies can only take on two values: 0 for no latency or -1 for maximum/optimal latency. If either one of these two latencies are specified as -1, they are both treated as if they are -1; for a completely combinatorial design both must be set to 0.

One other factor that effects the latency is the availability and use of the cascaded PCIN port. Figure 2 shows the placement of registers inside the XtremeDSP slice implementation of the Multiply Adder in its pipelined configurations.

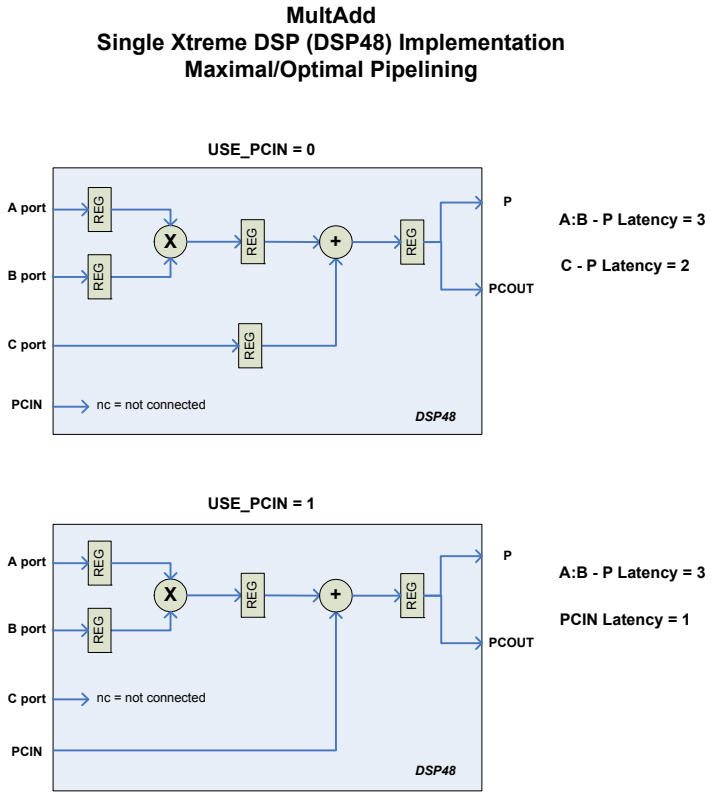

Figure 2: **Single XtremeDSP Slice Implementation**

Figure 3 shows the Multiply Adder configured using multiple XtremeDSP slices. Internally, the Multiplier and the Adder/Subtracter cores are used to create the wide multadd function. The latency variations from port-to-port for a multiple XtremeDSP slice implementation of a MultAdd are derived from the Multiplier and or the Adder/Subtracter latencies.

When the latency parameters are set to -1, there are functions that return the actual "A:B - P Latency" and "C - P Latency" values based on the setting of all the other parameters.

MultAdd
Multiple DSP48 Implementation

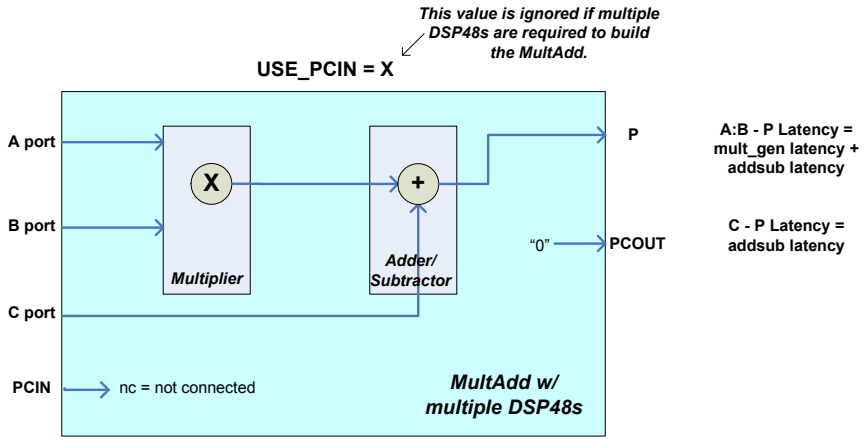

Figure 3: **Multiple XtremeDSP Slice Implementation**

Data Alignment

All inputs are right-justified when passed to the operators inside the core. The proper LSB or MSB padding or sign extending of the inputs (relative to the binary point) of the core are left to the user; this is true of all BaseIP (and the previous baseblocks) cores.

In the Multiply Adder, there is no truncation or rounding of the multiplier output; it is a full precision result. The C input is added to the product LSB-to-LSB. The example below shows how the operations take place. MSB and LSB positions can be chosen to extract the desired "slice" of output data. The slice shown in the example is taken from LSB = 0 to MSB = 11

A*B+C = P, where

A Width = 6

B Width = 8

C Width = 8

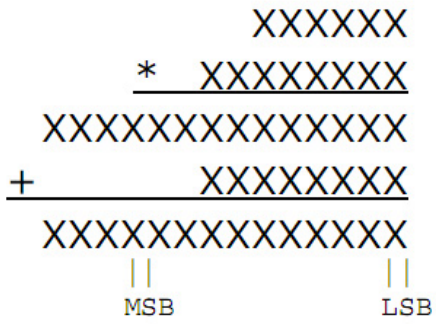

Figure 4: **Data Alignment Example**

Vector Multiply Example

Figure 5 shows a simple vector multiply and the necessary bit staggering required to line up inputs to the second and third MultAdd cores. The example below works for all supported bitwidths (i.e. single or multiple XtremeDSP slice implementations of the Multiply Adder). If the bitwidths of the core requires a multiple XtremeDSP slice implementation, then **Use PCIN** is disallowed and the result is provided via P only.

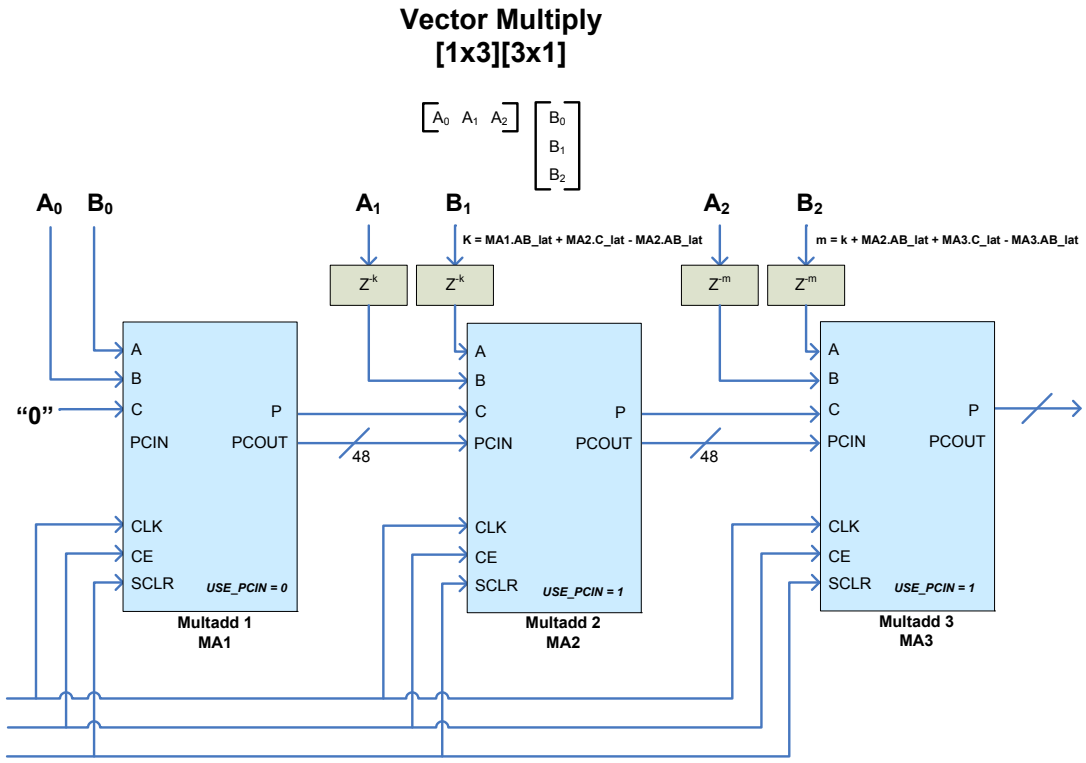

Figure 5: **Vector Multiply Implementation**

Performance and Resource Utilization

Table 3 and Table 4 provide Multiply Adder performance and resource usage for a number of different configurations.

The maximum clock frequency results were obtained by double-registering input and output ports to reduce dependence on I/O placement. The inner level of registers used a separate clock signal to measure the path from the input registers to the first output register through the core.

The resource usage results do not include the above "characterization wrapper" registers and represent the true logic used by the core.

The map options used were: "`map -pr b -ol high`."

The par options used were: "`par -ol high`."

Clock frequency does not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification.

The maximum achievable clock frequency and the resource counts may also be affected by other tool options, additional logic in the FPGA device, using a different version of Xilinx tools, and other factors. The Xilinx SmartXplorer™ script can be used to find the optimal settings.

All characterization was done using the following parameter settings unless otherwise noted:

- **A Input Type** = 0 (signed)
- **B Input Type** = 0 (signed)
- **C Input Type** = 0 (signed)
- **Sync Control CE Priority** = 1

Table 3: **XtremeDSP Slice Multiply Adder: Virtex-5 (Part = XC5VSX50T-1)**

Description	Non-Pipelined			Pipelined		
A Input Width, B Input Width	16	30	48	16	30	48
C Width	38	76	100	38	76	100
Max Clock Frequency (MHz)	152	57	35	450	448	276
LUT6-FF pairs	0	0	0	0	213	751
LUTs	0	0	0	0	0	262
Flip-flops	0	0	0	0	213	735
DSP48Es	1	6	12	1	6	12

Table 4: **XtremeDSP Slice Multiply Adder: Spartan-3A DSP (Part = XC3SD3400A-4)**

Description	Non-Pipelined			Pipelined		
A Width, B Width	16	30	48	16	30	48
C Width	38	76	100	38	76	100
Max Clock Frequency (MHz)	102	10	10	249	244	165
LUTs	0	0	0	0	60	472
Flip-flops	0	0	0	0	364	1174
DSP48As	1	6	12	1	6	12

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the IP Release Notes Guide (XTP025) for further information on this core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This LogiCORE IP module is included at no additional cost with the Xilinx ISE Design Suite development software and is provided under the terms of the Xilinx End User License Agreement. To generate the core, use the Xilinx CORE Generator system v13.1, which is included with the ISE Design Suite.

For more information, visit the core page.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

Revision History

Date	Version	Description of Revisions
4/24/2009	2.0	First customer release of Multiply Adder core.
3/01/2011	2.1	Added support for Virtex-7 and Kintex-7.

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