LogiCORE IP Video Timing Controller v2.1

DS729 September 21, 2010 **Product Specification**

Introduction

The Xilinx Video Timing Controller LogiCORE™ IP is a general purpose video timing generator and detector. The input side of this core automatically detects horizontal and vertical synchronization pulses, polarity, blanking timing and active video pixels. While on the output, it generates the horizontal and vertical blanking and synchronization pulses used with a standard video system including support for programmable pulse polarity. The core is highly programmable through a comprehensive register set allowing control of various timing generation parameters. This programmability is coupled with a comprehensive set of interrupt bits which provides easy integration with the MicroBlaze™ Soft Processor for in-system control of the block in real-time. The Video Timing Controller is provided with a General Purpose Processor register interface.

Features

- Support for video frame sizes up to 4096x4096
- Direct regeneration of output timing signals with independent timing and polarity inversion
- Automatic detection and generation of horizontal and vertical video timing signals
- Support for multiple combinations of blanking or synchronization signals
- Automatic detection of input video control signal polarities
- Programmable output video signal polarities
- Generation of up to 16 additional independent output frame synchronization signals
- Selectable processor interface
  - EDK pCore (PLBv46)
  - General Purpose Processor
- High number of interrupts and status registers for easy system control and integration

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[1]	Spartan®-3A DSP, Spartan-6LX, Spartan-6LXT, Virtex®-5, Virtex-6LX, Virtex-6LXT				
Supported User Interfaces	General Processor Interface, EDK PLB 4.6				
Supported Operating Systems	Windows XP Professional 32-Bit/64-bit, Windows Vista Business 32-Bit/64-bit, Red Hat Enterprise Linux WS v4.0 32-bit/64-bit, Red Hat Enterprise Desktop v5.0 32-bit/64-bit (with Workstation Option), SUSE Linux Enterprise (SLE) desktop and server v10.1 32-bit/64-bit				
	Resources				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Spartan-3A DSP	See Table 33		0	0	150 MHz
Spartan-6	See Table 35		0	0	150 MHz
Virtex-5	See Table 34		0	0	225 MHz
Virtex-6	See Table 36		0	0	225 MHz
Provided with Core					
Documentation	Product Specification				
Design Files	Netlist, EDK pCore				
Example Design	Not Provided				
Test Bench	Not Provided				
Constraints File	Not Provided				
Simulation Model	Not Provided				
Tested Design Tools					
Xilinx Implementation Tools	ISE® 12.3 XPS 12.3				
Simulation	ModelSim v6.5c ISE Simulator 12.3				
Synthesis Tools	ISE XST 12.3				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core.

Applications

- Video Surveillance
- Industrial Imaging
- Video Conferencing
- Machine Vision

Overview

All video systems require management of video timing signals, which are used to synchronize a variety of processes. The Video Timing Controller serves the function of both detecting and generating these timing signals.

Figure 1 shows a typical video frame including timing signals.

Note: All signals are shown with active high polarity.

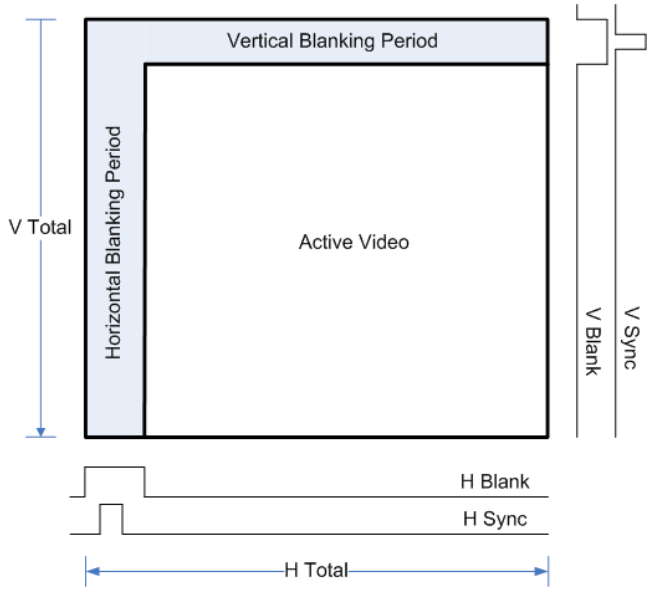

Figure 1: **Example Video Frame and Timing Signals**

A video frame can be completely described in terms of timing by only a few definitions. A video frame comprises active video and blanking periods. The vertical and horizontal synchronization signals describe the video frame timing, which includes active and blanking data. In addition, the frame synchronization signals can be used to synchronize video data from one processing block to another within a video system. There are additional signals that can also be used to control the video system, such as a signal to differentiate valid chroma samples.

Video systems may utilize different combinations of blank, synchronization or active signals with various polarities to synchronize processing and control video data. The Video Timing Controller makes this process easy by providing a highly programmable and flexible core that allows detection and generation of the various timing signals within a video system.

General Purpose Processor Interface

The General Purpose Processor Interface exposes all control and status registers as ports. These ports can easily be connected to a Host Processor via a Register File with minimal logic. An interrupt output and interrupt enable, status and clear registers are included. The ports for this interface are defined in Table 1.

Table 1: **General Purpose Processor Port Descriptions**

Name	Direction	Description
sclr	Input	SYNCHRONOUS CLEAR/RESET System synchronous reset (active high). Asserting `sclr` synchronously with `video_clk_in` resets the video timing controller internal state machines. `sclr` has priority over `ce`.
ce	Input	CLOCK ENABLE Used to halt processing and hold current values.
Detector Interface		
video_clk_in	Input	INPUT CLOCK Core clock (active high edge). Always present.
hsync_in	Input	INPUT HORIZONTAL SYNCHRONIZATION Used to set the `det_hsync_start` and the `det_hbp_start` registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. Either horizontal blank or horizontal synchronization signal inputs must be present. Both do not have to be present.
hblank_in	Input	INPUT HORIZONTAL BLANK Used to set the `det_hfp_start` and the `det_hactive_start` registers. Polarity is auto-detected. Optional. Either horizontal blank or horizontal synchronization signal inputs must be present. Both do not have to be present.
vsync_in	Input	INPUT VERTICAL SYNCHRONIZATION Used to set the `det_v0sync_start` and the `det_v0bp_start` registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. One of the following inputs must be present: active video, vertical blank or vertical synchronization.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
vblank_in	Input	INPUT VERTICAL BLANK Used to set the det_v0fp_start and the det_v0active_start registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. One of the following inputs must be present: active video, vertical blank or vertical synchronization.
field_id_in	Input	Reserved.
active_video_in	Input	INPUT ACTIVE VIDEO Used to set the det_v0fp_start and the det_v0active_start registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. One of the following inputs must be present: active video, vertical blank or vertical synchronization.
active_chroma_in	Input	INPUT ACTIVE CHROMA Used to set the det_v0achroma_start register and bit 4 in the detection status register. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional.
Generator Interface		
video_clk_out	Output	OUTPUT CLOCK Same as video_clk_in.
hsync_out	Output	OUTPUT HORIZONTAL SYNCHRONIZATION Generated horizontal synchronization signal. Polarity configured by the control register. Asserted active during the cycle set by the gen_hsync_start register and deasserted during the cycle set by the gen_hbp_start register.
hblank_out	Output	OUTPUT HORIZONTAL BLANK Generated horizontal blank signal. Polarity configured by the control register. Asserted active during the cycle set by the gen_hfp_start and deasserted during the cycle set by the gen_hactive_start register.
vsync_out	Output	OUTPUT VERTICAL SYNCHRONIZATION Generated vertical synchronization signal. Polarity configured by the control register. Asserted active during the line set by the gen_v0sync_start register and deasserted during the line set by the gen_v0bp_start register.
vblank_out	Output	OUTPUT VERTICAL BLANK Generated vertical blank signal. Polarity configured by the control register. Asserted active during the line set by the gen_v0fp_start register and deasserted during the line set by the gen_v0active_start register.
field_id_out	Output	Reserved.
active_video_out	Output	OUTPUT ACTIVE VIDEO Generated active video signal. Polarity configured by the control register. Active for non blanking lines. Asserted active during the cycle set by the gen_hactive_start register and deasserted during the cycle set by the gen_hbp_start register.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
active_chroma_out	Output	OUTPUT ACTIVE CHROMA Generated active chroma signal. Denotes which lines contain valid chroma samples (used for YUV 4:2:0). Polarity configured by the control register. Active for non blanking lines after the line set by the `gen_v0achroma_start` register (inclusive). For valid chroma lines, asserted active during every cycle the `active_video_out` signal is set per line.
Frame Synchronization Interface		
fsync *[Frame Syncs - 1:0]*	Output	FRAME SYNCHRONIZATION OUTPUT Each Frame Synchronization bit toggles for only one clock cycle during each frame. The number of bits is configured with the Frame Syncs GUI parameter. Each bit is independently configured for horizontal and vertical clock cycle position with the "fsync_hstart" and "fsync_vstart" registers).
General Purpose Processor Interface		
control[31:0]	Input	CONTROL REGISTER Bit 0: Generation Enable. When low, the generation hardware will not generate video timing output signals. When high, enable hardware to generate output. Set this bit high only after the software has configured the generator registers. Bit 1: Detection Enable. When low, no detection will be performed. All 'locked' status bits will be driven low. When high, perform timing signal detection for enabled signals. Bit 2: Generator/Detector Synchronization Enable. When low, the generator will not be synchronized to the detector. When high, the generator will be synchronized to the detector. Bit 3: Lock Interrupt Polarity. When low, the lock interrupts (see "INTERRUPT STATUS REGISTER") will trigger an interrupt on the falling edge of the internal lock signals, signifying that the detected input has changed timing. When high, the lock interrupts will trigger an interrupt on the rising edge of the internal lock signals, signifying that a lock has been achieved on the detected input. Bit 4: Generated Active Chroma Skip. This is the number of lines to skip between each successive active chroma line. Low denotes not to skip lines. Used for YUV 4:2:2 or 4:4:4. High denotes to skip every other line. Used for 4:2:0.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
control[31:0] *(continued from previous page)*	Input	Bits 7-5: RESERVED Source Selects. Bits 8-18 select which register controls the generator outputs. Low denotes the detection register will be used. High denotes that the generation register will be used. These bits allow the video timing controller detector to control the generator outputs (when low) or allow the host processor to override each value independently (when high). Bit 8: Horizontal Total Register Source Select Bit 9: Horizontal Front Porch Start Register Source Select Bit 10: Horizontal Synchronization Start Register Source Select Bit 11: Horizontal Back Porch Start Register Source Select Bit 12: Horizontal Active Video Start Register Source Select Bit 13: Vertical Total Register Source Select Bit 14: Vertical Front Porch Start Register Source Select Bit 15: Vertical Synchronization Start Register Source Select Bit 16: Vertical Back Porch Start Register Source Select Bit 17: Vertical Active Video Start Register Source Select Bit 18: Start of Active Chroma Register Source Select Bit 19: RESERVED Generated Output Signal Polarities. Bits 20-26 configure the polarity of each output. High denotes active high polarity. Low denotes active low polarity. Bit 20: Horizontal Synchronization Output Polarity Bit 21: Horizontal Blank Output Polarity Bit 22: Vertical Synchronization Output Polarity Bit 23: Vertical Blank Output Polarity Bit 24: Field ID Output Polarity Bit 25: Active Video Output Polarity Bit 26: Active Chroma Output Polarity Bits 27-31: RESERVED

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
det_status[31:0]	Output	DETECTION STATUS REGISTER Bits 0-3: RESERVED Bit 4: Detected Active Chroma Skip. This is the number of lines skipped between each successive active chroma line. Low denotes no lines are skipped. Used for detecting YUV 4:2:2 or 4:4:4. High denotes every other line is skipped. Used for detecting YUV 4:2:0. Bits 5-19: RESERVED Detected Input Signal Polarities. Bits 20-26 denote the polarity of each input. High denotes active high polarity. Low denotes active low polarity. Bit 20: Horizontal Synchronization Input Polarity Bit 21: Horizontal Blank input Polarity Bit 22: Vertical Synchronization Input Polarity Bit 23: Vertical Blank Input Polarity Bit 24: Field ID Input Polarity Bit 25: Active Video Input Polarity Bit 26: Active Chroma Input Polarity Bits 27-31: RESERVED
gen_htotal[X_{b2}-1:0]	Input	GENERATED HORIZONTAL TOTAL Total number of horizontal clock cycles (minus 1) per line including blanking and active cycles. This is the last pixel count on each line. Each line starts at count 0. Maximum allowable Horizontal Total is configured by the *MAX CLOCKS PER LINE* parameter.
gen_hfp_start[X_{b2}-1:0]	Input	GENERATED HORIZONTAL FRONT PORCH START Cycle count during which the Horizontal Front Porch starts. Also denotes the end of Active Video.
gen_hsync_start[X_{b2}-1:0]	Input	GENERATED HORIZONTAL SYNCHRONIZATION START Cycle count during which the Horizontal Synchronization starts. Also denotes the end of Horizontal Front Porch.
gen_hbp_start[X_{b2}-1:0]	Input	GENERATED HORIZONTAL BACK PORCH START Cycle count during which the Horizontal Back Porch starts. Also denotes the end of Horizontal Synchronization.
gen_hactive_start[X_{b2}-1:0]	Input	GENERATED HORIZONTAL ACTIVE VIDEO START Cycle count during which the Horizontal Active Video starts. Also denotes the end of Horizontal Back Porch.
gen_v0total[Y_{b2}-1:0]	Input	GENERATED VERTICAL TOTAL LINES Total number of Vertical lines per frame (minus 1) including blanking and active cycles. This is the last line count in each frame. Each frame starts at line count 0. Maximum allowable Vertical Total is configured by the *MAX LINES PER FRAME* parameter.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
gen_v0fp_start[Y_{b2}-1:0]	Input	GENERATED VERTICAL FRONT PORCH START Line count during which the Vertical Front Porch starts. Also denotes the end of Active Video.
gen_v0sync_start[Y_{b2}-1:0]	Input	GENERATED VERTICAL SYNCHRONIZATION START Line count during which the Vertical Synchronization starts. Also denotes the end of Vertical Front Porch.
gen_v0bp_start[Y_{b2}-1:0]	Input	GENERATED VERTICAL BACK PORCH START Line count during which the Vertical Back Porch starts. Also denotes the end of Vertical Synchronization.
gen_v0active_start[Yb2-1:0]	Input	GENERATED VERTICAL ACTIVE VIDEO START Line count during which the Active Video starts. Also denotes the end of Vertical Back Porch.
gen_v0achroma_start [Y_{b2}-1:0]	Input	GENERATED ACTIVE CHROMA START Line count during which the Active Chroma starts. See bit 4 of the control register to configure for YUV 4:2:0 mode.
det_htotal[X_{b2}-1:0]	Output	DETECTED HORIZONTAL TOTAL Detected Total number of horizontal clock cycles per line including blanking and active cycles (minus 1). Maximum allowable horizontal Total is configured by the *MAX CLOCKS PER LINE* parameter.
det_hfp_start[X_{b2}-1:0]	Output	DETECTED HORIZONTAL FRONT PORCH START Detected cycle count during which the Input Horizontal Front Porch starts. Also denotes the end of Input Active Video.
det_hsync_start[X_{b2}-1:0]	Output	DETECTED HORIZONTAL SYNCHRONIZATION START Detected Cycle count during which the Input Horizontal Synchronization starts. Also denotes the end of Input Horizontal Front Porch.
det_hbp_start[X_{b2}-1:0]	Output	DETECTED HORIZONTAL BACK PORCH START Detected Cycle count during which the Input Horizontal Back Porch starts. Also denotes the end of Input Horizontal Synchronization.
det_hactive_start[X_{b2}-1:0]	Output	DETECTED HORIZONTAL ACTIVE VIDEO START Cycle count during which the Input Horizontal Active Video starts. Also denotes the end of Input Horizontal Back Porch.
det_v0total[Y_{b2}-1:0]	Output	DETECTED VERTICAL TOTAL Total number of Input Vertical lines per frame including blanking and active cycles (minus 1). Maximum allowable Vertical Total is configured by the *MAX LINES PER FRAME* parameter.
det_v0fp_start[Y_{b2}-1:0]	Output	DETECTED VERTICAL FRONT PORCH START Line count during which the Input Vertical Front Porch starts. Also denotes the end of Input Active Video.
det_v0sync_start[Y_{b2}-1:0]	Output	DETECTED VERTICAL SYNCHRONIZATION START Line count during which the Input Vertical Synchronization starts. Also denotes the end of Input Vertical Front Porch.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
det_v0bp_start[Y_{b2}-1:0]	Output	DETECTED VERTICAL BACK PORCH START Line count during which the Input Vertical Back Porch starts. Also denotes the end of Input Vertical Synchronization.
det_v0active_start[Yb2-1:0]	Output	DETECTED VERTICAL ACTIVE VIDEO START Line count during which the Input Vertical Active Video starts. Also denotes the end of Input Vertical Back Porch.
det_v0achroma_start [Y_{b2}-1:0]	Output	DETECTED ACTIVE CHROMA START Line count during which the Input Active Chroma starts.
fsync_hstart [Frame Syncs*X_{b2}-1:0]	Input	FRAME SYNCHRONIZATION HORIZONTAL START REGISTER Bits Y_{b2}-1 to 0: Horizontal Cycle during which Frame Synchronization 0 is active. Bits $2X_{b2}$-1 to X_{b2}: Horizontal Cycle during which Frame Synchronization 1 is active.
fsync_vstart [Frame Syncs*Y_{b2}-1:0]	Input	FRAME SYNCHRONIZATION VERTICAL START REGISTER Bits Y_{b2}-1 to 0: Vertical line during which Frame Synchronization 0 is active. Bits $2Y_{b2}$-1 to Y_{b2}: Vertical line during which Frame Synchronization 1 is active. ***Note:*** Frame Syncs are not active during the complete line, only in the cycle during which both the `fsync_vstart` and `fsync_hstart` are valid each frame.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
intr_status[31:0]	Output	INTERRUPT STATUS REGISTER Bit 0: Horizontal Synchronization Lock Status. When the lock polarity is low (see "CONTROL REGISTER", bit 3), set high when the horizontal synchronization timing has changed, signifying a signal lock has been lost. When the lock polarity is high, set high when the horizontal synchronization timing remains unchanged, signifying a signal lock. Bit 1: Horizontal Blank Lock Status. Set high when the horizontal blank timing has changed and the lock polarity is low. Set high when the horizontal blank timing remains unchanged and the lock polarity is high. Bit 2: Vertical Synchronization Lock Status. Set high when the vertical synchronization timing has changed and the lock polarity is low. Set high when the vertical synchronization timing remains unchanged and the lock polarity is high. Bit 3: Vertical Blank Lock Status. Set high when the vertical blank timing has changed and the lock polarity is low. Set high when the vertical blank timing remains unchanged and the lock polarity is high. Bit 4: Reserved. Bit 5: Active Video Lock Status. Set high when the active video timing has changed and the lock polarity is low. Set high when the active video timing remains unchanged and the lock polarity is high. Bit 6: Active Chroma Lock Status. Set high when the active chroma timing has changed and the lock polarity is low. Set high when the active chroma timing remains unchanged and the lock polarity is high. Bit 7: All Lock Status. Set high when bits 0-6 of the interrupt status register are high. When the lock polarity is high, a high on bit 7 indicates that all signals have been locked. When the lock polarity is low, a high on bit 7 indicates that all signal timing have changed. Bit 8: Detected Vertical Blank Interrupt Status. Set high during the first cycle the input vertical blank is asserted active after lock. Bit 9: Detected Active Video Interrupt. Set high during the first cycle the input active video is asserted active after lock. Bits 11-10: Reserved. Bit 12: Generated Vertical Blank Interrupt Status. Set high during the first cycle the output vertical blank is asserted. Bit 13: Generated Active Video Interrupt. Set high during the first cycle the output active video is asserted. Bits 15-14: Reserved. Bits 31-16: Frame Synchronization Interrupt Status. Bits 31-16 are set high when frame syncs 15-0 are set respectively.

Table 1: **General Purpose Processor Port Descriptions *(Cont'd)***

Name	Direction	Description
intr_enable[31:0]	Input	INTERRUPT ENABLE REGISTER Same bit definitions as in the interrupt status register. Setting a bit high in the interrupt enable register enables the corresponding interrupt. Bits that are low mask the corresponding interrupt from triggering a host interrupt.
intr_clr[31:0]	Input	INTERRUPT CLEAR REGISTER Same bit definitions as in the interrupt status register. Setting a bit high in the interrupt clear register clears the corresponding bit in the interrupt status register. Bits in the interrupt status register are cleared only on the rising edge of the corresponding bits in the interrupt clear register. Therefore, each bit in the interrupt clear register must be driven low before being driven high to clear the status register bits.
intr_out	Output	HOST INTERRUPT Active high host interrupt output. This output is set active high when an interrupt occurs (an enabled bit in the status register is high) and cleared to low when all enabled status bits in the `intr_status` register have been cleared by writing to the `intr_clr` register.

Notes:

1. X_{b2} is the $\log_2$(*Max Clocks per Line*) GUI parameter. Y_{b2} is the $\log_2$(*Max Lines per Frame*) GUI parameter.
2. All registers are little-endian.

Dynamic Register Interface

There are 16 dynamic inputs as listed in Table 1 (see "General Purpose Processor Interface"). They may be driven by the user as desired. New values take effect immediately. It is recommended to disable Video Timing Generation (see "CONTROL REGISTER" bit 0) while updating these inputs.

EDK pCore (PLB) Interface

The Xilinx Video Timing controller, when configured as an EDK pCore, uses the Processor Local Bus to interface to a microprocessor. See the Processor Local Bus (PLB) v4.6 Data Sheet for more information on the PLB interface signals.

When the developer selects the EDK pCore interface, the Xilinx CORE Generator™ software creates a pCore and all support files that can be added to an EDK project as a hardware peripheral. This pCore provides a memory-mapped interface for the programmable registers within the core and a complete device driver to enable rapid application development.

Xilinx CORE Generator software will place all EDK pCore source files in the "pcores" subdirectory located in the core output directory. The core output directory is given the same name as the component. For example, if the component name is set to "v_timebase_v2_1_u0," then the EDK pCore source files will be located in the following directory:

```
<coregen project directory>/v_timebase_v2_1_u0/pcores/timebase_v2_01_a
```

The pCore should be copied to the user's <EDK_Project>/pcores directory or to a user pCores repository.

EDK pCore Port Descriptions

Table 2 shows the I/O signals on the Xilinx Video Timing Controller when the core is configured with an EDK pCore Interface. The PLB v4.6 signals are specified in Table 4.

Table 2: **EDK pCore Port Descriptions**

Name	Direction	Description
ce	Input	CLOCK ENABLE Used to halt processing and hold current values.
Detector Interface		
video_clk_in	Input	INPUT CLOCK Core clock (active high edge). Always present.
timebase_hsync_i	Input	INPUT HORIZONTAL SYNCHRONIZATION Used to set the `det_hsync_start` and the `det_hbp_start` registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. Either horizontal blank or horizontal synchronization signal inputs must be present. Both do not have to be present.
timebase_hblank_i	Input	INPUT HORIZONTAL BLANK Used to set the `det_hfp_start` and the `det_hactive_start` registers. Polarity is auto-detected. Optional. Either horizontal blank or horizontal synchronization signal inputs must be present. Both do not have to be present.
timebase_vsync_i	Input	INPUT VERTICAL SYNCHRONIZATION Used to set the `det_v0sync_start` and the `det_v0bp_start` registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. One of the following inputs must be present: active video, vertical blank or vertical synchronization.
timebase_vblank_i	Input	INPUT VERTICAL BLANK Used to set the `det_v0fp_start` and the `det_v0active_start` registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. One of the following inputs must be present: active video, vertical blank or vertical synchronization.
timebase_field_id_i	Input	Reserved.
timebase_active_video_i	Input	INPUT ACTIVE VIDEO Used to set the `det_v0fp_start` and the `det_v0active_start` registers. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional. One of the following inputs must be present: active video, vertical blank or vertical synchronization.
timebase_active_chroma_i	Input	INPUT ACTIVE CHROMA Used to set the `det_v0achroma_start` register and bit 4 in the detection status register. Polarity is auto-detected (see "DETECTION STATUS REGISTER"). Optional.

Table 2: **EDK pCore Port Descriptions *(Cont'd)***

Name	Direction	Description
Generator Interface		
timebase_video_clk_o	Output	OUTPUT CLOCK Same as `video_clk_in`.
timebase_hsync_o	Output	OUTPUT HORIZONTAL SYNCHRONIZATION Generated horizontal synchronization signal. Polarity configured by the control register. Asserted active during the cycle set by the `gen_hsync_start` register and deasserted during the cycle set by the `gen_hbp_start` register.
timebase_hblank_o	Output	OUTPUT HORIZONTAL BLANK Generated horizontal blank signal. Polarity configured by the control register. Asserted active during the cycle set by the `gen_hfp_start` and deasserted during the cycle set by the `gen_hactive_start` register.
timebase_vsync_o	Output	OUTPUT VERTICAL SYNCHRONIZATION Generated vertical synchronization signal. Polarity configured by the control register. Asserted active during the line set by the `gen_v0sync_start` register and deasserted during the line set by the `gen_v0bp_start` register.
timebase_vblank_o	Output	OUTPUT VERTICAL BLANK Generated vertical blank signal. Polarity configured by the control register. Asserted active during the line set by the `gen_v0fp_start` register and deasserted during the line set by the `gen_v0active_start` register.
timebase_field_id_o	Output	Reserved.
timebase_active_video_o	Output	OUTPUT ACTIVE VIDEO Generated active video signal. Polarity configured by the control register. Active for non blanking lines. Asserted active during the cycle set by the `gen_hactive_start` register and deasserted during the cycle set by the `gen_hbp_start` register.
timebase_active_chroma_o	Output	OUTPUT ACTIVE CHROMA Generated active chroma signal. Denotes which lines contain valid chroma samples (used for YUV 4:2:0). Polarity configured by the control register. Active for non blanking lines after the line set by the `gen_v0achroma_start` register (inclusive). For valid chroma lines, asserted active during every cycle the `active_video_out` signal is set per line.
Frame Synchronization Interface		
fsync_o *[Frame Syncs - 1:0]*	Output	FRAME SYNCHRONIZATION OUTPUT Each Frame Synchronization bit toggles for only one clock cycle during each frame. The number of bits is configured with the Frame Syncs GUI parameter. Each bit is independently configured for horizontal and vertical clock cycle position with the "fsync_hstart" and "fsync_vstart" registers).

Table 3: **Processor Local Bus (PLB) v4.6 Signals**

Name	Direction	Description
SPLB_Clk	Input	Slave PLB Clock
SPLB_Rst	Input	Slave PLB Reset
PLB_ABus [0:C_SPLB_AWIDTH-1]	Input	PLB address bus
PLB_PAValid	Input	PLB primary address valid indicator
PLB_masterID[0:C_SPLB_MID_WIDTH-1]	Input	PLB current master identifier
PLB_abort	Input	PLB abort bus request indicator
PLB_RNW	Input	PLB read not write
PLB_BE [0:(C_SPLB_DWIDTH/8)-1]	Input	PLB byte enables
PLB_MSize [0:1]	Input	PLB master data bus size
PLB_size [0:3]	Input	PLB transfer size
PLB_type [0:2]	Input	PLB transfer type
PLB_wrDBus [0:C_SPLB_DWIDTH-1]	Input	PLB write data bus
PLB_wrBurst	Input	PLB burst write transfer indicator
PLB_rdBurst	Input	PLB burst read transfer indicator
PLB_SAValid	Input	PLB Secondary address valid
PLB_UABus[0:31]	Input	PLB Upper address bus
PLB_BusLock	Input	PLB Bus Lock
PLB_LockErr	Input	PLB Lock Error
PLB_TAttribute[0:15]	Input	PLB Attribute
PLB_RdPrim	Input	PLB Read Primary
PLB_WrPrim	Input	PLB Write Primary
PLB_RDPendPri[0:1]	Input	PLB Read Pending on Primary
PLB_WrPendPri[0:1]	Input	PLB Write Pending on Primary
PLB_RdPendReq	Input	PLB Read Pending Request
PLB_WrPendReq	Input	PLB Write Pending Request
Sl_addAck	Output	Slave address acknowledge
Sl_SSize[0:1]	Output	Slave data bus size
Sl_wait	Output	Slave wait indicator
Sl_rearbitrate	Output	Slave rearbitrate bus indicator
Sl_wrDAck	Output	Slave write data acknowledge
Sl_wrComp	Output	Slave write transfer complete indicator
Sl_wrBTerm	Output	Slave terminate write burst transfer
Sl_rdDBus[0:C_SPLB_DWIDTH-1]	Output	Slave read data bus
Sl_rdWdAddr[0:3]	Output	Slave read word address
Sl_rdDAck	Output	Slave read data acknowledge
Sl_rdComp	Output	Slave read transfer complete indicator
Sl_rdBTerm	Output	Slave terminate read burst transfer

Table 3: **Processor Local Bus (PLB) v4.6 Signals**

Name	Direction	Description
Sl_MBusy[0:C_SPLB_NUM_MASTERS-1]	Output	Slave busy indicator
Sl_MrdErr[0:C_SPLB_NUM_MASTERS-1]	Output	Slave read error indicator
Sl_MwrErr[0:C_SPLB_NUM_MASTERS-1]	Output	Slave write error indicator
Sl_MIRQ[0:C_SPLB_NUM_MASTERS-1]	Output	Slave Interrupt
IP2INTC_Irpt	Output	Interrupt signal

EDK pCore Register Set

The EDK pCore Interface provides a memory mapped interface for all programmable registers within the core. All registers default to 0x00000000 on Power-on/Reset unless otherwise noted.

Table 4: **EDK pCore Address Map**

Address Offset	Name	Read/Write	Description
0x0000	Control	R/W	General control register
0x0004	Generator Horizontal 0	R/W	Horizontal total and front porch
0x0008	Generator Horizontal 1	R/W	Horizontal sync and back porch
0x000c	Generator Horizontal 2	R/W	Horizontal Active Video
0x0010	Generator Vertical 0	R/W	Vertical total and front porch
0x0014	Generator Vertical 1	R/W	Vertical sync and back porch
0x0018	Generator Vertical 2	R/W	Vertical Active Video and Active Chroma
0x001C	Reserved	-	Reserved
0x0020	Reserved	-	Reserved
0x0024	Reserved	-	Reserved
0x0028	Detector Status	R	Detector polarities and chroma format status
0x002c	Detector Horizontal 0	R	Horizontal total and front porch (detected)
0x0030	Detector Horizontal 1	R	Horizontal sync and back porch (detected)
0x0034	Detector Horizontal 2	R	Horizontal Active Video (detected)
0x0038	Detector Vertical 0	R	Vertical total and front porch (detected)
0x003c	Detector Vertical 1	R	Vertical sync and back porch (detected)
0x0040	Detector Vertical 2	R	Vertical Active Video and Active Chroma (detected)
0x0044	Reserved	-	Reserved
0x0048	Reserved	-	Reserved
0x004c	Reserved	-	Reserved
0x0050 … 0x008c	Frame Sync 0 - 15 Config	R/W	Horizontal start clock and vertical start line of Frame Sync 0 - 15
0x0090 … 0x009c	Reserved	-	Reserved
0x00f0	Version Registers	R	Core Hardware Version

Table 4: **EDK pCore Address Map *(Cont'd)***

0x0100	Software Reset	R/W	Resets pCore when written with 0xa000_0000
0x021c	GIER	R/W	Global Interrupt Enable Register
0x0220	ISR	R/W	Interrupt Status/Clear Register
0x0228	IER	R/W	Interrupt Enable Register

Note: The registers of the EDK pCore Interface are big-endian. The registers of the General Purpose Processor Interface are little-endian.

Table 5: **Control Register (Address Offset 0x0000)**

0x0000	**Control Register**	**R/W**
Name	**Bits**	**Description**
Reserved	27:31	Reserved
Active_Chroma_pol(1)	26	Active Chroma Output Polarity
Active_Video_pol(1)	25	Active Video Output Polarity
Field_id_pol(1)	24	Field ID Output Polarity
Vblank_pol(1)	23	Vertical Blank Output Polarity
Vsync_pol(1)	22	Vertical Synchronization Output Polarity
Hblank_pol(1)	21	Horizontal Blank Output Polarity
Hsync_pol(1)	20	Horizontal Synchronization Output Polarity
Reserved	19	Reserved
Vchroma_src_sel(2)	18	Start of Active Chroma Register Source Select 1: Select Host CPU register as the start of Active Chroma 0: Select the Timebase Detect register as the start of Active Chroma.
Vactive_src_sel(2)	17	Vertical Active Video Start Register Source Select
Vbp_src_sel(2)	16	Vertical Back Porch Start Register Source Select
Vsync_src_sel(2)	15	Vertical Synchronization Start Register Source Select
Vfp_src_sel(2)	14	Vertical Front Porch Start Register Source Select
Vtotal_src_sel(2)	13	Vertical Total Register Source Select
Hactive_src_sel(2)	12	Horizontal Active Video Start Register Source Select
Hbp_src_sel(2)	11	Horizontal Back Porch Start Register Source Select
Hsync_src_sel(2)	10	Horizontal Synchronization Start Register Source Select
Hfp_src_sel(2)	9	Horizontal Front Porch Start Register Source Select
Htotal_src_sel	8	Horizontal Total Register Source Select
Reserved	5:7	Reserved
Gen_achroma_skip	4	Generated Active Chroma Skip. This is the number of lines to skip between each successive active chroma line. Low denotes not to skip lines. Used for YUV 4:2:2 or 4:4:4. High denotes to skip every other line. Used for 4:2:0.
Reserved	3	Reserved

Table 5: **Control Register (Address Offset 0x0000) *(Cont'd) (Cont'd)***

Sync_en	2	Generator/Detector Synchronization Enable. When low, the generator will not be synchronized to the detector. When high, the generator will be synchronized to the detector.
Det_en	1	Detection Enable. When low, no detection will be performed. All 'locked' status bits will be driven low. When high, perform timing signal detection for enabled signals.
Gen_en	0	Generation Enable. When low, the generation hardware will not generate video timing output signals. When high, enable hardware to generate output. Set this bit high only after the software has configured the generator registers.

1. Bits 20-26 configure the polarity of each output. High denotes active high polarity. Low denotes active low polarity.
2. Bits 8-18 select which register controls the generator outputs. Low denotes the detection register will be used. High denotes that the generation register will be used. These bits allow the video timing controller detector to control the generator outputs (when low) or allow the host processor to override each value independently (when high).

Table 6: **Generator Horizontal 0 Register (Address Offset 0x0004)**

0x0004	**Generator Horizontal 0**	**R/W**
Name	**Bits**	**Description**
Reserved	28:31	Reserved
HFP_start	16:27	GENERATED HORIZONTAL FRONT PORCH START Cycle count during which the Horizontal Front Porch starts. Also denotes the end of Active Video.
Reserved	12:15	Reserved
HTotal	0:11	GENERATED HORIZONTAL TOTAL Total number of horizontal clock cycles (minus 1) per line including blanking and active cycles. This is the last pixel count on each line. Each line starts at count 0. Maximum allowable Horizontal Total is configured by the *MAX CLOCKS PER LINE* parameter.

Table 7: **Generator Horizontal 1 Register (Address Offset 0x0008)**

0x0008	**Generator Horizontal 1**	**R/W**
Name	**Bits**	**Description**
Reserved	28:31	Reserved
HBP_start	16:27	GENERATED HORIZONTAL BACK PORCH START Cycle count during which the Horizontal Back Porch starts. Also denotes the end of Horizontal Synchronization.
Reserved	12:15	Reserved
HSync_start	0:11	GENERATED HORIZONTAL SYNCHRONIZATION START Cycle count during which the Horizontal Synchronization starts. Also denotes the end of Horizontal Front Porch.

Table 8: **Generator Horizontal 2 Register (Address Offset 0x000C)**

0x000C	Generator Horizontal 2	R/W
Name	**Bits**	**Description**
Reserved	12:32	Reserved
HActive_start	0:11	GENERATED HORIZONTAL ACTIVE VIDEO START Cycle count during which the Horizontal Active Video starts. Also denotes the end of Horizontal Back Porch.

Table 9: **Generator Vertical 0 Register (Address Offset 0x0010)**

0x0010	Generator Vertical 0	R/W
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V0FP_start	16:27	GENERATED VERTICAL FRONT PORCH START Line count during which the Vertical Front Porch starts. Also denotes the end of Active Video.
Reserved	12:15	Reserved
V0Total	0:11	GENERATED VERTICAL TOTAL LINES Total number of Vertical lines per frame (minus 1) including blanking and active cycles. This is the last line count in each frame. Each frame starts at line count 0. Maximum allowable Vertical Total is configured by the *MAX LINES PER FRAME* parameter.

Table 10: **Generator Vertical 1 Register (Address Offset 0x0014)**

0x0014	Generator Vertical 1	R/W
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V0BP_start	16:27	GENERATED VERTICAL BACK PORCH START Line count during which the Vertical Back Porch starts. Also denotes the end of Vertical Synchronization.
Reserved	12:15	Reserved
V0Sync_start	0:11	GENERATED VERTICAL SYNCHRONIZATION START Line count during which the Vertical Synchronization starts. Also denotes the end of Vertical Front Porch.

Table 11: **Generator Vertical 2 Register (Address Offset 0x0018)**

0x0018	Generator Vertical 2	R/W
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V0chroma_start	16:27	GENERATED ACTIVE CHROMA START Line count during which the Active Chroma starts. See bit 4 of the control register to configure for YUV 4:2:0 mode.
Reserved	12:15	Reserved
V0active_start	0:11	GENERATED VERTICAL ACTIVE VIDEO START Line count during which the Active Video starts. Also denotes the end of Vertical Back Porch.

Table 12: **Detector Status Register (Address Offset 0x0028)**

0x0028	Detector Status	R
Name	**Bits**	**Description**
Reserved	27:31	Reserved
Active_Chroma_pol	26	Active Chroma Input Polarity
Active_Video_pol	25	Active Video Input Polarity
Field_id_pol	24	Field ID Input Polarity
Vblank_pol	23	Vertical Blank Input Polarity
Vsync_pol	22	Vertical Synchronization Input Polarity
Hblank_pol	21	Horizontal Blank Input Polarity
Hsync_pol	20	Horizontal Synchronization Input Polarity
Reserved	5:19	Reserved
Det_achroma_skip	4	Detected Active Chroma Skip. This is the number of lines skipped between each successive active chroma line. Low denotes no lines are skipped. Used for detecting YUV 4:2:2 or 4:4:4. High denotes every other line is skipped. Used for detecting YUV 4:2:0.
Reserved	0:3	Reserved

Note: Bits 20-26 denote the polarity of each input. High denotes active high polarity. Low denotes active low polarity.

Table 13: **Detector Horizontal 0 Register (Address Offset 0x002C)**

0x002C	Detector Horizontal 0	R
Name	**Bits**	**Description**
Reserved	28:31	Reserved
HFP_start	16:27	DETECTED HORIZONTAL FRONT PORCH START Detected cycle count during which the Input Horizontal Front Porch starts. Also denotes the end of Input Active Video.
Reserved	12:15	Reserved
HTotal	0:11	DETECTED HORIZONTAL TOTAL Detected Total number of horizontal clock cycles per line including blanking and active cycles (minus 1). Maximum allowable horizontal Total is configured by the *MAX CLOCKS PER LINE* parameter.

Table 14: **Detector Horizontal 1 Register (Address Offset 0x0030)**

0x0030	Detector Horizontal 1	R
Name	**Bits**	**Description**
Reserved	28:31	Reserved
HBP_start	16:27	DETECTED HORIZONTAL BACK PORCH START Detected Cycle count during which the Input Horizontal Back Porch starts. Also denotes the end of Input Horizontal Synchronization.
Reserved	12:15	Reserved
HSync_start	0:11	DETECTED HORIZONTAL SYNCHRONIZATION START Detected Cycle count during which the Input Horizontal Synchronization starts. Also denotes the end of Input Horizontal Front Porch.

Table 15: **Detector Horizontal 2 Register (Address Offset 0x0034)**

0x0034	Detector Horizontal 2	R
Name	**Bits**	**Description**
Reserved	12:31	Reserved
HActive_start	0:11	DETECTED HORIZONTAL ACTIVE VIDEO START Cycle count during which the Input Horizontal Active Video starts. Also denotes the end of Input Horizontal Back Porch.

Table 16: **Detector Vertical 0 Register (Address Offset 0x0038)**

0x0038	Detector Vertical 0	R
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V0FP_start	16:27	DETECTED VERTICAL FRONT PORCH START Line count during which the Input Vertical Front Porch starts. Also denotes the end of Input Active Video.
Reserved	12:15	Reserved
V0Total	0:11	DETECTED VERTICAL TOTAL Total number of Input Vertical lines per frame including blanking and active cycles (minus 1). Maximum allowable Vertical Total is configured by the *MAX LINES PER FRAME* parameter.

Table 17: **Detector Vertical 1 Register (Address Offset 0x003C)**

0x003C	Detector Vertical 1	R
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V0BP_start	16:27	DETECTED VERTICAL BACK PORCH START Line count during which the Input Vertical Back Porch starts. Also denotes the end of Input Vertical Synchronization
Reserved	12:15	Reserved
V0Sync_start	0:11	DETECTED VERTICAL SYNCHRONIZATION START Line count during which the Input Vertical Synchronization starts. Also denotes the end of Input Vertical Front Porch.

Table 18: **Detector Vertical 2 Register (Address Offset 0x0040)**

0x0040	Detector Vertical 2	R
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V0chroma_start	16:27	DETECTED ACTIVE CHROMA START Line count during which the Input Active Chroma starts.
Reserved	12:15	Reserved
V0active_start	0:11	DETECTED VERTICAL ACTIVE VIDEO START Line count during which the Input Vertical Active Video starts. Also denotes the end of Input Vertical Back Porch.

Table 19: **Frame Sync 0 Register (Address Offset 0x0050)**

0x0050	Frame Sync 0	R/W
Name	**Bits**	**Description**
Reserved	28:31	Reserved
V_start	16:27	FRAME SYNCHRONIZATION VERTICAL START REGISTER Vertical line during which Frame Synchronization 0 is active. ***Note:*** Frame Syncs are not active during the complete line, only in the cycle during which both the `fsync_vstart` and `fsync_hstart` are valid each frame.
Reserved	12:15	Reserved
H_start	0:11	FRAME SYNCHRONIZATION HORIZONTAL START REGISTER Horizontal Cycle during which Frame Synchronization 0 is active.

Note: Frame Sync 1-15 Registers (address offset 0x54 - 0x8c) have the same format as the Frame Sync 0 Register.

Table 20: **Version Register (Address Offset 0x00F0)**

0x00F0	Version Register	R
Name	**Bits**	**Description**
Major Version	28:31	Major Version Number. Set to 0x2.
Minor Version	20:27	Minor Version Number. Set to 0x01.
Revision	16:19	Revision Number. Set to 0XA.
Reserved	0:15	Reserved

Table 21: **Software Reset Register (Address Offset 0x0100)**

0x0100	Software Reset	R/W
Name	**Bits**	**Description**
Soft_Reset_Value	0:31	Soft Reset to reset the registers and IP Core, data Value provided by the EDK create peripheral utility. (0xa000_0000)

Table 22: **Global Interrupt Enable Register (Address Offset 0x021c)**

0x00F0	Version Register	R/W
Name	**Bits**	**Description**
GIER	31	Global Interrupt Enable. Writing a 1 to this bit will enable all interrupts. Set to 0 (all interrupts disabled) by default.
Reserved	0:30	Reserved

Table 23: **ISR (Interrupt Status/Clear) Register (Address Offset 0x0220)**

0x0220	ISR - Interrupt Status/Clear	R/W
Name	**Bits**	**Description**
Fsync	16:31	Frame Synchronization Interrupt Status. Bits 16-31 are set high when frame syncs 0-15 are set respectively.
Reserved	14:15	Reserved
Gen_active_video	13	Generated Active Video Interrupt. Set high during the first cycle the output active video is asserted.
Gen_blank	12	Generated Vertical Blank Interrupt Status. Set high during the first cycle the output vertical blank is asserted.
Reserved	10:11	Reserved
Det_active_video	9	Detected Active Video Interrupt. Set high during the first cycle the input active video is asserted active after lock.
Det_vblank	8	Detected Vertical Blank Interrupt Status. Set high during the first cycle the input vertical blank is asserted active after lock.
All_lock	7	All Lock Status. Set High when bits 0-6 are high, signifying that all enabled detection signals have locked. Signals that have detection disabled will not affect this bit.
Active_chroma_lock	6	Active Chroma Lock Status. Set high when the active chroma timing has changed and the lock polarity is low. Set high when the active chroma timing remains unchanged and the lock polarity is high.
Active_video_lock	5	Active Video Lock Status. Set high when the active video timing has changed and the lock polarity is low. Set high when the active video timing remains unchanged and the lock polarity is high.
Reserved	4	Reserved
Vblank_lock	3	Vertical Blank Lock Status. Set high when the vertical blank timing has changed and the lock polarity is low. Set high when the vertical blank timing remains unchanged and the lock polarity is high.
Vsync_lock	2	Vertical Synchronization Lock Status. Set high when the vertical synchronization timing has changed and the lock polarity is low. Set high when the vertical synchronization timing remains unchanged and the lock polarity is high.
Hblank_lock	1	Horizontal Blank Lock Status. Set high when the horizontal blank timing has changed and the lock polarity is low. Set high when the horizontal blank timing remains unchanged and the lock polarity is high.
Hsync_lock	0	Horizontal Synchronization Lock Status. When the lock polarity is low (see "CONTROL REGISTER", bit 3), set high when the horizontal synchronization timing has changed, signifying a signal lock has been lost. When the lock polarity is high, set high when the horizontal synchronization timing remains unchanged, signifying a signal lock.

Note: Setting a bit high in the ISR will clear the corresponding interrupt.

Table 24: **IER (Interrupt Enable) Register (Address Offset 0x0228)**

0x0228	IER - Interrupt Enable	R/W
Name	**Bits**	**Description**
Fsync	16:31	Frame Synchronization Interrupt Enable.
Reserved	14:15	Reserved
Gen_active_video	13	Generated Active Video Interrupt Enable.
Gen_blank	12	Generated Vertical Blank Interrupt Enable.
Reserved	10:11	Reserved
Det_active_video	9	Detected Active Video Interrupt Enable.
Det_vblank	8	Detected Vertical Blank Interrupt Enable.
All_lock	7	All Lock Enable.
Active_chroma_lock	6	Active Chroma Lock Enable.
Active_video_lock	5	Active Video Lock Enable.
Reserved	4	Reserved
Vblank_lock	3	Vertical Blank Lock Enable.
Vsync_lock	2	Vertical Synchronization Lock Enable.
Hblank_lock	1	Horizontal Blank Lock Enable.
Hsync_lock	0	Horizontal Synchronization Lock Enable.

Note: Setting a bit high in the interrupt enable register enables the corresponding interrupt. Bits that are low mask the corresponding interrupt from triggering a host interrupt.

pCore Device Driver

The Xilinx Video Timing Controller pCore includes a software driver written in the C Language that the user can use to control the Xilinx Video Timing Controller devices. A high-level API is provided and can be used without detailed knowledge of the Xilinx Video Timing Controller devices. Application developers are encouraged to use this API to access the device features. A low-level API is also provided in case applications prefer to access the devices directly through the system registers described in the previous section.

Table 25 lists the files that are included with the Xilinx Video Timing Controller pCore driver and their description.

Table 25: **Device Driver Source Files**

File Name	Description
xtimebase.h	Contains all prototypes of high-level API to access all of the features of the Xilinx Video Timing Controller devices.
xtimebase.c	Contains the implementation of high-level API to access all of the features of the Xilinx Video Timing Controller devices except interrupts.
xtimebase_intr.c	Contains the implementation of high-level API to access interrupt feature of the Xilinx Video Timing Controller devices.
xtimebase_sinit.c	Contains static initialization methods for the Xilinx Video Timing Controller device driver.
xtimebase_g.c	Contains a template for a configuration table of Xilinx Video Timing Controller devices. This file is used by the high-level API and will be automatically generated to match the Video Timing Controller device configurations by Xilinx EDK/SDK tools when the software project is built.
xtimebase_hw.h	Contains low-level API (that is, register offset/bit definition and register-level driver API) that can be used to access the Xilinx Video Timing Controller devices.
example.c	An example that demonstrates how to control the Xilinx Video Timing Controller devices using the high-level API.

Xilinx CORE Generator software will place all EDK pCore driver files in the "drivers" subdirectory located in the core output directory. The core output directory is given the same name as the component. For example, if the component name is set to "v_timebase_v2_1_u0," then the device driver source files will be located in the following directory:

```
<coregen project directory>/v_timebase_v2_1_u0/drivers/timebase_v1_01_a/
```

The driver software should be copied to the user's <EDK_Project>/drivers directory or to a user pCores repository.

Parameter Modification in CORE Generator Software

EDK pCore parameters found in the timebase_v2_01_a/data/timebase_v2_1_0.mpd file *cannot* be modified in the Xilinx CORE Generator tool. Parameters shown on the CORE Generator Graphical User Interface will be disabled if the EDK pCore (PLB) Interface is selected. Xilinx recommends that all parameter changes be made with the Video Timing Controller pCore GUI in the EDK environment.

CORE Generator Graphical User Interface (GUI)

The Xilinx Video Timing Controller core is easily configured to meet the developer's specific needs through the CORE Generator graphical user interface (GUI). See Figure 2. This section provides a quick reference to parameters that can be configured at generation time.

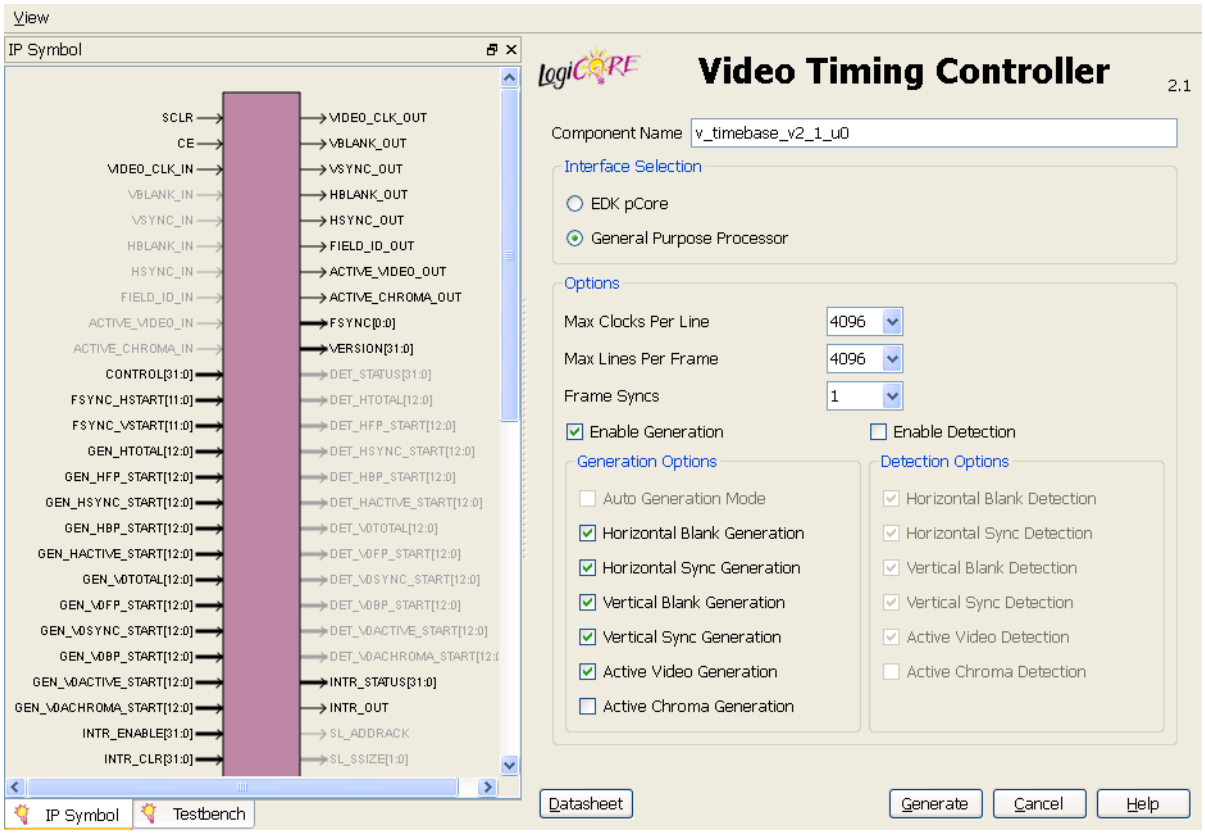

Figure 2: **Video Timing Controller Graphical User Interface**

The GUI displays a representation of the IP symbol on the left side and the parameter assignments on the right side, described as follows:

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_".

  Note: The name **`v_timebase_v2_1`** is not allowed.

- **Interface Selection:** The Video Timing Controller is generated with one of two interfaces
  - **EDK pCore Interface:** The CORE Generator tool will generate the Video Timing Controller as a pCore which can be easily imported into an EDK project as a hardware peripheral. The core registers can then be programmed in real-time via the MicroBlaze processor. See the "EDK pCore (PLB) Interface" section.
  - **General Purpose Processor Interface: The** CORE Generator tool will generate a set of ports that can be used to program the Video Timing Controller. See the "General Purpose Processor Interface" section.
- **Maximum Clocks per Line:** This parameter sets the maximum number of clock cycles per video line that the Video Timing Controller can generate or detect. Values of 128, 256, 512, 1024, 2048 and 4096 are valid.

- **Maximum Lines per Frame:** This parameter sets the maximum number of lines per video frame that the Video Timing Controller can generate or detect. Values of 128, 256, 512, 1024, 2048 and 4096 are valid.
- **Frame Syncs**: This parameter sets the number of frame synchronization outputs to generate and supports up to 16 independent outputs.
- **Enable Generation:** This parameter enables or disables the video timing outputs.
- **Auto Mode Generation:** When enabled, this parameter will cause the generated video timing outputs to change based on the detected inputs. If this parameter is disabled, the video timing outputs will be generated based on only the first detected input format. The output for the generated synchronization signals will continue even if the detection block loses lock. This parameter is available only if both the *Enable Generation* and *Enable Detection* parameters are enabled.

  Note: This parameter has an effect only if one or more of the source select control register bits are set to low.
- **Horizontal Blank Generation:** This parameter enables or disables generating the horizontal blank output.
- **Horizontal Sync Generation:** This parameter enables or disables generating the horizontal synchronization output.
- **Vertical Blank Generation:** This parameter enables or disables generating the vertical blank output.
- **Vertical Sync Generation:** This parameter enables or disables generating the vertical synchronization output.
- **Active Video Generation:** This parameter enables or disables generating the active video output.
- **Active Chroma Generation:** This parameter enables or disables generating the active chroma output.
- **Enable Detection:** This parameter enables or disables the detecting the timing of the video inputs.
- **Horizontal Blank Detection:** This parameter enables or disables detecting the horizontal blank input.
- **Horizontal Sync Detection:** This parameter enables or disables detecting the horizontal synchronization input.
- **Vertical Blank Detection:** This parameter enables or disables detecting the vertical blank input.
- **Vertical Sync Detection:** This parameter enables or disables detecting the vertical synchronization input.
- **Active Video Detection:** This parameter enables or disables detecting the active video input.
- **Active Chroma Detection:** This parameter enables or disables detecting the active chroma input.

Basic Architecture

The Video Timing Controller core contains three modules: the video timing detector, the video timing generator and the interrupt controller. See Figure 3.

Either the detector or the generator module can be disabled with the CORE Generator GUI to save resources.

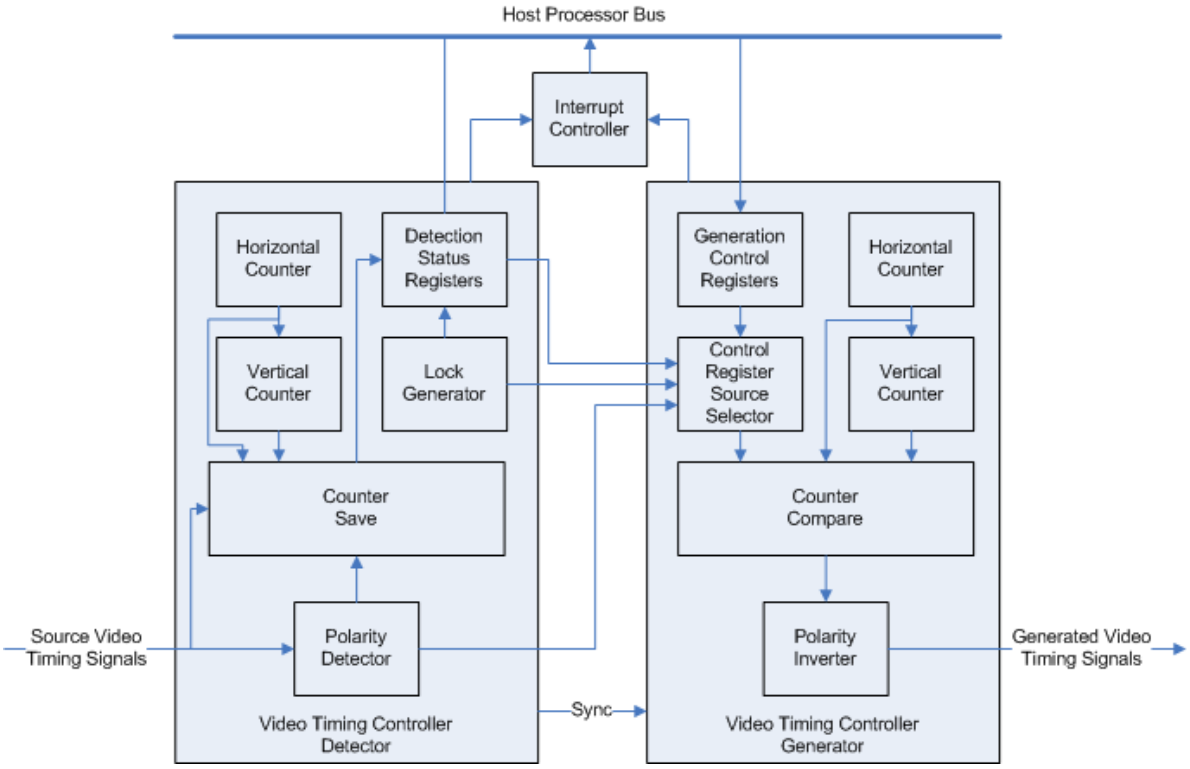

Figure 3: **Video Timing Controller Block Diagram**

Control Signals and Timing

The Video Timing Controller Inputs and Outputs are discussed and shown with timing diagrams in the following sections.

The blanking and active period definitions were discussed previously. In addition to these definitions, the period from the start of blanking (or end of active video) to the start of synchronization is called the front porch. The period from the end of synchronization to the end of blanking (or start of active video) is called the back porch. The total horizontal period (including blanking and active video) can also be defined, and similarly the total vertical period.

Figure 4 shows the start of the horizontal front porch (HFP_Start), synchronization (HSync_Start), back porch (HBP_Start) and active video (Hactive_Start). It also shows the start of the vertical front porch (VFP_Start), synchronization (VSync_Start), back porch (VBP_Start) and active video (Vactive_Start). The total number of horizontal clock cycles is H Total and the total number of lines is the V Total.

These definitions of video frame periods are used for both "Video Timing Detection" and "Video Timing Generation."

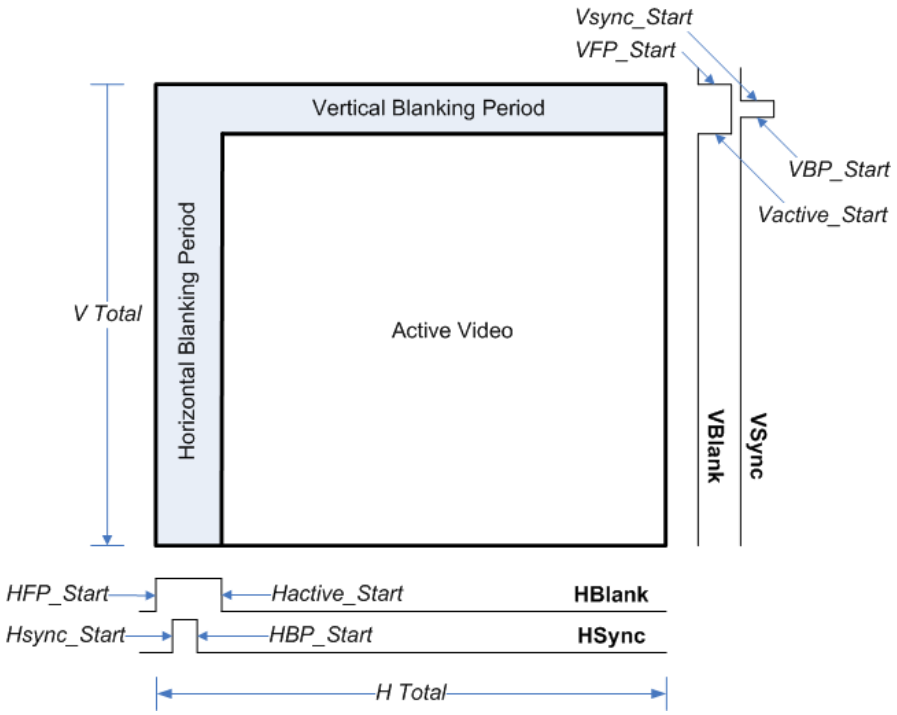

Figure 4: **Example Video Frame and Timing Signals with Front and Back Porch**

Video Timing Detection

The Video Timing Controller has six inputs for detecting the timing of the input video signal: vertical blank, vertical synchronization, horizontal blank, horizontal synchronization, active video and active chroma (see "Detector Interface" in Table 1). To enable detection, the *Enable Detection* GUI parameter must be set, and the control register bit 1 must also be set. The GUI parameter allows saving FPGA resources. The *Control Register* allows run-time flexibility. Other GUI parameters can be set to selectively disable detection of one or more input video timing signals (see "CORE Generator Graphical User Interface (GUI)").

The detected polarity of each input signal is shown by bits 26-20 of the Detection Status Register. High denotes active high polarity, and low denotes active low polarity. Bit 4 of the Detection Status Register shows the number of lines skipped between each active chroma line. High denotes that every other line is skipped (4:2:0), and low denotes that no lines are skipped (4:4:4 or 4:2:2).

The Video Timing Controller also has 11 little-endian output busses to show the status and timing of the input signals. Horizontal Detection Status busses have a width of $\log_2$(*Max Clocks per Line*). Vertical Detection Status busses have a width of $\log_2$(*Max Lines per Frame*).

Video Timing Generation

The Video Timing Controller generates six output video signals: vertical blank, vertical synchronization, horizontal blank, horizontal synchronization, active video and active chroma (see "Generator Interface" in Table 1). To enable generation of these signals, the *Enable Generation* GUI parameter must be set, and the control register bit 0 must also be set. Other GUI parameters can be set to selectively disable generation of one or more video timing signals (see "CORE Generator Graphical User Interface (GUI)").

The polarity of each output signal can be set by bits 26-20 of the *Control Register*. High denotes active high polarity, and low denotes active low polarity. Bit 4 of the Control Register also sets the number of lines skipped between each active chroma line. High denotes that every other line is skipped (4:2:0), and low denotes that no lines are skipped (4:4:4 or 4:2:2).

The Video Timing Controller has 11 little-endian input control busses to set the timing of the output signals. Each bus has a corresponding bit in the *Control Register* (bits 18-8) called *Source Selects* to select the internal detection bus or the external input generation bus. These bits allow the detected timing (if enabled) to control the generated outputs or allow the host processor to override each value independently via the generation input control busses (see "CONTROL REGISTER" in Table 1). Horizontal Generation Control busses have a width of $\log_2$(*Max Clocks per Line*). Vertical Generation Control busses have a width of $\log_2$(*Max Lines per Frame*).

Table 26 through Table 31 show example settings of the input control busses and the resultant video timing output signals.

Programming the horizontal generation registers to the values shown in Table 26 will result in the video timing signal outputs shown in Figure 5.

Notice that in Table 26 the Control Register bit 0 is set to enable generation, that all source selects are set to 1 to select the Generation Registers and that the polarity bits are all set to 1 to configure the outputs for active high polarity. (See "CONTROL REGISTER" in Table 1 for a description of this register).

Table 26: **Example Horizontal Generation Register Inputs**

Generation Register Input	Value
gen_htotal	0x006
gen_hfp_start	0x000
gen_hsync_start	0x001
gen_hbp_start	0x002
gen_hactive_start	0x004
control	0x07f7_ff05

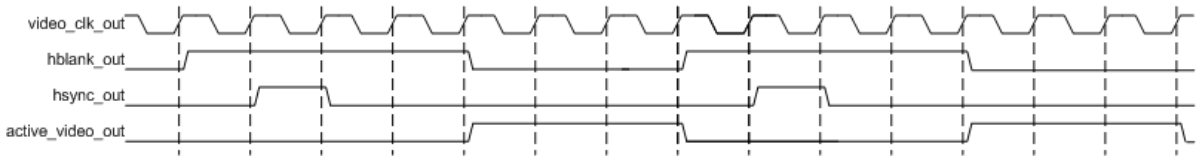

Figure 5: **Generated Horizontal Timing**

Note: All signals are shown active high. The polarities of the output signals can be changed at any time in the control register.

Next, an example vertical generation configuration is given. Programming the vertical generation registers to the values shown in Table 27 will result in the video timing signal outputs shown in Figure 6.

Notice that in Table 27 the Control Register bit 4 is set to 0 to configure the number of lines skipped between each active chroma line to be 0. This configures the Active Chroma output signal for 4:4:4 or 4:2:2 mode in which every line contains valid chroma samples. (See "CONTROL REGISTER" in Table 1 for a description of this register.)

Table 27: **Example Vertical Generation Register Inputs**

Generation Register Input	Value
gen_v0total	0x006
gen_v0fp_start	0x000
gen_v0sync_start	0x001
gen_v0bp_start	0x002
gen_v0active_start	0x003
gen_v0achroma_start	0x003
control	0x07f7_ff05

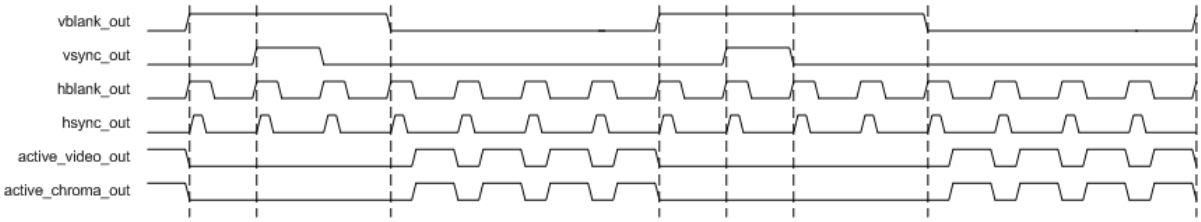

Figure 6: **Generated Vertical Timing (4:4:4 Chroma)**

Next is a vertical generation example similar to the previous except that the Active Chroma output is configured to for YUV 4:2:0. Programming the vertical generation registers to the values shown in Table 28 will result in the video timing signal outputs shown in Figure 7.

Notice that in Table 28 the Control Register bit 4 is set to 1 to configure the number of lines skipped between each active chroma line to be one line. This configures the Active Chroma output signal for 4:2:0 mode in which only every other line contains valid chroma samples. (See "CONTROL REGISTER" in Table 1 for a description of this register.)

Table 28: **Example Vertical Generation Register Inputs (4:2:0 Chroma)**

Generation Register Input	Value
gen_v0total	0x006
gen_v0fp_start	0x000
gen_v0sync_start	0x001
gen_v0bp_start	0x002
gen_v0active_start	0x003
gen_v0achroma_start	0x003
control	0x07f7_ff15

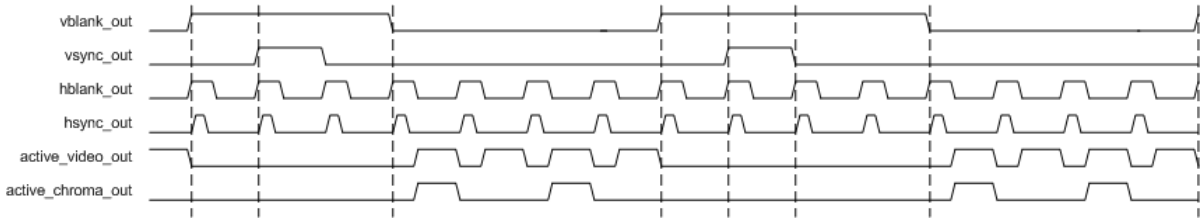

Figure 7: **Generated Vertical Timing (4:2:0 Chroma)**

Next is a vertical generation example similar to the previous except that the Active Chroma output is configured to be active for odd lines instead of even lines. Programming the vertical generation registers to the values shown in Table 29 will result in the video timing signal outputs shown in Figure 8.

Notice that the Generated Active Chroma Start Register is set to 4 instead of 3, as in the previous example. This configures the Active Chroma output signal for 4:2:0 mode, but with the opposite line set.

Table 29: **Example Vertical Generation Register Inputs (Alternate 4:2:0 Chroma)**

Generation Register Input	Value
gen_v0total	0x006
gen_v0fp_start	0x000
gen_v0sync_start	0x001
gen_v0bp_start	0x002
gen_v0active_start	0x003
gen_v0achroma_start	0x004
control	0x07f7_ff15

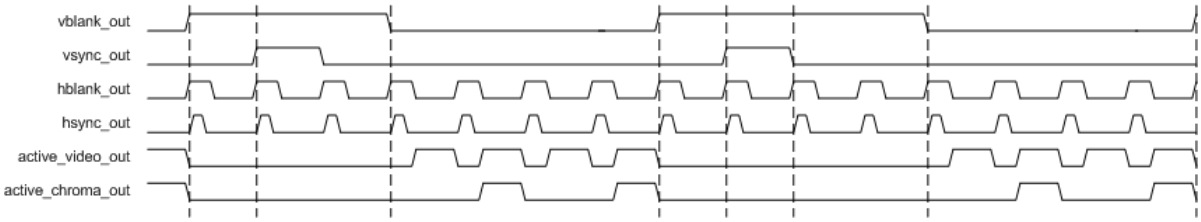

Figure 8: **Generated Vertical Timing (Alternate 4:2:0 Chroma)**

The next example shows how the Video Timing Controller can be configured to regenerate timing signals to selectively override individual characteristics. Table 30 shows the detection output register output signals. Programming the horizontal generation registers to the values shown in Table 31 will result in the video timing signal outputs shown in Figure 9.

Table 30: **Example Horizontal Detection Register Outputs**

Detection Register Output	Value
det_htotal	0x006
det_hfp_start	0x000
det_hsync_start	0x001
det_hbp_start	0x002
det_hactive_start	0x004
det_status	0x07f0_000

Notice that all polarities bits are high in the Detection Status Register, signifying that all inputs are detected to have an active high polarity.

Table 31: **Example Horizontal Generation Register Inputs**

Generation Register Input	Value
gen_hfp_start	0x006
gen_hactive_start	0x005
control	0x07e0_1207

Notice, in the Control Register, that bit 0 is set to enable generation, bit 1 is set to enable detection and bit 2 is set to enable synchronizing the generated output to the detected inputs.

The Horizontal Front Porch Start Register Source Select (bit 9 of the Control Register) is set to 1 and the Horizontal Active Video Start Register Source Select (bit 12 of the Control Register) is set to 1. This signifies that the `gen_hfp_start` and the `gen_hactive_start` registers will be used instead of the `det_hfp_start` and the `det_hactive_start` registers since these values are being overridden. All other source selects are low, signifying that the detection register should be used.

Also notice that the polarity of the output horizontal synchronization has been changed to active low by clearing bit 20 of the Control Register.

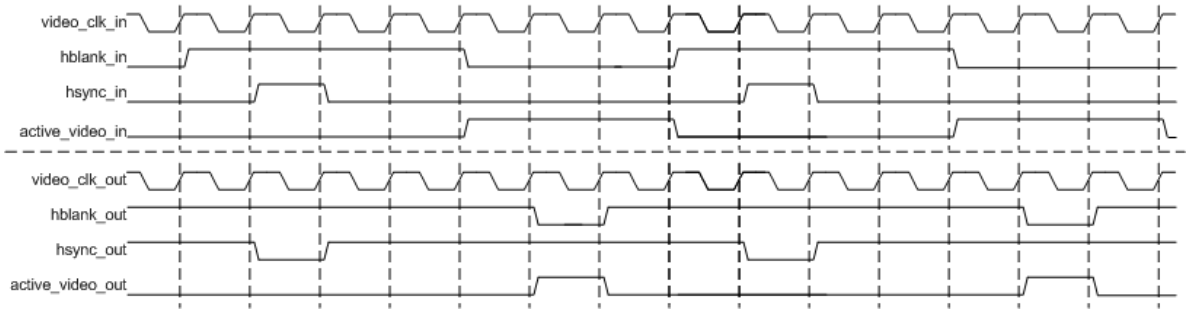

Figure 9: **Detected and Regenerated Horizontal Timing**

Note: All generated outputs remain synchronized to the inputs. The only changes made to the output are to the horizontal synchronization polarity and to the active video start and stop times.

Synchronization

Generation of the video timing output signals can be synchronized to the detected video timing input signals or generated independently. Synchronization of the output to the input allows the developer to override each individual timing signal with different settings such as signal polarity or start time. For example, the active video signal could be regenerated shifted one cycle earlier or later. This provides a flexible method for regenerating video timing output signals with different settings while remaining synchronized to the input timing.

The Video Timing Controller also has a GUI parameter, called Auto Mode Generation, to control the behavior of the generated outputs based on the detected inputs. When the Auto Mode Generation parameter is set, the generated video timing outputs will change based on the detected inputs. If this parameter is not set, then the video timing outputs will be generated based on only the first detected input format. (If the detector loses lock, the generated outputs will continue to be generated.) To change output timing while Auto Mode Generation is set, timing detection must first be disabled by clearing bit 1 in the Control Register and then re-enabling, if any of the Source Select bits are low.

Frame Syncs

The Video Timing Controller has a frame synchronization output bus. Each bit can be configured to toggle high for any one clock cycle during each video frame. Each bit is independently configured for horizontal and vertical clock cycle position with the `fsync_hstart` and `fsync_vstart` registers. Table 32 shows which bits in the `fsync_hstart` and `fsync_vstart` registers control which frame synchronization output.

Table 32: **Frame Synchronization Control Registers**

Frame Synchronization Output	Horizontal Position (fsync_hstart) Bits	Vertical Position (fsync_vstart) Bits
fsync[0]	[log2(x) - 1] to [0]	[log2(y) - 1] to [0]
fsync[1]	[2*log2(x) - 1] to [log2(x)]	[2*log2(y) - 1] to [log2(y)]
fsync[2]	[3*log2(x) - 1] to [2*log2(x)]	[3*log2(y) - 1] to [2*log2(y)]
fsync[3]	[4*log2(x) - 1] to [3*log2(x)]	[4*log2(y) - 1] to [3*log2(y)]
fsync[4]	[5*log2(x) - 1] to [4*log2(x)]	[5*log2(y) - 1] to [4*log2(y)]
fsync[5]	[6*log2(x) - 1] to [5*log2(x)]	[6*log2(y) - 1] to [5*log2(y)]
fsync[6]	[7*log2(x) - 1] to [6*log2(x)]	[7*log2(y) - 1] to [6*log2(y)]
fsync[7]	[8*log2(x) - 1] to [7*log2(x)]	[8*log2(y) - 1] to [7*log2(y)]
fsync[8]	[9*log2(x) - 1] to [8*log2(x)]	[9*log2(y) - 1] to [8*log2(y)]
fsync[9]	[10*log2(x) - 1] to [9*log2(x)]	[10*log2(y) - 1] to [9*log2(y)]
fsync[10]	[11*log2(x) - 1] to [10*log2(x)]	[11*log2(y) - 1] to [10*log2(y)]
fsync[11]	[12*log2(x) - 1] to [11*log2(x)]	[12*log2(y) - 1] to [11*log2(y)]
fsync[12]	[13*log2(x) - 1] to [12*log2(x)]	[13*log2(y) - 1] to [12*log2(y)]
fsync[13]	[14*log2(x) - 1] to [13*log2(x)]	[14*log2(y) - 1] to [13*log2(y)]
fsync[14]	[15*log2(x) - 1] to [14*log2(x)]	[15*log2(y) - 1] to [14*log2(y)]
fsync[15]	[16*log2(x) - 1] to [15*log2(x)]	[16*log2(y) - 1] to [15*log2(y)]

Notes:

1. x is the Max Clocks per Line GUI parameter. y is the Max Lines per Frame GUI parameter.
2. The width of the frame synchronization bus is configured with the Frame Syncs GUI parameter. Frame syncs can be used for various control applications including controlling the timing of processing of external modules.

Host CPU Interrupts

The Video Timing Controller has an active high host CPU interrupt output. This output is set high when an interrupt occurs and set low when the interrupt event has been cleared by the host CPU. The Video Timing Controller also contains three 32-bit registers for configuring and reporting status of interrupts: the Interrupt Status, the Interrupt Enable and the Interrupt Clear Registers. A logical AND is performed on the Interrupt Enable Register and the Interrupt Status Register to set the interrupt output high. The Interrupt Clear Register is used to clear the Interrupt Status Register. Interrupt Status Register bits are cleared only on the rising edge of the corresponding Interrupt Clear Register. Therefore, each bit in the Interrupt Clear Register must be driven low before being driven high to clear the status register bits.

The polarity of the lock interrupts is configurable by bit 3 in the Control Register (see Table 1). When this bit is low, the lock interrupts (see "INTERRUPT STATUS REGISTER") will trigger an interrupt on the falling edge of the internal lock signals, signifying that the detected input has changed timing. When high, the lock interrupts will trigger an interrupt on the rising edge of the internal lock signals, signifying that a lock has been achieved on the detected input.

Use Model

This section illustrates a likely usage scenario for the Xilinx Video Timing Controller core.

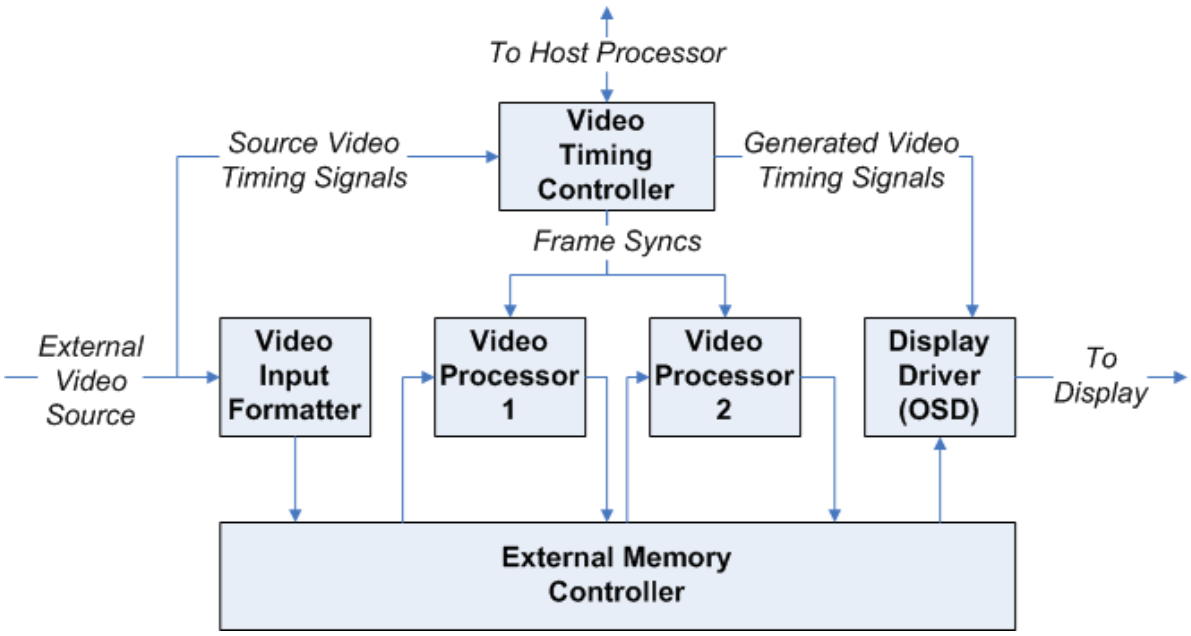

Figure 10: **Example Video Timing Controller Use Model**

Figure 10 shows four features of the Video Timing Controller being utilized in a video system:

1. Detection of the source video frame timing
2. Generation of video timing signals
3. Generation of two Frame Syncs to control the Video Processors
4. Connection to a Host Processor via the General Purpose Processor Interface

To detect the timing of the source video, the timing signals are connected to the Video Timing Controller Detection Module. Both the timing and the signal polarity of the timing signals are captured and easily read by the host processor.

Video timing signals are generated to control a display driver module and an external display. The timing of these output signals is controlled by the host processor. The Video Timing Controller can be configured in real-time to replicate the source video format or to slightly change the format on the output, for example, in cases where the input signals are positive polarity yet the display requires negative polarity synchronization signals. The Video Timing Controller can also be reconfigured in real-time to output a completely different format from the input source.

Two Frame Sync outputs are generated to control Video Processor 1 and Video Processor 2. These outputs could be used to control when Video Processor 2 starts processing relative to when Video Processor 1 starts processing. These Frame Syncs can be reconfigured in real-time as well.

The Video Timing Controller is connected to a Host Processor in this example. General Purpose Processor Interface allows for easy connection between status/control registers and the host processor. In addition, the Video Timing Controller interrupt output can also be used to synchronize the software with hardware events.

Core Resource Utilization

Resource requirements for the Xilinx Timing Controller LogiCore are estimated in tables 33, 34, 35, and 36 for Spartan®-3A DSP, Virtex®-5, Spartan-6, and Virtex-6 devices respectively. Resource usage values were generated using the Xilinx CORE Generator tools v12.3. They are derived from post-synthesis reports, and may change during MAP and PAR. The resource usage values in the following tables are for the General Purpose Processor Interface. The EDK pCore Interface adds an estimated additional 250 to 460 to 810 LUTs and 460 flip-flops. The Xilinx Timing Controller LogiCore does not utilize Block RAM.

Table 33: **Spartan-3A DSP Device Resource Estimates**

Maximum Clocks	Maximum Lines	Detection Enable	Generation Enable	H/V Blanks	H/V Syncs	Active Video	Active Chroma	LUTs	FFs
256	256	No	Yes	No	Yes	No	No	107	114
256	256	No	Yes	No	Yes	No	Yes	140	152
256	256	No	Yes	No	Yes	Yes	No	131	144
256	256	No	Yes	No	Yes	Yes	Yes	143	156
256	256	No	Yes	Yes	No	No	No	109	109
256	256	No	Yes	Yes	No	No	Yes	120	121
256	256	No	Yes	Yes	No	Yes	No	113	113
256	256	No	Yes	Yes	No	Yes	Yes	125	125
256	256	No	Yes	Yes	Yes	No	No	132	145
256	256	No	Yes	Yes	Yes	No	Yes	144	157
256	256	No	Yes	Yes	Yes	Yes	No	137	149
256	256	No	Yes	Yes	Yes	Yes	Yes	149	161
256	256	Yes	No	No	Yes	No	No	88	121
256	256	Yes	No	No	Yes	No	Yes	98	144

Table 33: **Spartan-3A DSP Device Resource Estimates**

256	256	Yes	No	No	Yes	Yes	No	147	207
256	256	Yes	No	No	Yes	Yes	Yes	160	233
256	256	Yes	No	Yes	No	No	No	110	148
256	256	Yes	No	Yes	No	No	Yes	121	171
256	256	Yes	No	Yes	No	Yes	No	155	179
256	256	Yes	No	Yes	No	Yes	Yes	170	205
256	256	Yes	No	Yes	Yes	No	No	171	224
256	256	Yes	No	Yes	Yes	No	Yes	181	247
256	256	Yes	No	Yes	Yes	Yes	No	233	278
256	256	Yes	No	Yes	Yes	Yes	Yes	247	304
256	256	Yes	Yes	No	Yes	No	No	270	254
256	256	Yes	Yes	No	Yes	No	Yes	351	315
256	256	Yes	Yes	No	Yes	Yes	No	386	371
256	256	Yes	Yes	No	Yes	Yes	Yes	419	409
256	256	Yes	Yes	Yes	No	No	No	286	277
256	256	Yes	Yes	Yes	No	No	Yes	318	312
256	256	Yes	Yes	Yes	No	Yes	No	336	312
256	256	Yes	Yes	Yes	No	Yes	Yes	370	350
256	256	Yes	Yes	Yes	Yes	No	No	409	388
256	256	Yes	Yes	Yes	Yes	No	Yes	439	423
256	256	Yes	Yes	Yes	Yes	Yes	No	477	447
256	256	Yes	Yes	Yes	Yes	Yes	Yes	510	485
512	512	No	Yes	Yes	Yes	Yes	Yes	153	176
512	512	Yes	No	Yes	Yes	Yes	Yes	268	332
512	512	Yes	Yes	Yes	Yes	Yes	Yes	551	530
1024	1024	No	Yes	Yes	Yes	Yes	Yes	162	191
1024	1024	Yes	No	Yes	Yes	Yes	Yes	276	360
1024	1024	Yes	Yes	Yes	Yes	Yes	Yes	582	575
2048	2048	No	Yes	Yes	Yes	Yes	Yes	182	206
2048	2048	Yes	No	Yes	Yes	Yes	Yes	301	388
2048	2048	Yes	Yes	Yes	Yes	Yes	Yes	640	620
4096	4096	No	Yes	No	Yes	No	No	143	158
4096	4096	No	Yes	No	Yes	No	Yes	179	212
4096	4096	No	Yes	No	Yes	Yes	No	172	200
4096	4096	No	Yes	No	Yes	Yes	Yes	182	216
4096	4096	No	Yes	Yes	No	No	No	144	149
4096	4096	No	Yes	Yes	No	No	Yes	155	165
4096	4096	No	Yes	Yes	No	Yes	No	148	153
4096	4096	No	Yes	Yes	No	Yes	Yes	159	169

Table 33: **Spartan-3A DSP Device Resource Estimates**

4096	4096	No	Yes	Yes	Yes	No	No	172	201
4096	4096	No	Yes	Yes	Yes	No	Yes	183	217
4096	4096	No	Yes	Yes	Yes	Yes	No	177	205
4096	4096	No	Yes	Yes	Yes	Yes	Yes	187	221
4096	4096	Yes	No	No	Yes	No	No	115	169
4096	4096	Yes	No	No	Yes	No	Yes	126	200
4096	4096	Yes	No	No	Yes	Yes	No	187	287
4096	4096	Yes	No	No	Yes	Yes	Yes	201	321
4096	4096	Yes	No	Yes	No	No	No	140	204
4096	4096	Yes	No	Yes	No	No	Yes	152	235
4096	4096	Yes	No	Yes	No	Yes	No	194	243
4096	4096	Yes	No	Yes	No	Yes	Yes	210	277
4096	4096	Yes	No	Yes	Yes	No	No	220	312
4096	4096	Yes	No	Yes	Yes	No	Yes	231	343
4096	4096	Yes	No	Yes	Yes	Yes	No	296	382
4096	4096	Yes	No	Yes	Yes	Yes	Yes	311	416
4096	4096	Yes	Yes	No	Yes	No	No	370	354
4096	4096	Yes	Yes	No	Yes	No	Yes	470	439
4096	4096	Yes	Yes	No	Yes	Yes	No	512	515
4096	4096	Yes	Yes	No	Yes	Yes	Yes	550	565
4096	4096	Yes	Yes	Yes	No	No	No	384	381
4096	4096	Yes	Yes	Yes	No	No	Yes	423	428
4096	4096	Yes	Yes	Yes	No	Yes	No	443	424
4096	4096	Yes	Yes	Yes	No	Yes	Yes	485	474
4096	4096	Yes	Yes	Yes	Yes	No	No	545	540
4096	4096	Yes	Yes	Yes	Yes	No	Yes	580	587
4096	4096	Yes	Yes	Yes	Yes	Yes	No	627	615
4096	4096	Yes	Yes	Yes	Yes	Yes	Yes	665	665

Table 34: **Virtex-5 Device Resource Estimates**

Maximum Clocks	Maximum Lines	Detection Enable	Generation Enable	H/V Blanks	H/V Syncs	Active Video	Active Chroma	LUTs	FFs
256	256	No	Yes	No	Yes	No	No	92	114
256	256	No	Yes	No	Yes	No	Yes	112	152
256	256	No	Yes	No	Yes	Yes	No	111	144
256	256	No	Yes	No	Yes	Yes	Yes	117	156
256	256	No	Yes	Yes	No	No	No	96	109
256	256	No	Yes	Yes	No	No	Yes	102	121

Table 34: **Virtex-5 Device Resource Estimates *(Cont'd)***

256	256	No	Yes	Yes	No	Yes	No	98	113
256	256	No	Yes	Yes	No	Yes	Yes	105	125
256	256	No	Yes	Yes	Yes	No	No	112	145
256	256	No	Yes	Yes	Yes	No	Yes	117	157
256	256	No	Yes	Yes	Yes	Yes	No	115	149
256	256	No	Yes	Yes	Yes	Yes	Yes	120	161
256	256	Yes	No	No	Yes	No	No	102	121
256	256	Yes	No	No	Yes	No	Yes	113	144
256	256	Yes	No	No	Yes	Yes	No	155	207
256	256	Yes	No	No	Yes	Yes	Yes	169	233
256	256	Yes	No	Yes	No	No	No	120	148
256	256	Yes	No	Yes	No	No	Yes	131	171
256	256	Yes	No	Yes	No	Yes	No	155	179
256	256	Yes	No	Yes	No	Yes	Yes	170	205
256	256	Yes	No	Yes	Yes	No	No	206	224
256	256	Yes	No	Yes	Yes	No	Yes	218	247
256	256	Yes	No	Yes	Yes	Yes	No	298	278
256	256	Yes	No	Yes	Yes	Yes	Yes	313	304
256	256	Yes	Yes	No	Yes	No	No	260	254
256	256	Yes	Yes	No	Yes	No	Yes	327	315
256	256	Yes	Yes	No	Yes	Yes	No	357	371
256	256	Yes	Yes	No	Yes	Yes	Yes	389	409
256	256	Yes	Yes	Yes	No	No	No	282	277
256	256	Yes	Yes	Yes	No	No	Yes	309	312
256	256	Yes	Yes	Yes	No	Yes	No	321	312
256	256	Yes	Yes	Yes	No	Yes	Yes	350	350
256	256	Yes	Yes	Yes	Yes	No	No	417	388
256	256	Yes	Yes	Yes	Yes	No	Yes	453	423
256	256	Yes	Yes	Yes	Yes	Yes	No	515	447
256	256	Yes	Yes	Yes	Yes	Yes	Yes	550	485
512	512	No	Yes	Yes	Yes	Yes	Yes	130	176
512	512	Yes	No	Yes	Yes	Yes	Yes	324	332
512	512	Yes	Yes	Yes	Yes	Yes	Yes	574	530
1024	1024	No	Yes	Yes	Yes	Yes	Yes	136	191
1024	1024	Yes	No	Yes	Yes	Yes	Yes	337	360
1024	1024	Yes	Yes	Yes	Yes	Yes	Yes	614	575
2048	2048	No	Yes	Yes	Yes	Yes	Yes	156	206
2048	2048	Yes	No	Yes	Yes	Yes	Yes	355	388
2048	2048	Yes	Yes	Yes	Yes	Yes	Yes	666	620

Table 34: **Virtex-5 Device Resource Estimates *(Cont'd)***

4096	4096	No	Yes	No	Yes	No	No	125	158
4096	4096	No	Yes	No	Yes	No	Yes	148	212
4096	4096	No	Yes	No	Yes	Yes	No	150	200
4096	4096	No	Yes	No	Yes	Yes	Yes	153	216
4096	4096	No	Yes	Yes	No	No	No	124	149
4096	4096	No	Yes	Yes	No	No	Yes	132	165
4096	4096	No	Yes	Yes	No	Yes	No	127	153
4096	4096	No	Yes	Yes	No	Yes	Yes	135	169
4096	4096	No	Yes	Yes	Yes	No	No	152	201
4096	4096	No	Yes	Yes	Yes	No	Yes	153	217
4096	4096	No	Yes	Yes	Yes	Yes	No	154	205
4096	4096	No	Yes	Yes	Yes	Yes	Yes	156	221
4096	4096	Yes	No	No	Yes	No	No	122	169
4096	4096	Yes	No	No	Yes	No	Yes	136	200
4096	4096	Yes	No	No	Yes	Yes	No	182	287
4096	4096	Yes	No	No	Yes	Yes	Yes	200	321
4096	4096	Yes	No	Yes	No	No	No	145	204
4096	4096	Yes	No	Yes	No	No	Yes	157	235
4096	4096	Yes	No	Yes	No	Yes	No	235	243
4096	4096	Yes	No	Yes	No	Yes	Yes	204	277
4096	4096	Yes	No	Yes	Yes	No	No	233	312
4096	4096	Yes	No	Yes	Yes	No	Yes	245	343
4096	4096	Yes	No	Yes	Yes	Yes	No	342	382
4096	4096	Yes	No	Yes	Yes	Yes	Yes	362	416
4096	4096	Yes	Yes	No	Yes	No	No	373	354
4096	4096	Yes	Yes	No	Yes	No	Yes	452	439
4096	4096	Yes	Yes	No	Yes	Yes	No	504	515
4096	4096	Yes	Yes	No	Yes	Yes	Yes	528	565
4096	4096	Yes	Yes	Yes	No	No	No	379	381
4096	4096	Yes	Yes	Yes	No	No	Yes	413	428
4096	4096	Yes	Yes	Yes	No	Yes	No	484	424
4096	4096	Yes	Yes	Yes	No	Yes	Yes	526	474
4096	4096	Yes	Yes	Yes	Yes	No	No	534	540
4096	4096	Yes	Yes	Yes	Yes	No	Yes	576	587
4096	4096	Yes	Yes	Yes	Yes	Yes	No	661	615
4096	4096	Yes	Yes	Yes	Yes	Yes	Yes	690	665

Table 35: **Spartan-6 Device Resource Estimates**

Maximum Clocks	Maximum Lines	Detection Enable	Generation Enable	H/V Blanks	H/V Syncs	Active Video	Active Chroma	LUTs	FFs
256	256	No	Yes	No	Yes	No	No	108	114
256	256	No	Yes	No	Yes	No	Yes	136	152
256	256	No	Yes	No	Yes	Yes	No	127	144
256	256	No	Yes	No	Yes	Yes	Yes	135	156
256	256	No	Yes	Yes	No	No	No	108	109
256	256	No	Yes	Yes	No	No	Yes	107	121
256	256	No	Yes	Yes	No	Yes	No	105	113
256	256	No	Yes	Yes	No	Yes	Yes	110	125
256	256	No	Yes	Yes	Yes	No	No	130	145
256	256	No	Yes	Yes	Yes	No	Yes	136	157
256	256	No	Yes	Yes	Yes	Yes	No	137	149
256	256	No	Yes	Yes	Yes	Yes	Yes	143	161
256	256	Yes	No	No	Yes	No	No	106	121
256	256	Yes	No	No	Yes	No	Yes	119	144
256	256	Yes	No	No	Yes	Yes	No	193	207
256	256	Yes	No	No	Yes	Yes	Yes	181	233
256	256	Yes	No	Yes	No	No	No	128	148
256	256	Yes	No	Yes	No	No	Yes	144	171
256	256	Yes	No	Yes	No	Yes	No	210	179
256	256	Yes	No	Yes	No	Yes	Yes	193	206
256	256	Yes	No	Yes	Yes	No	No	213	224
256	256	Yes	No	Yes	Yes	No	Yes	218	247
256	256	Yes	No	Yes	Yes	Yes	No	276	279
256	256	Yes	No	Yes	Yes	Yes	Yes	306	306
256	256	Yes	Yes	No	Yes	No	No	260	253
256	256	Yes	Yes	No	Yes	No	Yes	329	315
256	256	Yes	Yes	No	Yes	Yes	No	388	371
256	256	Yes	Yes	No	Yes	Yes	Yes	394	410
256	256	Yes	Yes	Yes	No	No	No	267	277
256	256	Yes	Yes	Yes	No	No	Yes	300	313
256	256	Yes	Yes	Yes	No	Yes	No	354	312
256	256	Yes	Yes	Yes	No	Yes	Yes	364	352
256	256	Yes	Yes	Yes	Yes	No	No	398	387
256	256	Yes	Yes	Yes	Yes	No	Yes	429	423
256	256	Yes	Yes	Yes	Yes	Yes	No	459	448
256	256	Yes	Yes	Yes	Yes	Yes	Yes	489	487

Table 35: **Spartan-6 Device Resource Estimates**

512	512	No	Yes	Yes	Yes	Yes	Yes	158	176
512	512	Yes	No	Yes	Yes	Yes	Yes	329	334
512	512	Yes	Yes	Yes	Yes	Yes	Yes	602	535
1024	1024	No	Yes	Yes	Yes	Yes	Yes	179	191
1024	1024	Yes	No	Yes	Yes	Yes	Yes	368	362
1024	1024	Yes	Yes	Yes	Yes	Yes	Yes	668	583
2048	2048	No	Yes	Yes	Yes	Yes	Yes	197	206
2048	2048	Yes	No	Yes	Yes	Yes	Yes	407	390
2048	2048	Yes	Yes	Yes	Yes	Yes	Yes	744	629
4096	4096	No	Yes	No	Yes	No	No	160	160
4096	4096	No	Yes	No	Yes	No	Yes	197	214
4096	4096	No	Yes	No	Yes	Yes	No	190	202
4096	4096	No	Yes	No	Yes	Yes	Yes	187	218
4096	4096	No	Yes	Yes	No	No	No	162	149
4096	4096	No	Yes	Yes	No	No	Yes	164	165
4096	4096	No	Yes	Yes	No	Yes	No	163	153
4096	4096	No	Yes	Yes	No	Yes	Yes	165	169
4096	4096	No	Yes	Yes	Yes	No	No	185	203
4096	4096	No	Yes	Yes	Yes	No	Yes	194	219
4096	4096	No	Yes	Yes	Yes	Yes	No	187	207
4096	4096	No	Yes	Yes	Yes	Yes	Yes	197	223
4096	4096	Yes	No	No	Yes	No	No	130	169
4096	4096	Yes	No	No	Yes	No	Yes	143	200
4096	4096	Yes	No	No	Yes	Yes	No	222	287
4096	4096	Yes	No	No	Yes	Yes	Yes	241	321
4096	4096	Yes	No	Yes	No	No	No	165	204
4096	4096	Yes	No	Yes	No	No	Yes	190	235
4096	4096	Yes	No	Yes	No	Yes	No	277	244
4096	4096	Yes	No	Yes	No	Yes	Yes	287	279
4096	4096	Yes	No	Yes	Yes	No	No	318	313
4096	4096	Yes	No	Yes	Yes	No	Yes	335	344
4096	4096	Yes	No	Yes	Yes	Yes	No	418	383
4096	4096	Yes	No	Yes	Yes	Yes	Yes	402	418
4096	4096	Yes	Yes	No	Yes	No	No	349	353
4096	4096	Yes	Yes	No	Yes	No	Yes	427	439
4096	4096	Yes	Yes	No	Yes	Yes	No	487	516
4096	4096	Yes	Yes	No	Yes	Yes	Yes	550	566
4096	4096	Yes	Yes	Yes	No	No	No	380	381
4096	4096	Yes	Yes	Yes	No	No	Yes	426	430

Table 35: **Spartan-6 Device Resource Estimates**

4096	4096	Yes	Yes	Yes	No	Yes	No	517	426
4096	4096	Yes	Yes	Yes	No	Yes	Yes	554	477
4096	4096	Yes	Yes	Yes	Yes	No	No	599	539
4096	4096	Yes	Yes	Yes	Yes	No	Yes	624	587
4096	4096	Yes	Yes	Yes	Yes	Yes	No	728	620
4096	4096	Yes	Yes	Yes	Yes	Yes	Yes	730	668

Table 36: **Virtex-6 Device Resource Estimates**

Maximum Clocks	Maximum Lines	Detection Enable	Generation Enable	H/V Blanks	H/V Syncs	Active Video	Active Chroma	LUTs	FFs
256	256	No	Yes	No	Yes	No	No	101	114
256	256	No	Yes	No	Yes	No	Yes	109	152
256	256	No	Yes	No	Yes	Yes	No	114	144
256	256	No	Yes	No	Yes	Yes	Yes	134	156
256	256	No	Yes	Yes	No	No	No	87	109
256	256	No	Yes	Yes	No	No	Yes	96	121
256	256	No	Yes	Yes	No	Yes	No	90	113
256	256	No	Yes	Yes	No	Yes	Yes	100	125
256	256	No	Yes	Yes	Yes	No	No	120	145
256	256	No	Yes	Yes	Yes	No	Yes	134	157
256	256	No	Yes	Yes	Yes	Yes	No	119	149
256	256	No	Yes	Yes	Yes	Yes	Yes	128	161
256	256	Yes	No	No	Yes	No	No	100	121
256	256	Yes	No	No	Yes	No	Yes	112	144
256	256	Yes	No	No	Yes	Yes	No	145	207
256	256	Yes	No	No	Yes	Yes	Yes	177	233
256	256	Yes	No	Yes	No	No	No	130	148
256	256	Yes	No	Yes	No	No	Yes	129	171
256	256	Yes	No	Yes	No	Yes	No	199	179
256	256	Yes	No	Yes	No	Yes	Yes	209	205
256	256	Yes	No	Yes	Yes	No	No	187	224
256	256	Yes	No	Yes	Yes	No	Yes	208	247
256	256	Yes	No	Yes	Yes	Yes	No	254	278
256	256	Yes	No	Yes	Yes	Yes	Yes	275	304
256	256	Yes	Yes	No	Yes	No	No	244	253
256	256	Yes	Yes	No	Yes	No	Yes	293	314
256	256	Yes	Yes	No	Yes	Yes	No	346	371
256	256	Yes	Yes	No	Yes	Yes	Yes	346	409
256	256	Yes	Yes	Yes	No	No	No	256	277

Table 36: **Virtex-6 Device Resource Estimates**

256	256	Yes	Yes	Yes	No	No	Yes	280	312
256	256	Yes	Yes	Yes	No	Yes	No	335	312
256	256	Yes	Yes	Yes	No	Yes	Yes	363	350
256	256	Yes	Yes	Yes	Yes	No	No	366	387
256	256	Yes	Yes	Yes	Yes	No	Yes	393	422
256	256	Yes	Yes	Yes	Yes	Yes	No	426	447
256	256	Yes	Yes	Yes	Yes	Yes	Yes	446	485
512	512	No	Yes	Yes	Yes	Yes	Yes	136	176
512	512	Yes	No	Yes	Yes	Yes	Yes	334	332
512	512	Yes	Yes	Yes	Yes	Yes	Yes	538	530
1024	1024	No	Yes	Yes	Yes	Yes	Yes	148	191
1024	1024	Yes	No	Yes	Yes	Yes	Yes	341	360
1024	1024	Yes	Yes	Yes	Yes	Yes	Yes	561	575
2048	2048	No	Yes	Yes	Yes	Yes	Yes	169	206
2048	2048	Yes	No	Yes	Yes	Yes	Yes	365	388
2048	2048	Yes	Yes	Yes	Yes	Yes	Yes	615	620
4096	4096	No	Yes	No	Yes	No	No	133	158
4096	4096	No	Yes	No	Yes	No	Yes	165	212
4096	4096	No	Yes	No	Yes	Yes	No	160	200
4096	4096	No	Yes	No	Yes	Yes	Yes	173	216
4096	4096	No	Yes	Yes	No	No	No	129	149
4096	4096	No	Yes	Yes	No	No	Yes	134	165
4096	4096	No	Yes	Yes	No	Yes	No	123	153
4096	4096	No	Yes	Yes	No	Yes	Yes	134	169
4096	4096	No	Yes	Yes	Yes	No	No	162	201
4096	4096	No	Yes	Yes	Yes	No	Yes	161	217
4096	4096	No	Yes	Yes	Yes	Yes	No	162	205
4096	4096	No	Yes	Yes	Yes	Yes	Yes	165	221
4096	4096	Yes	No	No	Yes	No	No	128	169
4096	4096	Yes	No	No	Yes	No	Yes	145	200
4096	4096	Yes	No	No	Yes	Yes	No	209	287
4096	4096	Yes	No	No	Yes	Yes	Yes	212	321
4096	4096	Yes	No	Yes	No	No	No	171	204
4096	4096	Yes	No	Yes	No	No	Yes	177	235
4096	4096	Yes	No	Yes	No	Yes	No	204	243
4096	4096	Yes	No	Yes	No	Yes	Yes	240	277
4096	4096	Yes	No	Yes	Yes	No	No	259	312
4096	4096	Yes	No	Yes	Yes	No	Yes	272	343
4096	4096	Yes	No	Yes	Yes	Yes	No	355	382

Table 36: **Virtex-6 Device Resource Estimates**

4096	4096	Yes	No	Yes	Yes	Yes	Yes	350	416
4096	4096	Yes	Yes	No	Yes	No	No	320	353
4096	4096	Yes	Yes	No	Yes	No	Yes	387	438
4096	4096	Yes	Yes	No	Yes	Yes	No	453	515
4096	4096	Yes	Yes	No	Yes	Yes	Yes	481	565
4096	4096	Yes	Yes	Yes	No	No	No	344	381
4096	4096	Yes	Yes	Yes	No	No	Yes	366	428
4096	4096	Yes	Yes	Yes	No	Yes	No	395	424
4096	4096	Yes	Yes	Yes	No	Yes	Yes	432	474
4096	4096	Yes	Yes	Yes	Yes	No	No	485	539
4096	4096	Yes	Yes	Yes	Yes	No	Yes	520	586
4096	4096	Yes	Yes	Yes	Yes	Yes	No	599	615
4096	4096	Yes	Yes	Yes	Yes	Yes	Yes	594	665

Note: The Video Timing Controller does not utilize block RAMs or Xilinx XtremeDSP™ slices.

Performance

The following are typical clock frequencies for the target families. The maximum achievable clock frequency could vary and in most cases will be higher. The maximum achievable clock frequency and all resource counts may be affected by other tool options, additional logic in the FPGA device, using a different version of Xilinx tools, and other factors.

- Spartan-3A DSP: 150 MHz
- Spartan-6: 150 MHz
- Virtex-5: 225 MHz
- Virtex-6: 225 MHz

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

License Options

The Xilinx Video Timing Controller LogiCORE IP system provides three licensing options. After installing the required Xilinx ISE® software and IP Service Packs, choose a license option:

Simulation Only

The Simulation Only Evaluation license key is provided with the Xilinx CORE Generator tool. This key lets you assess the core functionality with either the provided example design or alongside your own design and demonstrates the various interfaces on the core in simulation. (Functional simulation is supported by a dynamically-generated HDL structural model.)

Full System Hardware Evaluation

The Full System Hardware Evaluation license is available at no cost and lets you fully integrate the core into an FPGA design, place-and-route the design, evaluate timing, and perform functional simulation of the Video Timing Controller core.

In addition, the license key lets you generate a bitstream from the placed and routed design, which can then be downloaded to a supported device and tested in hardware. The core can be tested in the target device for a limited time before timing out (ceasing to function), at which time it can be reactivated by reconfiguring the device.

Full

The Full license key is provided when you purchase the core and provides full access to all core functionality both in simulation and in hardware, including:

- Functional simulation support
- Back annotated gate-level simulation support
- Full implementation support including place and route and bitstream generation
- Full functionality in the programmed device with no time outs

Obtaining Your License Key

This section contains information about obtaining a simulation, full system hardware, and full license keys.

Simulation License

No action is required to obtain the Simulation Only Evaluation license key; it is provided by default with the Xilinx CORE Generator software.

Full System Hardware Evaluation License

To obtain a Full System Hardware Evaluation license:

1. Navigate to the product page for this core from:
   www.xilinx.com/products/ipcenter/EF-DI-VID-TIMING.htm
2. Click Evaluate.
3. Follow the instructions to install the required Xilinx ISE software and IP Service Packs.

Full License

To obtain a Full license key, you must purchase a license for the core. After doing so, click the "Access Core" link on the Xilinx.com IP core product page for further instructions.

Installing Your License File

The Simulation Only Evaluation license key is provided with the ISE CORE Generator system and does not require installation of an additional license file. For the Full System Hardware Evaluation license and the Full license, an email will be sent to you containing instructions for installing your license file. Additional details about IP license key installation can be found in the ISE Design Suite Installation, Licensing and Release Notes document.

Ordering Information

The Video Timing Controller v2.1 core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator system v12.3 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software. To order Xilinx software, please contact your local Xilinx sales representative. Information on additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
12/02/09	2.0	Update for core version 2.0.
09/21/10	3.0	Update for core version 2.1 and ISE 12.3.

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