LogiCORE IP Color Correction Matrix v5.00.a

Product Guide

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SECTION I: SUMMARY

IP Facts

Overview

Product Specification

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Introduction

The Xilinx LogiCORE™ IP Color Correction Matrix core is a 3 x 3 programmable coefficient matrix multiplier with offset compensation. This core can be used for color correction operations such as adjusting white balance, color cast, brightness, or contrast in an RGB image.

Features

- Programmable matrix coefficients
- Independent clipping and clamping control
- AXI4-Stream data interfaces
- Optional AXI4-Lite control interface
- Supports 8, 10, 12 and 16-bits per color component input and output
- Built-in, optional bypass and test-pattern generator mode
- Built-in, optional throughput monitors
- Supports spatial resolutions from 32x32 up to 7680x7680
  - Supports 1080P60 in all supported device families (1)
  - Supports 4kx2k @ 24 Hz in supported high performance devices

1. Performance on low power devices may be lower.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq-7000 (2), Artix-7, Virtex®-7, Kintex®-7, Virtex-6, Spartan®-6
Supported User Interfaces	AXI4-Lite, AXI4-Stream(3)
Resources	See Table 2-1 through Table 2-8.
Provided with Core	
Documentation	Product Guide
Design Files	ISE: NGC netlist, Encrypted HDL Vivado: Encrypted RTL
Example Design	Not Provided
Test Bench	Verilog (4)
Constraints File	Not Provided
Supported Software Drivers	Not Applicable
Simulation Models	VHDL or Verilog Structural, C-Model (4)
Tested Design Flows (5)	
Design Entry Tools	Integrated Software Environment (ISE), Vivado™ Design Suite (7), Platform Studio (XPS)
Simulation(6)	Mentor Graphics ModelSim, Xilinx® ISim
Synthesis Tools	Xilinx Synthesis Technology (XST) Vivado Synthesis (HLS)
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.
2. Supported in ISE Design Suite implementations only.
3. Video protocol as defined in the *Video IP: AXI Feature Adoption* section of UG761 AXI Reference Guide.
4. HDL test bench and C-Model available on the product page on Xilinx.com at http://www.xilinx.com/products/ipcenter/EF-DI-CCM.htm
5. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
6. For the supported versions of the tools, see the ISE Design Suite 14: Release Notes Guide.
7. Supports only 7 series devices.

Overview

There are many variations that cause difficulties in accurately reproducing color in imaging systems. These include:

- Spectral characteristics of the optics (lens, filters)
- Lighting source variations like daylight, fluorescent, or tungsten
- Characteristics of the color filters of the sensor

The Color Correction Matrix provides a method for correcting the image data for these variations. This fundamental block operates on either YUV or RGB data, and processing is "real-time" as a pre-processing hardware block.

As an example, following one of the three color channels through an imaging system from the original light source to the processed image helps understand the functionality of this core.

The blue color channel is a combination of the blue photons from the scene, multiplied by the relative response of the blue filter, multiplied by the relative response of the silicon to blue photons. However, the filter and silicon responses might be quite different from the response of the human eye, so blue to the sensor is quite different from blue to a human being.

This difference can be corrected and made to more closely match the blue that is acceptable to human vision. The Color Correction Matrix core multiplies the pixel values by some coefficient to strengthen or weaken it, creating an effective gain. At the same time a mixture of green or red can be added to the blue channel. To express this processing mathematically, the new blue (Bc) is related to the old blue (B), red (R), and green (G) according to:

$$Bc = K1 \times R + K2 \times G + K3 \times B$$

where K1, K2, and K3 are the weights for each of the mix of red, green, and blue to the new blue.

Extending this concept, a standard 3 x 3 matrix multiplication can be applied to each of the color channels in parallel simultaneously. This is a matrix operation where the weights define a color-correction matrix. In typical applications, color-correction also contains offset compensation to ensure black [0,0,0] levels are achieved.

$$\begin{bmatrix} R_c \\ G_c \\ B_c \end{bmatrix} = \begin{bmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} O_1 \\ O_2 \\ O_3 \end{bmatrix}$$

Equation 1-1

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix} + \begin{bmatrix} O_1 \\ O_2 \\ O_3 \end{bmatrix}$$

Equation 1-2

As shown in the matrix operation, the input pixels are transformed to a set of corrected output pixels. This can be a very useful function configured as a static application; however, the programmability of the coefficients and offset values allows this function to adapt to changing lighting conditions based on a separate control loop.

Feature Summary

The Color Correction Matrix core offers a 3x3 matrix multiplication for a variety of color correction applications. The coefficient matrix is fully programmable and includes offset compensation, and clipping and clamping of the output is also definable.

The core offers a processor interface for changing the matrix coefficients during run-time.

Applications

- Pre-processing block for image sensors
- Post-processing core for image data adjustment
- Video surveillance
- Video conferencing
- Machine vision

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite/ISE Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the Color Correction Matrix product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards Compliance

The Color Correction Matrix core is compliant with the AXI4-Stream Video Protocol and AXI4-Lite interconnect standards. Refer to the *Video IP: AXI Feature Adoption* section of the (UG761) *AXI Reference Guide* [Ref 1] for additional information.

Performance

The following sections detail the performance characteristics of the Color Correction Matrix core.

Maximum Frequencies

This section contains typical clock frequencies for the target devices. The maximum achievable clock frequency can vary. The maximum achievable clock frequency and all resource counts can be affected by other tool options, additional logic in the FPGA device, using a different version of Xilinx tools and other factors. Refer to in Table 2-1 through Table 2-8 for device-specific information.

Latency

The processing latency of the core is eight CLK cycles.

Throughput

The Color Correction Matrix core outputs one sample per clock cycle.

Resource Utilization

For an accurate measure of the usage of primitives, slices, and CLBs for a particular instance, check the **Display Core Viewer after Generation**.

Resource Utilization using Vivado Tools

The information presented in Table 2-1 through Table 2-3 is a guide to the resource utilization and maximum clock frequency of the Color Correction Matrix core for all input/output width combinations for Virtex-7, Kintex-7, Artix-7 FPGA families using Vivado tools. The Xtreme DSP Slice count is always 9, regardless of parameterization, and this core does not use any dedicated I/O or CLK resources. The design was tested with the AXI4-Lite interface, INTC_IF and the Debug Features disabled. By default, the maximum number of pixels per scan line was set to 1920, active pixels per scan line was set to 1920.

Table 2-1: **Kintex-7 (and Zynq-7000 Devices with Kintex Based Fabric)**

Input Data Width	Output Data Width	Slice Registers	Slice	LUT as Logic	LUT FF Pairs	DSPs	Clock Frequency (MHz)
8	8	224	86	190	260	9	256
	10	226	84	184	271	9	231
	12	244	98	197	294	9	280
	16	296	119	230	351	9	247
10	8	222	97	177	263	9	264
	10	256	102	201	292	9	272
	12	274	108	214	321	9	256
	16	294	111	217	342	9	264
12	8	236	93	179	272	9	256
	10	270	97	207	307	9	272
	12	288	113	216	330	9	256
	16	324	128	233	366	9	247
16	8	264	99	182	299	9	247
	10	282	97	197	312	9	280
	12	316	123	219	363	9	247
	16	352	141	237	394	9	256

Speedfile: XC7K70T-1 FBG484

Table 2-2: **Artix-7 (and Zynq-7000 devices with Artix Based Fabric)**

Input Data Width	Output Data Width	Slice Registers	Slice	LUT as Logic	LUT FF Pairs	DSPs	Clock Frequency (MHz)
8	8	208	87	176	259	9	182
	10	242	97	203	295	9	182
	12	244	89	196	296	9	182
	16	296	100	229	334	9	174
10	8	222	87	177	264	9	190
	10	256	105	200	300	9	190
	12	274	102	214	311	9	165
	16	294	120	217	348	9	182
12	8	252	97	195	291	9	182
	10	270	104	207	314	9	165
	12	272	96	201	308	9	190
	16	324	120	234	360	9	190
16	8	280	118	199	325	9	182
	10	298	116	210	335	9	182
	12	300	118	206	343	9	182
	16	352	133	238	394	9	174

Speedfile: XC7A100T-1 FF484

Table 2-3: **Virtex-7**

Input Data Width	Output Data Width	Slice Registers	Slice	LUT as Logic	LUT FF Pairs	DSPs	Clock Frequency (MHz)
8	8	208	82	176	255	9	263
	10	226	98	184	284	9	263
	12	260	99	212	312	9	268
	16	280	114	216	328	9	294
10	8	222	82	176	258	9	243
	10	256	108	201	298	9	253
	12	274	110	213	324	9	243
	16	294	113	218	344	9	284
12	8	236	96	177	283	9	253
	10	254	99	189	290	9	243
	12	272	95	201	314	9	268
	16	324	121	233	370	9	263

Table 2-3: **Virtex-7 *(Cont'd)***

Input Data Width	Output Data Width	Slice Registers	Slice	LUT as Logic	LUT FF Pairs	DSPs	Clock Frequency (MHz)
16	8	280	116	198	316	9	274
	10	282	110	196	321	9	274
	12	300	110	205	339	9	284
	16	352	122	237	391	9	253

Speedfile: XC7VX585T-1 FFG1157

Resource Utilization using ISE Tools

The information presented in Table 2-4 through Table 2-8 is a guide to the resource utilization and maximum clock frequency of the Color Correction Matrix core for all input/output width combinations for Virtex-7, Kintex-7, Artix-7, Zynq-7000, Virtex-6, and Spartan-6 FPGA families using ISE. The Xtreme DSP Slice count is always 9, regardless of parameterization, and this core does not use any dedicated I/O or CLK resources. The design was tested using ISE® v14.2 tools with default tool options for characterization data. The design was tested with the AXI4-Lite interface, `INTC_IF` and the Debug Features disabled. By default, the maximum number of pixels per scan line was set to 1920, active pixels per scan line was set to 1920.

Table 2-4: **Kintex-7 (and Zynq-7000 Devices with Kintex Based Fabric)**

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
8	8	212	292	346	0	0	9	321
	10	195	283	333	0	0	9	297
	12	213	311	348	0	0	9	288
	16	195	308	349	0	0	9	305
10	8	208	294	330	0	0	9	288
	10	209	299	335	0	0	9	297
	12	227	319	358	0	0	9	288
	16	209	306	368	0	0	9	297
12	8	240	310	363	0	0	9	305
	10	223	311	348	0	0	9	297
	12	223	307	368	0	0	9	288
	16	241	326	401	0	0	9	297

Table 2-4: **Kintex-7 (and Zynq-7000 Devices with Kintex Based Fabric) *(Cont'd)***

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
16	8	250	311	376	0	0	9	305
	10	269	323	406	0	0	9	288
	12	251	312	400	0	0	9	288
	16	251	325	411	0	0	9	297

Speedfile: XC7K70T-1 FBG484

Table 2-5: **Artix-7 (and Zynq-7000 devices with Artix Based Fabric)**

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
8	8	210	297	352	0	0	9	198
	10	195	282	330	0	0	9	206
	12	195	285	335	0	0	9	198
	16	211	319	377	0	0	9	206
10	8	224	307	358	0	0	9	198
	10	225	311	367	0	0	9	198
	12	225	317	372	0	0	9	215
	16	209	302	356	0	0	9	198
12	8	222	291	348	0	0	9	198
	10	239	320	377	0	0	9	198
	12	223	298	363	0	0	9	206
	16	239	334	403	0	0	9	206
16	8	266	326	403	0	0	9	215
	10	251	309	382	0	0	9	215
	12	251	319	384	0	0	9	206
	16	251	322	400	0	0	9	198

Speedfile: XC7A100T-1 FF484

Table 2-6: **Virtex-7**

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
8	8	212	298	339	0	0	9	304
	10	195	296	325	0	0	9	314
	12	195	297	335	0	0	9	304
	16	213	325	363	0	0	9	294
10	8	208	288	338	0	0	9	314
	10	227	313	349	0	0	9	294
	12	227	319	358	0	0	9	314
	16	209	306	368	0	0	9	294
12	8	240	304	368	0	0	9	294
	10	223	303	358	0	0	9	294
	12	241	318	380	0	0	9	304
	16	223	321	375	0	0	9	314
16	8	268	322	387	0	0	9	294
	10	251	313	401	0	0	9	304
	12	251	313	401	0	0	9	304
	16	269	339	428	0	0	9	294

Speedfile: XC7VX585T-1 FFG1157

Table 2-7: **Virtex-6**

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
8	8	194	274	318	0	0	9	262
	10	211	287	340	0	0	9	285
	12	195	282	333	0	0	9	277
	16	195	297	339	0	0	9	277
10	8	208	272	332	0	0	9	285
	10	209	277	335	0	0	9	277
	12	225	303	353	0	0	9	277
	16	209	303	353	0	0	9	262
12	8	222	282	349	0	0	9	270
	10	239	299	364	0	0	9	262
	12	239	308	373	0	0	9	262
	16	223	304	376	0	0	9	262

Table 2-7: **Virtex-6 *(Cont'd)***

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
16	8	266	306	388	0	0	9	270
	10	267	320	386	0	0	9	285
	12	267	321	398	0	0	9	277
	16	267	331	410	0	0	9	277

Speedfile: XC6VLX75T-1 FF484

Table 2-8: **Spartan-6**

Input Width	Output Width	Slice Registers	Slice LUTs	LUT6-FF Pairs	RAMB16BWER	RAMB8BWER	DSP48A1s	Clock Frequency (MHz)
8	8	201	315	369	0	0	9	185
	10	220	340	372	0	0	9	175
	12	220	341	384	0	0	9	175
	16	203	343	392	0	0	9	175
10	8	233	332	389	0	0	9	175
	10	217	329	381	0	0	9	185
	12	217	332	392	0	0	9	175
	16	234	357	409	0	0	9	175
12	8	229	331	392	0	0	9	175
	10	248	349	408	0	0	9	175
	12	231	346	402	0	0	9	144
	16	248	359	432	0	0	9	175
16	8	257	338	429	0	0	9	175
	10	276	357	436	0	0	9	175
	12	276	370	438	0	0	9	175
	16	259	368	444	0	0	9	164

Speedfile: XC6SLX25-2 FGG484

Core Interfaces and Register Space

Port Descriptions

The Color Correction Matrix core uses industry standard control and data interfaces to connect to other system components. The following sections describe the various interfaces

available with the core. Figure 2-1 illustrates an I/O diagram of the CCM core. Some signals are optional and not present for all configurations of the core. The AXI4-Lite interface and the IRQ pin are present only when the core is configured via the GUI with an AXI4-Lite control interface. The INTC_IF interface is present only when the core is configured via the GUI with the INTC interface enabled.

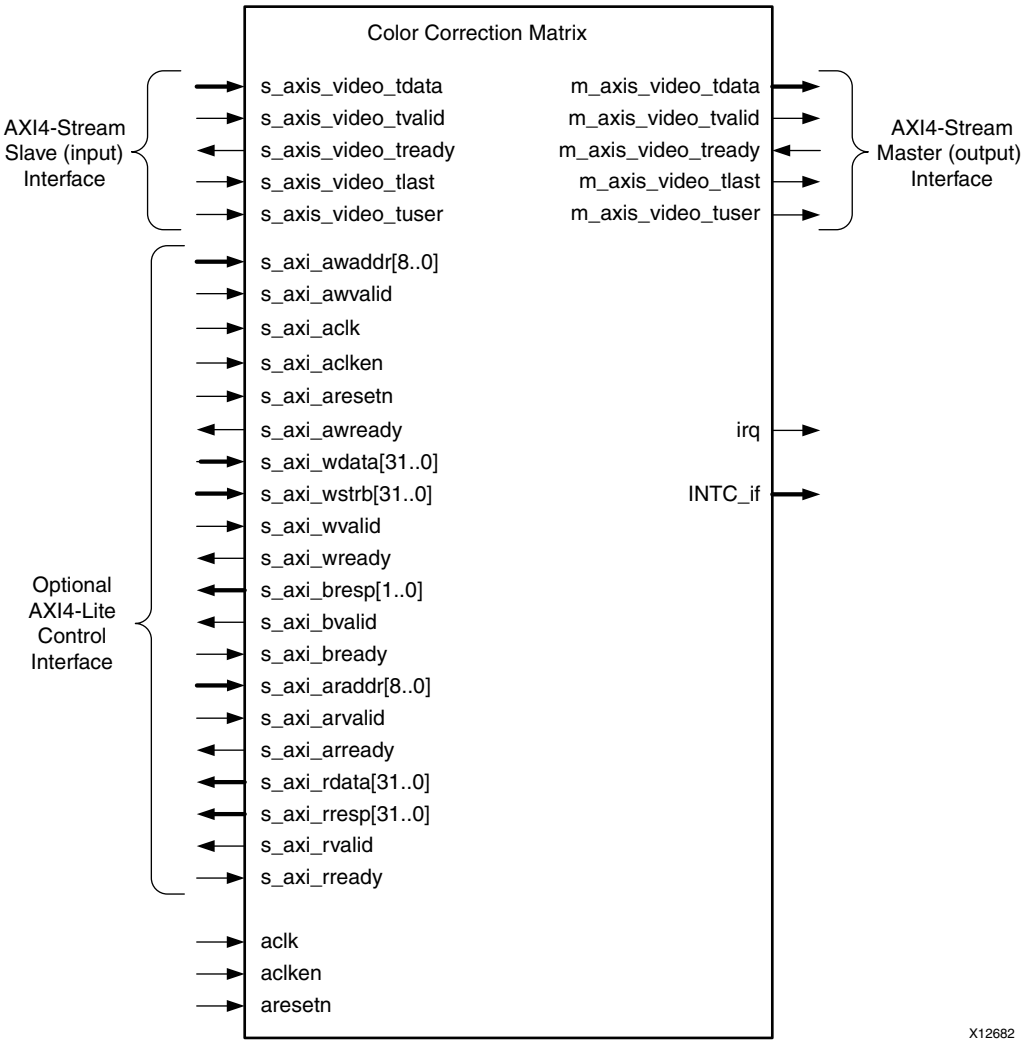

Figure 2-1: **CCM Core Top-Level Signaling Interface**

Common Interface Signals

Table 2-9 summarizes the signals which are either shared by, or not part of the dedicated AXI4-Stream data or AXI4-Lite control interfaces.

Table 2-9: **Common Interface Signals**

Signal Name	Direction	Width	Description
ACLK	In	1	Video Core Clock
ACLKEN	In	1	Video Core Active High Clock Enable

Table 2-9: **Common Interface Signals**

Signal Name	Direction	Width	Description
ARESETn	In	1	Video Core Active Low Synchronous Reset
INTC_IF	Out	6	Optional External Interrupt Controller Interface. Available only when INTC_IF is selected on GUI.
IRQ	Out	1	Optional Interrupt Request Pin. Available only when AXI4-Liter interface is selected on GUI.

The ACLK, ACLKEN and ARESETn signals are shared between the core and the AXI4-Stream data interfaces. The AXI4-Lite control interface has its own set of clock, clock enable and reset pins: S_AXI_ACLK, S_AXI_ACLKEN and S_AXI_ARESETn. Refer to The Interrupt Subsystem for a description of the INTC_IF and IRQ pins.

ACLK

The AXI4-Stream interface must be synchronous to the core clock signal ACLK. All AXI4-Stream interface input signals are sampled on the rising edge of ACLK. All AXI4-Stream output signal changes occur after the rising edge of ACLK. The AXI4-Lite interface is unaffected by the ACLK signal.

ACLKEN

The ACLKEN pin is an active-high, synchronous clock-enable input pertaining to AXI4-Stream interfaces. Setting ACLKEN low (de-asserted) halts the operation of the core despite rising edges on the ACLK pin. Internal states are maintained, and output signal levels are held until ACLKEN is asserted again. When ACLKEN is de-asserted, core inputs are not sampled, except ARESETn, which supersedes ACLKEN. The AXI4-Lite interface is unaffected by the ACLKEN signal.

ARESETn

The ARESETn pin is an active-low, synchronous reset input pertaining to only AXI4-Stream interfaces. ARESETn supersedes ACLKEN, and when set to 0, the core resets at the next rising edge of ACLK even if ACLKEN is de-asserted. The ARESETn signal must be synchronous to the ACLK and must be held low for a minimum of 32 clock cycles of the slowest clock. The AXI4-Lite interface is unaffected by the ARESETn signal.

Data Interface

The CCM core receives and transmits data using AXI4-Stream interfaces that implement a video protocol as defined in the *Video IP: AXI Feature Adoption* section of the (UG761) *AXI Reference Guide* [Ref 1].

AXI4-Stream Signal Names and Descriptions

Table 2-10 describes the AXI4-Stream signal names and descriptions.

Table 2-10: **AXI4-Stream Data Interface Signal Descriptions**

Signal Name	Direction	Width	Description
s_axis_video_tdata	In	24,32,40,48	Input Video Data
s_axis_video_tvalid	In	1	Input Video Valid Signal
s_axis_video_tready	Out	1	Input Ready
s_axis_video_tuser	In	1	Input Video Start Of Frame
s_axis_video_tlast	In	1	Input Video End Of Line
m_axis_video_tdata	Out	24,32,40,48	Output Video Data
m_axis_video_tvalid	Out	1	Output Valid
m_axis_video_tready	In	1	Output Ready
m_axis_video_tuser	Out	1	Output Video Start Of Frame
m_axis_video_tlast	Out	1	Output Video End Of Line

Video Data

The AXI4-Stream interface specification restricts TDATA widths to integer multiples of 8 bits. Therefore, 10, 12, and 16 bit image data must be padded with zeros on the MSB to form an integer that is a multiple of 8 bits wide vector before connecting to s_axis_video_tdata. Padding does not affect the size of the core.

For example, when using RGB video, the RGB data on the CCM output m_axis_video_tdata is packed and padded to multiples of 8 bits as necessary, as shown for the RGB case in Figure 2-2. Zero padding the most significant bits is only necessary for 10, 12, and 16 bit wide data.

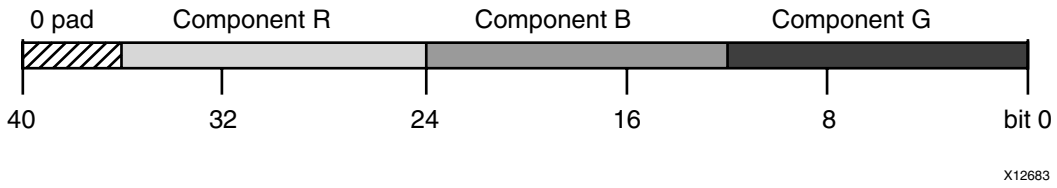

Figure 2-2: **RGB Data Encoding on m_axis_video_tdata**

READY/VALID Handshake

A valid transfer occurs whenever READY, VALID, ACLKEN, and ARESETn are high at the rising edge of ACLK, as seen in Figure 2-3. During valid transfers, DATA only carries active video data. Blank periods and ancillary data packets are not transferred via the AXI4-Stream video protocol.

Guidelines on Driving s_axis_video_tvalid

Once s_axis_video_tvalid is asserted, no interface signals (except the CCM core driving s_axis_video_tready) may change values until the transaction completes (s_axis_video_tready, s_axis_video_tvalid, ACLKEN high on the rising edge of ACLK). Once asserted, s_axis_video_tvalid may only be de-asserted after a transaction has completed. Transactions may not be retracted or aborted. In any cycle following a transaction, s_axis_video_tvalid can either be de-asserted or remain asserted to initiate a new transfer.

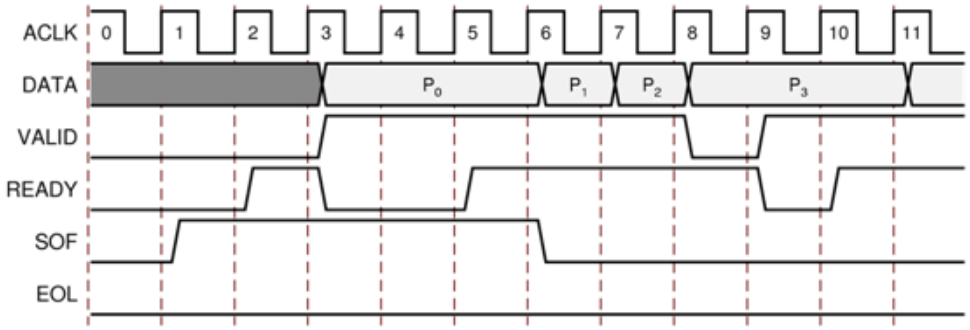

Figure 2-3: **Example of READY/VALID Handshake, Start of a New Frame**

Guidelines on Driving m_axis_video_tready

The m_axis_video_tready signal may be asserted before, during or after the cycle in which the CCM core asserted m_axis_video_tvalid. The assertion of m_axis_video_tready may be dependent on the value of m_axis_video_tvalid. A slave that can immediately accept data qualified by m_axis_video_tvalid, should pre-assert its m_axis_video_tready signal until data is received. Alternatively, m_axis_video_tready can be registered and driven the cycle following VALID assertion. It is recommended that the AXI4-Stream slave should drive READY independently, or pre-assert READY to minimize latency.

Start of Frame Signals - m_axis_video_tuser0, s_axis_video_tuser0

The Start-Of-Frame (SOF) signal, physically transmitted over the AXI4-Stream TUSER0 signal, marks the first pixel of a video frame. The SOF pulse is 1 valid transaction wide, and must coincide with the first pixel of the frame, as seen in Figure 2-3. SOF serves as a frame synchronization signal, which allows downstream cores to re-initialize, and detect the first pixel of a frame. The SOF signal may be asserted an arbitrary number of ACLK cycles before the first pixel value is presented on DATA, as long as a VALID is not asserted.

End of Line Signals - m_axis_video_tlast, s_axis_video_tlast

The End-Of-Line signal, physically transmitted over the AXI4-Stream TLAST signal, marks the last pixel of a line. The EOL pulse is 1 valid transaction wide, and must coincide with the last pixel of a scan-line, as seen in Figure 2-4.

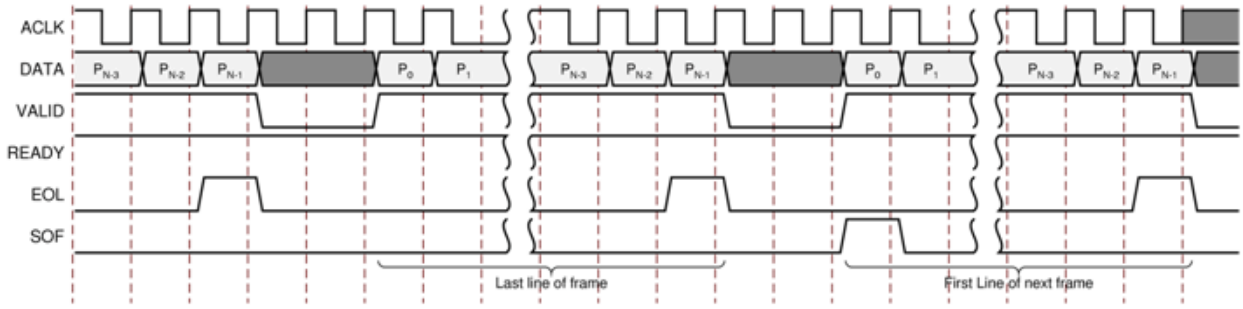

Figure 2-4: **Use of EOL and SOF Signals**

Control Interface

When configuring the core, the user has the option to add an AXI4-Lite register interface to dynamically control the behavior of the core. The AXI4-Lite slave interface facilitates integrating the core into a processor system, or along with other video or AXI4-Lite compliant IP, connected via AXI4-Lite interface to an AXI4-Lite master. In a static configuration with a fixed set of parameters (constant configuration), the core can be instantiated without the AXI4-Lite control interface, which reduces the core Slice footprint.

Constant Configuration

The constant configuration caters to those who uses the CCM core in a single setup that does not need to change. In constant configuration, the image resolution, matrix coefficients, offsets and clip/clamp values are hard coded into the core via the CCM core GUI. Since there is no AXI4-Lite interface, the core is not programmable, but can be reset, enabled, or disabled using the ARESETn and ACLKEN ports.

AXI4-Lite Interface

The AXI4-Lite interface allows a user to dynamically control parameters within the core. Core configuration can be accomplished using an AXI4-Stream master state machine, or an embedded ARM or soft system processor such as MicroBlaze.

The CCM core can be controlled via the AXI4-Lite interface using read and write transactions to the CCM register space.

Table 2-11: **AXI4-Lite Interface Signals**

Signal Name	Direction	Width	Description
s_axi_aclk	In	1	AXI4-Lite clock
s_axi_aclken	In	1	AXI4-Lite clock enable
s_axi_aresetn	In	1	AXI4-Lite synchronous Active Low reset
s_axi_awvalid	In	1	AXI4-Lite Write Address Channel Write Address Valid.
s_axi_awread	Out	1	AXI4-Lite Write Address Channel Write Address Ready. Indicates DMA ready to accept the write address.
s_axi_awaddr	In	32	AXI4-Lite Write Address Bus
s_axi_wvalid	In	1	AXI4-Lite Write Data Channel Write Data Valid.
s_axi_wready	Out	1	AXI4-Lite Write Data Channel Write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_wdata	In	32	AXI4-Lite Write Data Bus
s_axi_bresp	Out	2	AXI4-Lite Write Response Channel. Indicates results of the write transfer.
s_axi_bvalid	Out	1	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid.
s_axi_bready	In	1	AXI4-Lite Write Response Channel Ready. Indicates target is ready to receive response.
s_axi_arvalid	In	1	AXI4-Lite Read Address Channel Read Address Valid
s_axi_arready	Out	1	Ready. Indicates DMA is ready to accept the read address.
s_axi_araddr	In	32	AXI4-Lite Read Address Bus
s_axi_rvalid	Out	1	AXI4-Lite Read Data Channel Read Data Valid
s_axi_rready	In	1	AXI4-Lite Read Data Channel Read Data Ready. Indicates target is ready to accept the read data.
s_axi_rdata	Out	32	AXI4-Lite Read Data Bus
s_axi_rresp	Out	2	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer.

S_AXI_ACLK

The AXI4-Lite interface must be synchronous to the S_AXI_ACLK clock signal. The AXI4-Lite interface input signals are sampled on the rising edge of ACLK. The AXI4-Lite output signal changes occur after the rising edge of ACLK. The AXI4-Stream interfaces signals are not affected by the S_AXI_ACLK.

S_AXI_ACLKEN

The S_AXI_ACLKEN pin is an active-high, synchronous clock-enable input for the AXI4-Lite interface. Setting S_AXI_ACLKEN low (de-asserted) halts the operation of the AXI4-Lite interface despite rising edges on the S_AXI_ACLK pin. AXI4-Lite interface states are maintained, and AXI4-Lite interface output signal levels are held until S_AXI_ACLKEN is

asserted again. When S_AXI_ACLKEN is de-asserted, AXI4-Lite interface inputs are not sampled, except S_AXI_ARESETn, which supersedes S_AXI_ACLKEN. The AXI4-Stream interfaces signals are not affected by the S_AXI_ACLKEN.

S_AXI_ARESETn

The S_AXI_ARESETn pin is an active-low, synchronous reset input for the AXI4-Lite interface. S_AXI_ARESETn supersedes S_AXI_ACLKEN, and when set to 0, the core resets at the next rising edge of S_AXI_ACLK even if S_AXI_ACLKEN is de-asserted. The S_AXI_ARESETn signal must be synchronous to the S_AXI_ACLK and must be held low for a minimum of 32 clock cycles of the slowest clock. The S_AXI_ARESETn input is resynchronized to the ACLK clock domain. The AXI4-Stream interfaces and core signals are also reset by S_AXI_ARESETn.

Register Space

The standardized Xilinx Video IP register space is partitioned to control-, timing-, and core specific registers. The CCM core uses only one timing related register, ACTIVE_SIZE (0x0020), which allows specifying the input frame dimensions. The core has 14 core-specific registers for setting the matrix coefficients, the offsets and clip/clamp values.

Table 2-12: **Register Names and Descriptions**

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register Description
0x0000	CONTROL	R/W	N	Power-on-Reset : 0x0	Bit 0: SW_ENABLE Bit 1: REG_UPDATE Bit 4: BYPASS(1) Bit 5: TEST_PATTERN(1) Bit 30: FRAME_SYNC_RESET (1: reset) Bit 31: SW_RESET (1: reset)
0x0004	STATUS	R/W	No	0	Bit 0: PROC_STARTED Bit 1: EOF Bit 16: SLAVE_ERROR
0x0008	ERROR	R/W	No	0	Bit 0: SLAVE_EOL_EARLY Bit 1: SLAVE_EOL_LATE Bit 2: SLAVE_SOF_EARLY Bit 3: SLAVE_SOF_LATE
0x000C	IRQ_ENABLE	R/W	No	0	16-0: Interrupt enable bits corresponding to STATUS bits

Table 2-12: **Register Names and Descriptions *(Cont'd)***

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register Description
0x0010	VERSION	R	N/A	0x0500a000	7-0: REVISION_NUMBER 11-8: PATCH_ID 15-12: VERSION_REVISION 23-16: VERSION_MINOR 31-24: VERSION_MAJOR
0x0014	SYSDEBUG0	R	N/A	0	0-31: Frame Throughput monitor(1)
0x0018	SYSDEBUG1	R	N/A	0	0-31: Line Throughput monitor(1)
0x001C	SYSDEBUG2	R	N/A	0	0-31: Pixel Throughput monitor(1)
0x0020	ACTIVE_SIZE	R/W	Yes	Specified via GUI	12-0: Number of Active Pixels per Scanline 28-16: Number of Active Lines per Frame
0x0100	K11	R/W	Yes	Specified via GUI	17:0 - real numbers in the [-4 : 4] range, multiplied by 32768
0x0104	K12	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x0108	K13	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x010C	K21	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x0110	K22	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x0114	K23	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x0118	K31	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x011C	K32	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x0120	K33	R/W	Yes	Specified via GUI	17-0: Matrix Coefficient Real numbers in the [-4 : 4] range, multiplied by 32768
0x0124	ROFFSET	R/W	Yes	Specified via GUI	16-0: Red Offset [-2Out_Data_Width : 2Out_Data_Width-1]

Table 2-12: **Register Names and Descriptions *(Cont'd)***

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register Description
0x0128	GOFFSET	R/W	Yes	Specified via GUI	16-0: Green Offset [-2Out_Data_Width : 2Out_Data_Width-1]
0x012C	BOFFSET	R/W	Yes	Specified via GUI	16-0: Blue Offset [-2Out_Data_Width : 2Out_Data_Width-1]
0x0130	CLIP	R/W	Yes	Specified via GUI	15-0: Maximum Output [0 : 2Out_Data_Width-1]
0x0134	CLAMP	R/W	Yes	Specified via GUI	15-0: Minimum Output [0 : 2Out_Data_Width-1]

1. Only available when the debugging features option is enabled in the GUI at the time the core is instantiated.

CONTROL (0x0000) Register

Bit 0 of the CONTROL register, SW_ENABLE, facilitates enabling and disabling the core from software. Writing '0' to this bit effectively disables the core halting further operations, which blocks the propagation of all video signals. After Power up, or Global Reset, the SW_ENABLE defaults to 0 for the AXI4-Lite interface. Similar to the ACLKEN pin, the SW_ENABLE flag is not synchronized with the AXI4-Stream interfaces: Enabling or Disabling the core takes effect immediately, irrespective of the core processing status. Disabling the core for extended periods may lead to image tearing.

Bit 1 of the CONTROL register, REG_UPDATE is a write done semaphore for the host processor, which facilitates committing all user and timing register updates simultaneously. The CCM core ACTIVE_SIZE and BAYER_PHASE registers are double buffered. One set of registers (the processor registers) is directly accessed by the processor interface, while the other set (the active set) is actively used by the core. New values written to the processor registers get copied over to the active set at the end of the AXI4-Stream frame, if and only if REG_UPDATE is set. Setting REG_UPDATE to 0 before updating multiple register values, then setting REG_UPDATE to 1 when updates are completed ensures all registers are updated simultaneously at the frame boundary without causing image tearing.

Bit 4 of the CONTROL register, BYPASS, switches the core to bypass mode if debug features are enabled. In bypass mode the CCM core processing function is bypassed, and the core repeats AXI4-Stream input samples on its output. Refer to Debugging Features in Appendix C for more information. If debug features were not included at instantiation, this flag has no effect on the operation of the core. Switching bypass mode on or off is not synchronized to frame processing, therefore can lead to image tearing.

Bit 5 of the CONTROL register, TEST_PATTERN, switches the core to test-pattern generator mode if debug features are enabled. Refer to Debugging Features in Appendix C for more information. If debug features were not included at instantiation, this flag has no effect on

the operation of the core. Switching test-pattern generator mode on or off is not synchronized to frame processing, therefore can lead to image tearing.

Bits 30 and 31 of the CONTROL register, FRAME_SYNC_RESET and SW_RESET facilitate software reset. Setting SW_RESET reinitializes the core to GUI default values, all internal registers and outputs are cleared and held at initial values until SW_RESET is set to 0. The SW_RESET flag is not synchronized with the AXI4-Stream interfaces. Resetting the core while frame processing is in progress causes image tearing. For applications where the soft-ware reset functionality is desirable, but image tearing has to be avoided a frame synchronized software reset (FRAME_SYNC_RESET) is available. Setting FRAME_SYNC_RESET to 1 resets the core at the end of the frame being processed, or immediately if the core is between frames when the FRAME_SYNC_RESET was asserted. After reset, the FRAME_SYNC_RESET bit is automatically cleared, so the core can get ready to process the next frame of video as soon as possible. The default value of both RESET bits is 0. Core instances with no AXI4-Lite control interface can only be reset via the ARESETn pin.

STATUS (0x0004) Register

All bits of the STATUS register can be used to request an interrupt from the host processor. To facilitate identification of the interrupt source, bits of the STATUS register remain set after an event associated with the particular STATUS register bit, even if the event condition is not present at the time the interrupt is serviced.

Bits of the STATUS register can be cleared individually by writing '1' to the bit position to be cleared.

Bit 0 of the STATUS register, PROC_STARTED, indicates that processing of a frame has commenced via the AXI4-Stream interface.

Bit 1 of the STATUS register, End-of-frame (EOF), indicates that the processing of a frame has completed.

Bit 16 of the STATUS register, SLAVE_ERROR, indicates that one of the conditions monitored by the ERROR register has occurred.

ERROR (0x0008) Register

Bit 16 of the STATUS register, SLAVE_ERROR, indicates that one of the conditions monitored by the ERROR register has occurred. This bit can be used to request an interrupt from the host processor. To facilitate identification of the interrupt source, bits of the STATUS and ERROR registers remain set after an event associated with the particular ERROR register bit, even if the event condition is not present at the time the interrupt is serviced.

Bits of the ERROR register can be cleared individually by writing '1' to the bit position to be cleared.

Bit 0 of the ERROR register, EOL_EARLY, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the latest and the preceding End-Of-Line (EOL) signal was less than the value programmed into the ACTIVE_SIZE register.

Bit 1 of the ERROR register, EOL_LATE, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the last EOL signal surpassed the value programmed into the ACTIVE_SIZE register.

Bit 2 of the ERROR register, SOF_EARLY, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the latest and the preceding Start-Of-Frame (SOF) signal was less than the value programmed into the ACTIVE_SIZE register.

Bit 3 of the ERROR register, SOF_LATE, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the last SOF signal surpassed the value programmed into the ACTIVE_SIZE register.

IRQ_ENABLE (0x000C) Register

Any bits of the STATUS register can generate a host-processor interrupt request via the IRQ pin. The Interrupt Enable register facilitates selecting which bits of STATUS register asserts IRQ. Bits of the STATUS registers are masked by (AND) corresponding bits of the IRQ_ENABLE register and the resulting terms are combined (OR) together to generate IRQ.

Version (0x0010) Register

Bit fields of the Version Register facilitate software identification of the exact version of the hardware peripheral incorporated into a system. The core driver can take advantage of this Read-Only value to verify that the software is matched to the correct version of the hardware. Refer to Table 2-12 for more information.

SYSDEBUG0 (0x0014) Register

The SYSDEBUG0, or Frame Throughput Monitor, register indicates the number of frames processed since power-up or the last time the core was reset. The SYSDEBUG registers can be useful to identify external memory / Frame buffer / or throughput bottlenecks in a video system. Refer to Debugging Features in Appendix C for more information.

SYSDEBUG1 (0x0018) Register

The SYSDEBUG1, or Line Throughput Monitor, register indicates the number of lines processed since power-up or the last time the core was reset. The SYSDEBUG registers can be useful to identify external memory / Frame buffer / or throughput bottlenecks in a video system. Refer to Debugging Features in Appendix C for more information.

SYSDEBUG2 (0x001C) Register

The SYSDEBUG2, or Pixel Throughput Monitor, register indicates the number of pixels processed since power-up or the last time the core was reset. The SYSDEBUG registers can be useful to identify external memory / Frame buffer / or throughput bottlenecks in a video system. Refer to Debugging Features in Appendix C for more information.

ACTIVE_SIZE (0x0020) Register

The ACTIVE_SIZE register encodes the number of active pixels per scan line and the number of active scan lines per frame. The lower half-word (bits 12:0) encodes the number of active pixels per scan line. Supported values are between 32 and the value provided in the **Maximum number of pixels per scan line** field in the GUI. The upper half-word (bits 28:16) encodes the number of active lines per frame. Supported values are 32 to 7680. To avoid processing errors, the user should restrict values written to ACTIVE_SIZE to the range supported by the core instance.

K11 - K33 (0x0100 - 0x0120) Registers

The K11 - K33 registers hold the matrix coefficients shown in Equation 1-1 and Equation 1-2. The coefficients are presented in 18.15 fixed point format. The 18-bit signed integer values are equivalent to real numbers in the [-4 : 4] range, multiplied by 32768.

ROFFSET (0x0124) Register

The ROFFSET register holds the O1 offset value shown in Equation1-1 and Equation 1-2. The offset value has a width of the output data width plus 1. It is a signed integer with a range of [-2Out_Data_Width : 2Out_Data_Width-1].

GOFFSET (0x0128) Register

The GOFFSET register holds the O2 offset value shown in Equation1-1 and Equation 1-2. The offset value has a width of the output data width plus 1. It is a signed integer with a range of [-2Out_Data_Width : 2Out_Data_Width-1].

BOFFSET (0x012C) Register

The BOFFSET register holds the O3 offset value shown in Equation1-1 and Equation 1-2. The offset value has a width of the output data width plus 1. It is a signed integer with a range of [-2Out_Data_Width : 2Out_Data_Width-1].

Clip (0x0130) Register

The Clip register holds the maximum output data value. Output values greater than this value is replaced with this value. The Clip value has the same width as the output data width. It is an unsigned integer with a range of [0 : 2Out_Data_Width-1].

Clamp (0x0134) Register

The Clamp register holds the minimum output data value. Output values smaller than this value is replaced with this value. The Clamp value has the same width as the output data width. It is an unsigned integer with a range of `[0 : 2Out_Data_Width-1]`.

The Interrupt Subsystem

`STATUS` register bits can trigger interrupts so embedded application developers can quickly identify faulty interfaces or incorrectly parameterized cores in a video system. Irrespective of whether the AXI4-Lite control interface is present or not, the CCM core detects AXI4-Stream framing errors, as well as the beginning and the end of frame processing.

When the core is instantiated with an AXI4-Lite Control interface, the optional interrupt request pin (`IRQ`) is present. Events associated with bits of the `STATUS` register can generate a (level triggered) interrupt, if the corresponding bits of the interrupt enable register (`IRQ_ENABLE`) are set. Once set by the corresponding event, bits of the `STATUS` register stay set until the user application clears them by writing '1' to the desired bit positions. Using this mechanism the system processor can identify and clear the interrupt source.

Without the AXI4-Lite interface the user can still benefit from the core signaling error and status events. By selecting the **Enable INTC Port** check-box on the GUI, the core generates the optional `INTC_IF` port. This vector of signals gives parallel access to the individual interrupt sources, as seen in Table 2-13.

Unlike `STATUS` and `ERROR` flags, `INTC_IF` signals are not held, rather stay asserted only while the corresponding event persists.

Table 2-13: **INTC_IF Signal Functions**

INTC_IF signal	Function
0	Frame processing start
1	Frame processing complete
2	Reserved
3	Reserved
4	Video over AXI4-Stream Error
5	EOL Early
6	EOL Late
7	SOF Early
8	SOF Late

In a system integration tool, such as EDK, the interrupt controller INTC IP can be used to register the selected `INTC_IF` signals as edge triggered interrupt sources. The INTC IP

provides functionality to mask (enable or disable), as well as identify individual interrupt sources from software. Alternatively, for an external processor or MCU the user can custom build a priority interrupt controller to aggregate interrupt requests and identify interrupt sources.

Designing with the Core

General Design Guidelines

The Color Correction Matrix core is a 3x3 matrix multiplication with an additional offset.

The output values are:

$$Rc = K11 \times R + KK12 \times G + K13 \times B + O1$$

$$Gc = K21 \times R + K22x\ G + K33 \times B + O2$$

$$Bc = K31 \times R + K32x\ G + K33 \times B + O3$$

In cases where the Input Data Width does not equal the Output Data Width, the data is scaled up or down accordingly. For example, if the Input Data Width =8, and Output Data Width=12, then the core scales the data up by a factor of 4. Meaning, with an identity matrix, an input of 1 gives an output of 4.

The core processes samples provided via an AXI4-Stream slave interface, outputs pixels via an AXI4-Stream master interface, and can be controlled via an optional AXI4-Lite interface. It is recommended that the CCM core is used in conjunction with the Video In to AXI4-Stream and Video Timing Controller cores. The Video Timing Controller core measures the timing parameters, such as number of active scan lines, number of active pixels per scan line of the image sensor. The Video In to AXI4-Stream core formats the input video to the AXI4-Stream interface

Typically, the CCM core is part of a larger system such as an Image Sensor Pipeline (ISP) system shown in Figure 3-1.

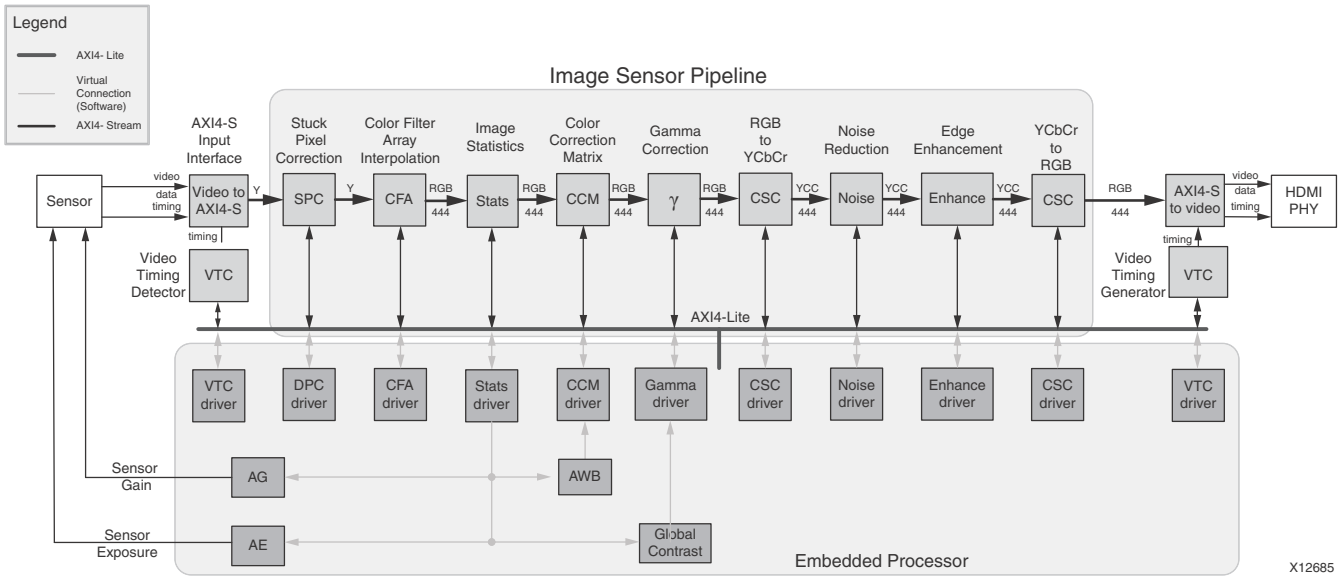

Figure 3-1: **Image Sensor Pipeline System with CCM Core**

Clock, Enable, and Reset Considerations

ACLK

The master and slave AXI4-Stream video interfaces use the ACLK clock signal as their shared clock reference, as shown in Figure 3-2.

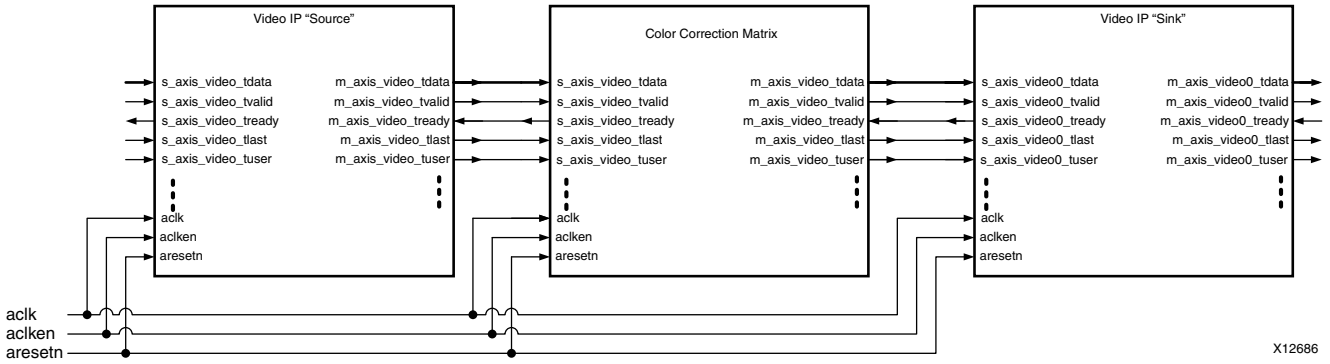

Figure 3-2: **Example of ACLK Routing in an ISP Processing Pipeline**

S_AXI_ACLK

The AXI4-Lite interface uses the A_AXI_ACLK pin as its clock source. The ACLK pin is not shared between the AXI4-Lite and AXI4-Stream interfaces. The CCM core contains clock-domain crossing logic between the ACLK (AXI4-Stream and Video Processing) and S_AXI_ACLK (AXI4-Lite) clock domains. The core automatically ensures that the AXI4-Lite

transactions complete even if the video processing is stalled with ARESETn, ACLKEN or with the video clock not running.

ACLKEN

The CCM core has two enable options: the ACLKEN pin (hardware clock enable), and the software reset option provided via the AXI4-Lite control interface (when present).

ACLKEN is by no means synchronized internally to AXI4-Stream frame processing therefore de-asserting ACLKEN for extended periods of time may lead to image tearing.

The ACLKEN pin facilitates:

- Multi-cycle path designs (high speed clock division without clock gating),
- Standby operation of subsystems to save on power
- Hardware controlled bring-up of system components

Note: When ACLKEN (clock enable) pins are used (toggled) in conjunction with a common clock source driving the master and slave sides of an AXI4-Stream interface, to prevent transaction errors the ACLKEN pins associated with the master and slave component interfaces must also be driven by the same signal (Figure 2-2).

Note: When two cores connected via AXI4-Stream interfaces, where only the master or the slave interface has an ACLKEN port, which is not permanently tied high, the two interfaces should be connected via the AXI4-Stream Interconnect or AXI-FIFO cores to avoid data corruption (Figure 2-3).

S_AXI_ACLKEN

The S_AXI_ACLKEN is the clock enable signal for the AXI4-Lite interface only. Driving this signal low only affects the AXI4-Lite interface and does not halt the video processing in the ACLK clock domain.

ARESETn

The CCM core has two reset source: the ARESETn pin (hardware reset), and the software reset option provided via the AXI4-Lite control interface (when present).

Note: ARESETn is not synchronized internally to AXI4-Stream frame processing, therefore de-asserting ARESETn while a frame is being process leads to image tearing.

The external reset pulse needs to be held for 32 ACLK cycles to reset the core. The ARESETn signal only resets the AXI4-Stream interfaces. The AXI4-Lite interface is unaffected by the ARESETn signal to allow the video processing core to be reset without halting the AXI4-Lite interface.

Note: When a system with multiple-clocks and corresponding reset signals are being reset, the reset generator has to ensure all reset signals are asserted/de-asserted long enough that all interfaces and clock-domains in all IP cores are correctly reinitialized.

S_AXI_ARESETn

The S_AXI_ARESETn signal is synchronous to the S_AXI_ACLK clock domain, but is internally synchronized to the ACLK clock domain. The S_AXI_ARESETn signal resets the entire core including the AXI4-Lite and AXI4-Stream interfaces.

System Considerations

The Color Correction Matrix IP core must be configured for the actual video frame-size to operate properly. To gather the frame size information from the video, it can be connected to the Video In to AXI4-Stream input and the Video Timing Controller. The timing detector logic in the Video Timing Controller gathers the video timing signals. The AXI4-Lite control interface on the Video Timing Controller allows the system processor to read out the measured frame dimensions, and program all downstream cores, such as the CCM, with the appropriate image dimensions.

If the target system uses only one setup of the CCM, the user may choose to create a constant configuration by removing the AXI4-Lite interface. This option allows reducing the core Slice footprint.

Clock Domain Interaction

The ARESETn and ACLKEN input signals do not reset or halt the AXI4-Lite interface. This allows the video processing to be reset or halted separately from the AXI4-Lite interface without disrupting AXI4-Lite transactions.

The AXI4-Lite interface responds with an error if the core registers cannot be read or written within 128 S_AXI_ACLK clock cycles. The core registers cannot be read or written if the ARESETn signal is held low, if the ACLKEN signal is held low or if the ACLK signal is not connected or not running. If core register read does not complete, the AXI4-Lite read transaction responds with **10** on the S_AXI_RRESP bus. Similarly, if a core register write does not complete, the AXI4-Lite write transaction responds with **10** on the S_AXI_BRESP bus. The S_AXI_ARESETn input signal resets the entire core.

Programming Sequence

If processing parameters such as the image size needs to be changed on the fly, or the system needs to be reinitialized, it is recommended that pipelined video IP cores are disabled/reset from system output towards the system input, and programmed/enabled from system input to system output. STATUS register bits allow system processors to identify the processing states of individual constituent cores, and successively disable a pipeline as one core after another is finished processing the last frame of data.

Error Propagation and Recovery

Parameterization and/or configuration registers define the dimensions of video frames video IP should process. Starting from a known state, based on these configuration settings the IP can predict when the beginning of the next frame is expected. Similarly, the IP can predict when the last pixel of each scan line is expected. SOF detected before it was expected (early), or SOF not present when it is expected (late), EOL detected before expected (early), or EOL not present when expected (late), signals error conditions indicative of either upstream communication errors or incorrect core configuration.

When SOF is detected early, the output SOF signal is generated early, terminating the previous frame immediately. When SOF is detected late, the output SOF signal is generated according to the programmed values. Extra lines / pixels from the previous frame are dropped until the input SOF is captured.

Similarly, when EOL is detected early, the output EOL signal is generated early, terminating the previous line immediately. When EOL is detected late, the output EOL signal is generated according to the programmed values. Extra pixels from the previous line are dropped until the input EOL is captured.

C Model Reference

Installation and Directory Structure

This chapter contains information for installing the Color Correction Matrix C-Model, and describes the file contents and directory structure.

Software Requirements

The Color Correction Matrix v5.00.a C-models were compiled and tested with the following software versions.

Table 4-1: **Supported Systems and Software Requirements**

Platform	C-Compiler
Linux 32-bit and 64-bit	GCC 4.1.1
Windows 32-bit and 64-bit	Microsoft Visual Studio 2008 (Visual C++ 8.0)

Installation

The installation of the C-Model requires updates to the PATH variable, as described below.

Linux

Ensure that the directory in which the `libIp_v_ccm_v5_00_a_bitacc_cmodel.so` and `libstlport.so.5.1` files are located is in your $LD_LIBRARY_PATH environment variable.

C-Model File Contents

Unzipping the `v_ccm_v5_00_a_bitacc_model.zip` file creates the following directory structures and files which are described in Table 4-2.

Table 4-2: **C-Model Files**

File	Description
/lin	Pre-compiled bit accurate ANSI C reference model for simulation on 32-bit Linux Platforms
libIp_v_ccm_v5_00_a_bitacc_cmodel.lib	Color Correction Matrix v4.00.a model shared object library (Linux platforms only)
libstlport.so.5.1	STL library, referenced by the Color Correction Matrix library (Linux platforms only)
run_bitacc_cmodel	Pre-compiled bit accurate executable for simulation on 32-bit Linux Platforms
/lin64	Pre-compiled bit accurate ANSI C reference model for simulation on 64-bit Linux Platforms
libIp_v_ccm_v5_00_a_bitacc_cmodel.lib	Color Correction Matrix v4.00.a model shared object library (Linux platforms only)
libstlport.so.5.1	STL library, referenced by the Color Correction Matrix library (Linux platforms only)
run_bitacc_cmodel	Pre-compiled bit accurate executable for simulation on 32-bit Linux Platforms
/nt	Pre-compiled bit accurate ANSI C reference model for simulation on 32-bit Windows Platforms
libIp_v_ccm_v5_00_a_bitacc_cmodel.lib	Pre-compiled library file for win32 compilation
run_bitacc_cmodel.exe	Pre-compiled bit accurate executable for simulation on 32-bit Windows Platforms
/nt64	Pre-compiled bit accurate ANSI C reference model for simulation on 64-bit Windows Platforms
libIp_v_ccm_v5_00_a_bitacc_cmodel.lib	Pre-compiled library file for win32 compilation
run_bitacc_cmodel.exe	Pre-compiled bit accurate executable for simulation on 64-bit Windows Platforms
README.txt	Release notes
pg001-v-ccm.pdf	*Color Correction Matrix Product Guide*
v_ccm_v5_00_a_bitacc_cmodel.h	Model header file
rgb_utils.h	Header file declaring the RGB image / video container type and support functions
bmp_utils.h	Header file declaring the bitmap (.bmp) image file I/O functions
video_utils.h	Header file declaring the generalized image / video container type, I/O and support functions.

Table 4-2: **C-Model Files *(Cont'd)***

File	Description
Kodim19_128x192.bmp	128x192 sample test image of the Lighthouse image from the True-color Kodak test images
run_bittacc_cmodel.c	Example code calling the C-Model

Using the C-Model

The bit accurate C model is accessed through a set of functions and data structures that are declared in the v_ccm_v5_00_a_bitacc_cmodel.h file.

Before using the model, the structures holding the inputs, generics and output of the CCM instance must be defined:

```
struct  xilinx_ip_v_ccm_v5_00_a_generics ccm_generics;
struct  xilinx_ip_v_ccm_v5_00_a_inputs   ccm_inputs;
struct  xilinx_ip_v_ccm_v5_00_a_outputs  ccm_outputs;
```

The declaration of these structures is in the v_ccm_v5_00_a_bitacc_cmodel.h file.

Table 4-3 lists the generic parameters taken by the CCM v4.00.a IP core bit accurate model, as well as the default values. For an actual instance of the core, these parameters can only be set in generation time through the CORE Generator™ GUI.

Table 4-3: **Model Generic Parameters and Default Values**

Generic Variable	Type	Default Value	Range	Description
IWIDTH	int	8	8,10,12, 16	Input data width
OWIDTH	int	8	8,10,12, 16	Output width
INPUT_VIDEO_FORMAT	int	2	1, 2	Input Video Format 1=YUV 4:4:4 2=RGB
OUTPUT_VIDEO_FORMAT	int	2	1 2	Output Video Format 1=YUV 4:4:4 2=RGB

Calling xilinx_ip_v_ccm_v5_00_a_get_default_generics(&ccm_generics) initializes the generics structure with the CCM GUI defaults, listed in Table 4-3.

Coefficients, offsets, clipping and clamping values can also be set dynamically through the pCore and General Purpose Processor interfaces. Consequently, these values are passed as inputs to the core, along with the actual test image, or video sequence (Table 4-4).

Table 4-4: **Core Generic Parameters and Default Values**

Input Variable	Type	Default Value	Range[1]	Description
video_in	video_struct	null	N/A	Container to hold input image or video data.[3]
coeffs	double[3][3]	identity[2]	[-4 to 4]	3x3 matrix of floating point numbers
offsets	double[3]	zeros[2]	-2^{OWIDTH} *to* $2^{OWIDTH}-1$	Offsets applied to the output color channels
CLAMP	int	0	0 *to* $2^{OWIDTH}-1$	Clamping value for outputs
CLIP	int	$2^{OWIDTH}-1$	0 *to* $2^{OWIDTH}-1$	Clipping value for outputs

1. OWIDTH is the output data width of each color component
2. For a detailed description of inputs and other generic parameters, see Core Interfaces and Register Space.
3. For the description of the input structure, see Initializing the CCM Input Video Structure.

The structure `ccm_inputs` defines the values of run time parameters and the actual input image. Calling

```
xilinx_ip_v_ccm_v5_00_a_get_default_inputs(&ccm_generics, &ccm_inputs)
```

initializes the input structure with the CCM GUI default values (see Table 4-4).

The `video_in` variable is not initialized because the initialization depends on the actual test image to be simulated. Initializing the CCM Input Video Structure describes the initialization of the `video_in` structure.

After the inputs are defined, the model can be simulated by calling this function:

```
int xilinx_ip_v_ccm_v5_00_a_bitacc_simulate(
struct xilinx_ip_v_ccm_v5_00_a_generics* generics,
struct xilinx_ip_v_ccm_v5_00_a_inputs*   inputs,
struct xilinx_ip_v_ccm_v5_00_a_outputs*  outputs).
```

Results are included in the outputs structure, which contains only one member, type `video_struct`. After the outputs are evaluated and saved, dynamically allocated memory for input and output video structures must be released by calling this function:

```
void xilinx_ip_v_ccm_v5_00_a_destroy(
struct xilinx_ip_v_ccm_v5_00_a_inputs *input,
struct xilinx_ip_v_ccm_v5_00_a_outputs *output).
```

Successful execution of all provided functions, except for the destroy function, return value 0. A non-zero error code indicates that problems occurred during function calls.

CCM Input and Output Video Structure

Input images or video streams can be provided to the CCM v4.00.a reference model using the `video_struct` structure, defined in `video_utils.h`:

```
struct video_struct{
  int       frames, rows, cols, bits_per_component, mode;
  uint16*** data[5]; };
```

Table 4-5: **Member Variables of the Video Structure**

Member Variable	Designation
frames	Number of video/image frames in the data structure.
rows	Number of rows per frame. Pertaining to the image plane with the most rows and columns, such as the luminance channel for YUV data. Frame dimensions are assumed constant through all frames of the video stream. However different planes, such as y, u and v can have different dimensions.
cols	Number of columns per frame. Pertaining to the image plane with the most rows and columns, such as the luminance channel for YUV data. Frame dimensions are assumed constant through all frames of the video stream. However different planes, such as y, u and v can have different dimensions.
bits_per_component	Number of bits per color channel/component.All image planes are assumed to have the same color/component representation. Maximum number of bits per component is 16.
mode	Contains information about the designation of data planes. Named constants to be assigned to mode are listed in Table 4-6.
data	Set of five pointers to three dimensional arrays containing image plane data. Data is in 16-bit unsigned integer format accessed as data[plane][frame][row][col].

Table 4-6: **Named Video Modes with Corresponding Planes and Representations**

Mode(1)	Planes	Video Representation
FORMAT_MONO	1	Monochrome – Luminance only
FORMAT_RGB	3	RGB image/video data
FORMAT_C444	3	444 YUV, or YCrCb image/video data
FORMAT_C422	3	422 format YUV video, (u, v chrominance channels horizontally sub-sampled)
FORMAT_C420	3	420 format YUV video, (u, v sub-sampled both horizontally and vertically)
FORMAT_MONO_M	3	Monochrome (Luminance) video with Motion
FORMAT_RGBA	4	RGB image/video data with alpha (transparency) channel
FORMAT_C420_M	5	420 YUV video with Motion
FORMAT_C422_M	5	422 YUV video with Motion
FORMAT_C444_M	5	444 YUV video with Motion
FORMAT_RGBM	5	RGB video with Motion

1. The Color Correction Matrix core supports Modes FORMAT_RGB and FORMAT_C444.

Initializing the CCM Input Video Structure

The easiest way to assign stimuli values to the input video structure is to initialize it with an image or video. The `bmp_util.h` and `video_util.h` header files packaged with the bit accurate C models contain functions to facilitate file I/O.

Bitmap Image Files

The header `bmp_utils.h` declares functions that help access files in Windows Bitmap format (http://en.wikipedia.org/wiki/BMP_file_format). However, this format limits color depth to a maximum of 8-bits per pixel, and operates on images with three planes (R,G,B). Consequently, the following functions operate on arguments type `rgb8_video_struct`, which is defined in `rgb_utils.h`. Also, both functions support only true-color, non-indexed formats with 24-bits per pixel.

```
int write_bmp(FILE *outfile, struct rgb8_video_struct *rgb8_video);
int read_bmp(FILE *infile, struct rgb8_video_struct *rgb8_video);
```

Exchanging data between `rgb8_video_struct` and general `video_struct` type frames/videos is facilitated by these functions:

```
int copy_rgb8_to_video(struct rgb8_video_struct* rgb8_in,
                       struct video_struct* video_out );
int copy_video_to_rgb8(struct video_struct* video_in,
                       struct rgb8_video_struct* rgb8_out );
```

Note: All image/video manipulation utility functions expect both input and output structures initialized; for example, pointing to a structure that has been allocated in memory, either as static or dynamic variables. Moreover, the input structure must have the dynamically allocated container (data or r, g, b) structures already allocated and initialized with the input frame(s). If the output container structure is pre-allocated at the time of the function call, the utility functions verify and issue an error if the output container size does not match the size of the expected output. If the output container structure is not pre-allocated, the utility functions create the appropriate container to hold results.

Binary Image/Video Files

The `video_utils.h` header file declares functions that help load and save generalized video files in raw, uncompressed format.

```
int read_video( FILE* infile,  struct video_struct* in_video);
int write_video(FILE* outfile, struct video_struct* out_video);
```

These functions serialize the video_struct structure. The corresponding file contains a small, plain text header defining, "Mode", "Frames", "Rows", "Columns", and "Bits per Pixel". The plain text header is followed by binary data, 16-bits per component in scan line continuous format. Subsequent frames contain as many component planes as defined by the video mode value selected. Also, the size (rows, columns) of component planes can differ within each frame as defined by the actual video mode selected.

Working with Video_struct Containers

The `video_utils.h` header file defines functions to simplify access to video data in `video_struct`.

```
int video_planes_per_mode(int mode);
int video_rows_per_plane(struct video_struct* video, int plane);
int video_cols_per_plane(struct video_struct* video, int plane);
```

The `video_planes_per_mode` function returns the number of component planes defined by the mode variable, as described in Table 4-6. The `video_rows_per_plane` and `video_cols_per_plane` functions return the number of rows and columns in a given plane of the selected video structure. The following example demonstrates using these functions in conjunction to process all pixels within a video stream stored in the `in_video` variable:

```
for (int frame = 0; frame < in_video->frames; frame++) {
  for (int plane = 0; plane < video_planes_per_mode(in_video->mode); plane++) {
    for (int row = 0; row < rows_per_plane(in_video,plane); row++) {
      for (int col = 0; col < cols_per_plane(in_video,plane); col++) {
   // User defined pixel operations on
// in_video->data[plane][frame][row][col]
      }
    }
  }
}
```

C Model Example Code

An example C file, `run_bitacc_cmodel.c`, is provided to demonstrate the steps required to run the model. After following the compilation instructions, run the example executable. The executable takes the path/name of the input file and the path of the output as parameters. If invoked with insufficient parameters, this help message is issued:

```
Usage: run_bitacc_cmodel in_file out_path
in_file     : path/name of the input file (YUV file)
out_path : path to to the output files
```

During successful execution, two directories is created at the location specified by the out_path command line parameter. The first directory is the "expected" directory. This directory contains a BMP file that corresponds to the output of the first frame that was processed. This directory also contains a txt file called `golden_1.txt`. This txt file contains the output of the model in a format that can be directly used with the demonstration test bench. The second directory that is created is the "stimuli" directory. This directory contains a txt file called `stimuli_1.txt`. This txt file contains the input of the model in a format that can be directly used with the demonstration test bench.

Compiling with the CCM C-Model

Linux (32- and 64-bit)

To compile the example code, first ensure that the directory in which the files `libIp_v_ccm_v5_00_a_bitacc_cmodel.so` and `libstlport.so.5.1` are located is present in your `$LD_LIBRARY_PATH` environment variable. These shared libraries are referenced during the compilation and linking process. Then cd into the directory where the header files, library files and `run_bitacc_cmodel.c` were unpacked. The libraries and header files are referenced during the compilation and linking process.

Place the header file and C source file in a single directory. Then in that directory, compile using the GNU C Compiler:

```
gcc -m32 -x c++ ../run_bitacc_cmodel.c ../gen_stim.c -o run_bitacc_cmodel -L.
-lIp_v_ccm_v5_00_a_bitacc_cmodel -Wl,-rpath,.


gcc  -m64 -x c++ ../run_bitacc_cmodel.c ../gen_stim.c -o run_bitacc_cmodel -L.
-lIp_v_ccm_v5_00_a_bitacc_cmodel -Wl,-rpath,.
```

Windows (32- and 64-bit)

Precompiled library `v_ccm_v5_00_a_bitacc_cmodel.dll`, and top level demonstration code `run_bitacc_cmodel.c` should be compiled with an ANSI C compliant compiler under Windows. Here an example is presented using Microsoft Visual Studio.

In Visual Studio create a new, empty Windows Console Application project. As existing items, add:

- The `llibIpv_ccm_v5_00_a_bitacc_cmodel.dll` file to the "Resource Files" folder of the project
- The `run_bitacc_cmodel.c` and `gen_stim.c` files to the "Source Files" folder of the project
- The `v_ccm_v5_00_a_bitacc_cmodel.h` header files to "Header Files" folder of the project (optional)

After the project has been created and populated, it needs to be compiled and linked (built) to create a win32 executable. To perform the build step, choose **Build Solution** from the Build menu. An executable matching the project name has been created either in the Debug or Release subdirectories under the project location based on whether **Debug** or **Release** has been selected in the **Configuration Manager** under the Build menu.

SECTION II: VIVADO DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Customizing and Generating the Core

This chapter includes information on using Xilinx tools to customize and generate the core.

GUI

The Color Correction Matrix core is easily configured to meet developers' specific needs before instantiation through the Vivado design tools Graphical User Interface (GUI). When you start to build the Color Correction Matrix core within the system, you are guided through and asked to set various parameters. This section provides a quick reference to the windows and parameters that can be configured at compile time.

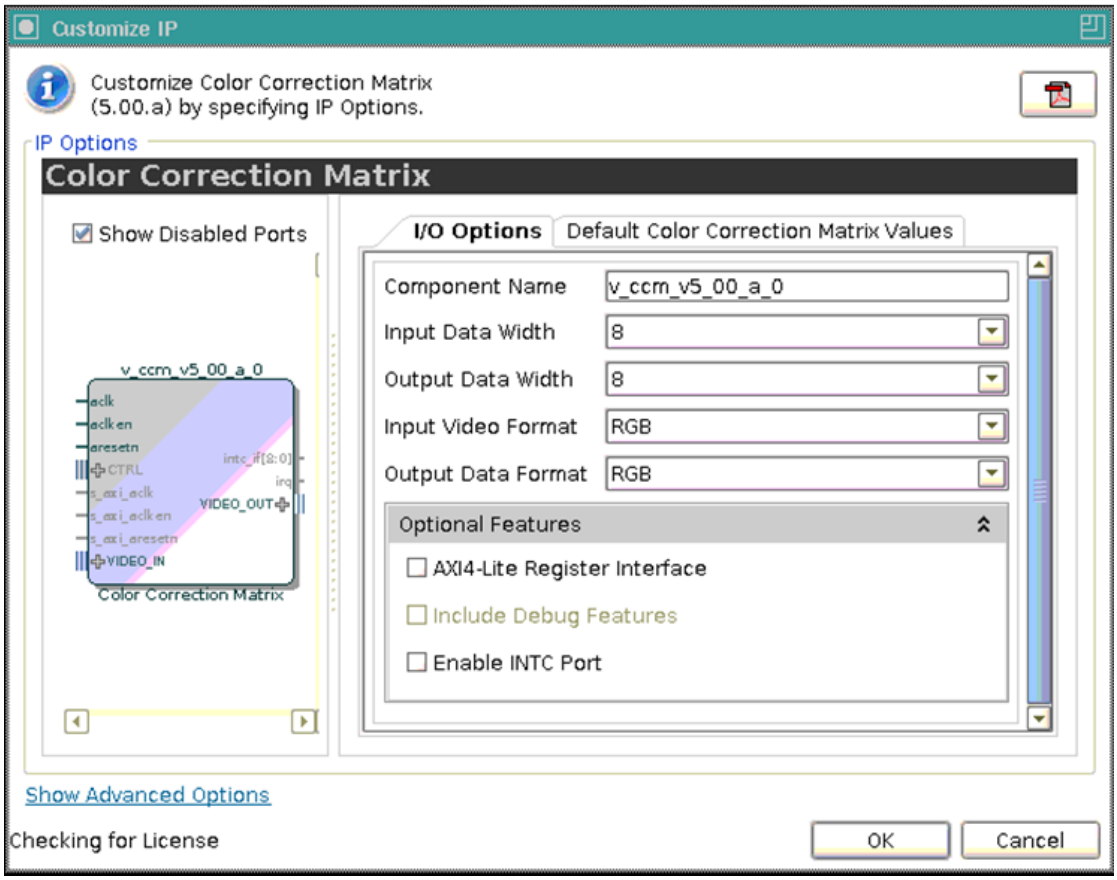

Figure 5-1: **IP Catalog Screen 1**

The first screen (Figure 5-1) shows a representation of the IP symbol on the left side, and the parameters on the right, which are described as follows:

- **Component Name**: The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_". The name v_ccm_v5_00_a cannot be used as a component name.
- **Input Data Width**: Specifies the bit width of the input color channel for each component.
  In cases where the Input Data Width does not equal the Output Data Width, the data is scaled up or down accordingly.
- **Output Data Width**: Specifies the bit width of the output color channel for each component.
  In cases where the Input Data Width does not equal the Output Data Width, the data is scaled up or down accordingly.
- **Input Video Format**: Specifies the format of the input video. Valid selections are RGB and YUV 4:4:4.
- **Output Video Format**: Specifies the format of the output video. Valid selections are RGB and YUV 4:4:4.
- **Optional Features**:
  - **AXI4-Lite Register Interface**: When selected, the core is generated with an AXI4-Lite interface, which gives access to dynamically program and change processing parameters. For more information, refer to Control Interface in Chapter 2.
  - **Include Debugging Features**: When selected, the core is generated with debugging features, which simplify system design, testing and debugging. For more information, refer to Debugging Features in Appendix C.

    Note: Debugging features are only available when the AXI4-Lite Register Interface is selected.
  - **INTC Interface**: When selected, the core generates the optional INTC_IF port, which gives parallel access to signals indicating frame processing status and error conditions. For more information, refer to The Interrupt Subsystem in Chapter 2.

The second screen (Figure 5-2) also shows a representation of the IP symbol on the left side, but has a second set of parameters on the right, as described in this section.

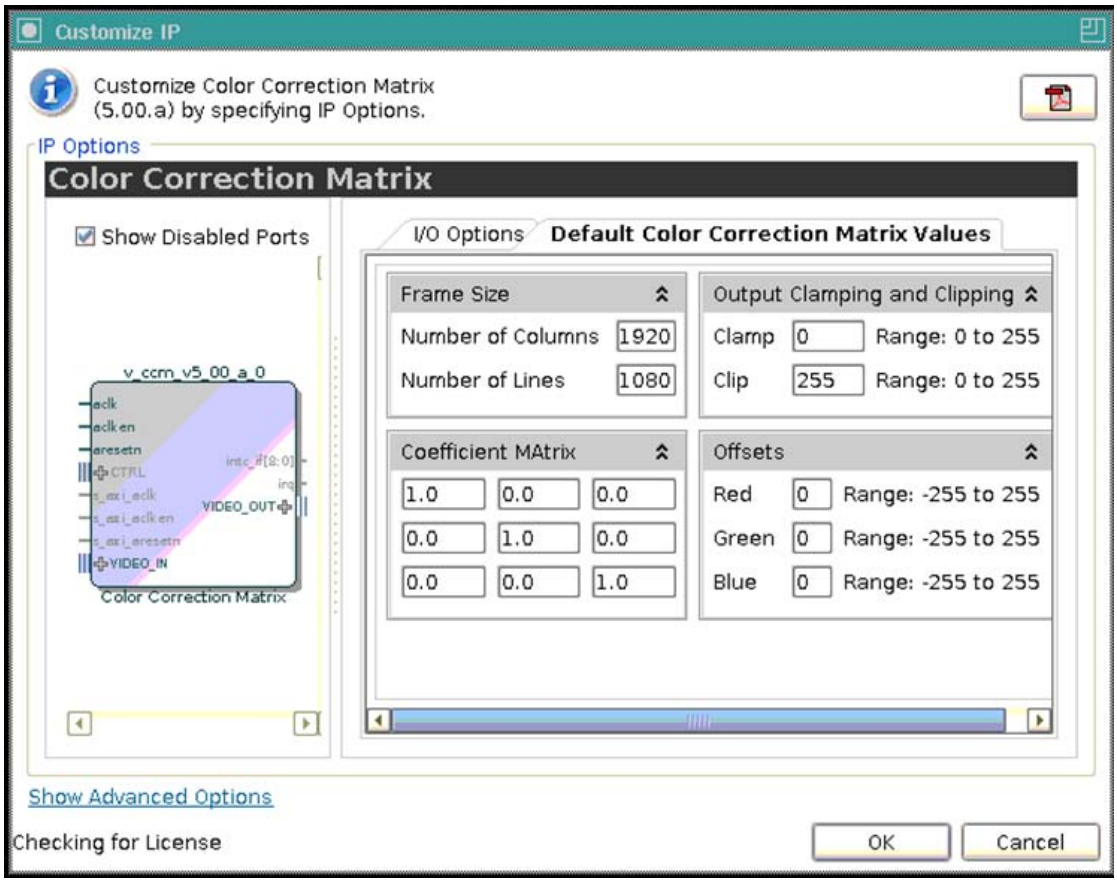

Figure 5-2: **IP Catalog Screen 2**

- **Frame Size**:
  - **Number of Columns**: When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the lower half-word of the ACTIVE_SIZE register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the horizontal size of the frames the generated core instance is to process.
  - **Number of Lines**: When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the upper half-word of the ACTIVE_SIZE register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the vertical size (number of lines) of the frames the generated core instance is to process.
- **Output Clamping and Clipping**:
  - **Clamp**: Sets the minimum value of the output data. When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the Clamp register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the minimum value of the output data for the generated core instance.

    - **Clip**: Sets the maximum value of the output data. When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the Clip register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the maximum value of the output data for the generated core instance.

- **Coefficient Matrix**: Enter the floating-point coefficients ranging from [-4, 4] (K in Equation 1-1) by specifying the 18 bit coefficients with 15 fractional bits of the coefficient matrix. The entered values are the default used to initialize the core and the values used when the core is reset. Enter the real valued coefficients as floating-point decimal values in the range [-4.0, 4.0] (K in Equation 1-1). When the core is generated, the floating-point decimal value is converted to an 18-bit vector with 15 fractional bits, which are used internally to the core.
- **Offsets**: Enter the offset coefficients (O in Equation 1-1). These signed coefficients have the same bit width as the output. Enter the offset values (O in Equation 1-1). These signed integer values must be in the range $[-2^{Out\_Data\_Width}, 2^{Out\_Data\_Width}-1]$, and are 1-bit wider than the Output Data Width.

Output Generation

Vivado design tools generate the files necessary to build the core and places those files in the `<project>/<project>.srcs/sources_1/ip/<core>` directory.

File Details

The Vivado design tools output consists of some or all the following files.

Name	Description
v_ccm_v5_00_a	Library directory for the v_ccm_v5_00_a core which contains the encrypted source files.
v_tc_v5_00_a	Library directory for the helper core which contain the encrypted source files used with the v_ccm_v5_00_a.
<component_name>.veo	The HDL template for instantiating the core.
<component_name>.vho	
<component_name>.xci	IP-XACT file describing which options were used to generate the core. An XCI file can also be used as a source file for Vivado.
<component_name>.xml	IP-XACT XML file describing how the core is constructed so Vivado can properly build the core.

Constraining the Core

Required Constraints

The ACLK pin should be constrained at the pixel clock rate desired for your video stream.

Device, Package, and Speed Grade Selections

There are no device, package, or speed grade requirements for this core. For a complete listing of supported devices, see the release notes for this core. For a complete listing of supported devices, see the release notes for this core.

Clock Frequencies

The pixel clock (ACLK) frequency is the required frequency for the Color Correction Matrix core. See Maximum Frequencies in Chapter 2. The S_AXI_ACLK maximum frequency is the same as the ACLK maximum.

Clock Management

The core automatically handles clock domain crossing between the ACLK (video pixel clock and AXI4-Stream) and the S_AXI_ACLK (AXI4-Lite) clock domains. The S_AXI_ACLK clock can be slower or faster than the ACLK clock signal, but must not be more than 128x faster than ACLK.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking rules for this core.

Transceiver Placement

There are no Transceiver Placement requirements for the Color Correction Matrix core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

SECTION III: ISE DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Detailed Example Design

Customizing and Generating the Core

This chapter includes information on using Xilinx tools to customize and generate the core.

GUI

The Color Correction Matrix core is easily configured to meet developers' specific needs before instantiation through the CORE Generator™ and EDK graphical user interfaces (GUIs). When you start to build the Color Correction Matrix core within the system, you are guided through and asked to set various parameters. This section provides a quick reference to the windows and parameters that can be configured at compile time.

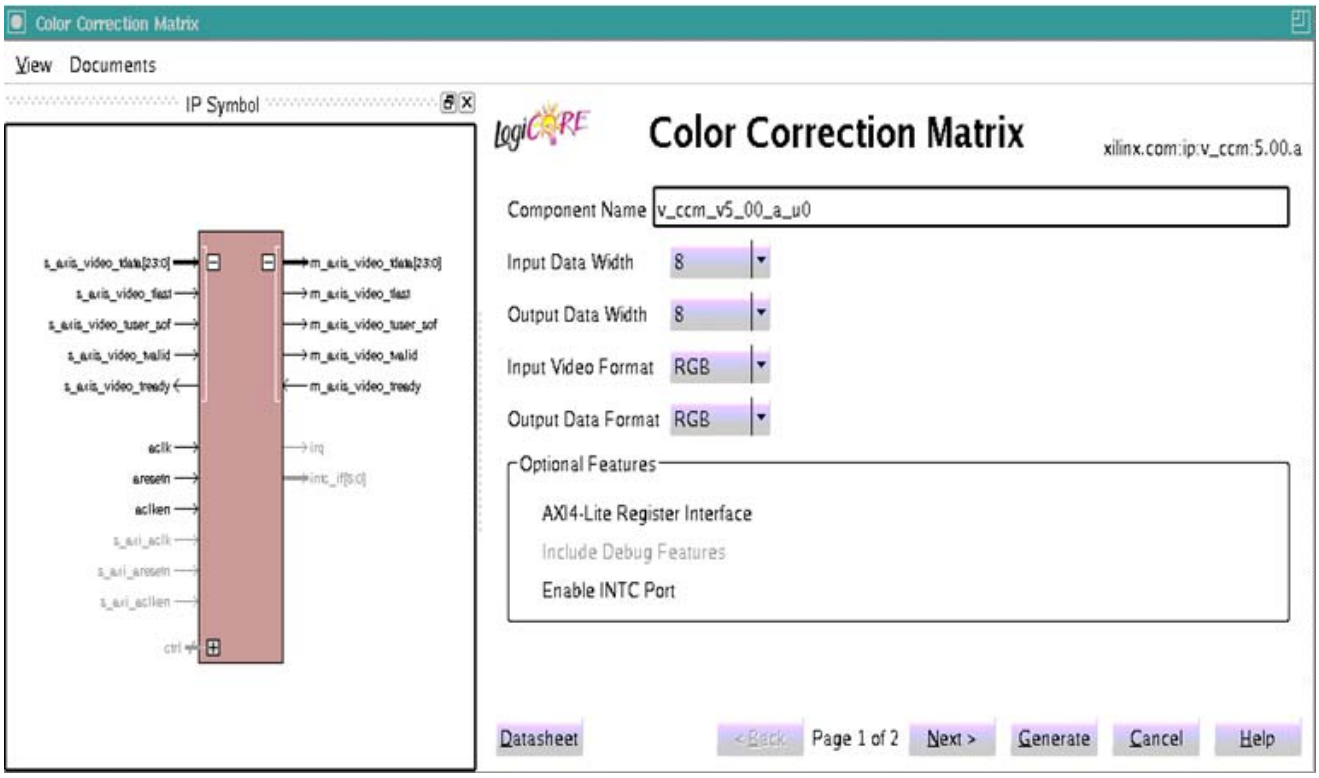

Figure 7-1: **Screen 1**

The first screen (Figure 7-1 for CORE Generator and Figure 7-3 for EDK) shows a representation of the IP symbol on the left side, and the parameters on the right, which are described as follows:

- **Component Name**: The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_". The name v_ccm_v5_00_a cannot be used as a component name.
- **Input Data Width**: Specifies the bit width of the input color channel for each component.
  In cases where the Input Data Width does not equal the Output Data Width, the data is scaled up or down accordingly.
- **Output Data Width**: Specifies the bit width of the output color channel for each component.
  In cases where the Input Data Width does not equal the Output Data Width, the data is scaled up or down accordingly.
- **Input Video Format**: Specifies the format of the input video. Valid selections are RGB and YUV 4:4:4.
- **Output Video Format**: Specifies the format of the output video. Valid selections are RGB and YUV 4:4:4.
- **Optional Features**:
  - **AXI4-Lite Register Interface**: When selected, the core is generated with an AXI4-Lite interface, which gives access to dynamically program and change processing parameters. For more information, refer to Control Interface in Chapter 2.
  - **Include Debugging Features**: When selected, the core is generated with debugging features, which simplify system design, testing and debugging. For more information, refer to Debugging Features in Appendix C.

    Note: Debugging features are only available when the AXI4-Lite Register Interface is selected.
  - **INTC Interface**: When selected, the core generates the optional INTC_IF port, which gives parallel access to signals indicating frame processing status and error conditions. For more information, refer to The Interrupt Subsystem in Chapter 2.

The second screen (Figure 7-2) also shows a representation of the IP symbol on the left side, but has a second set of parameters on the right, as described in this section.

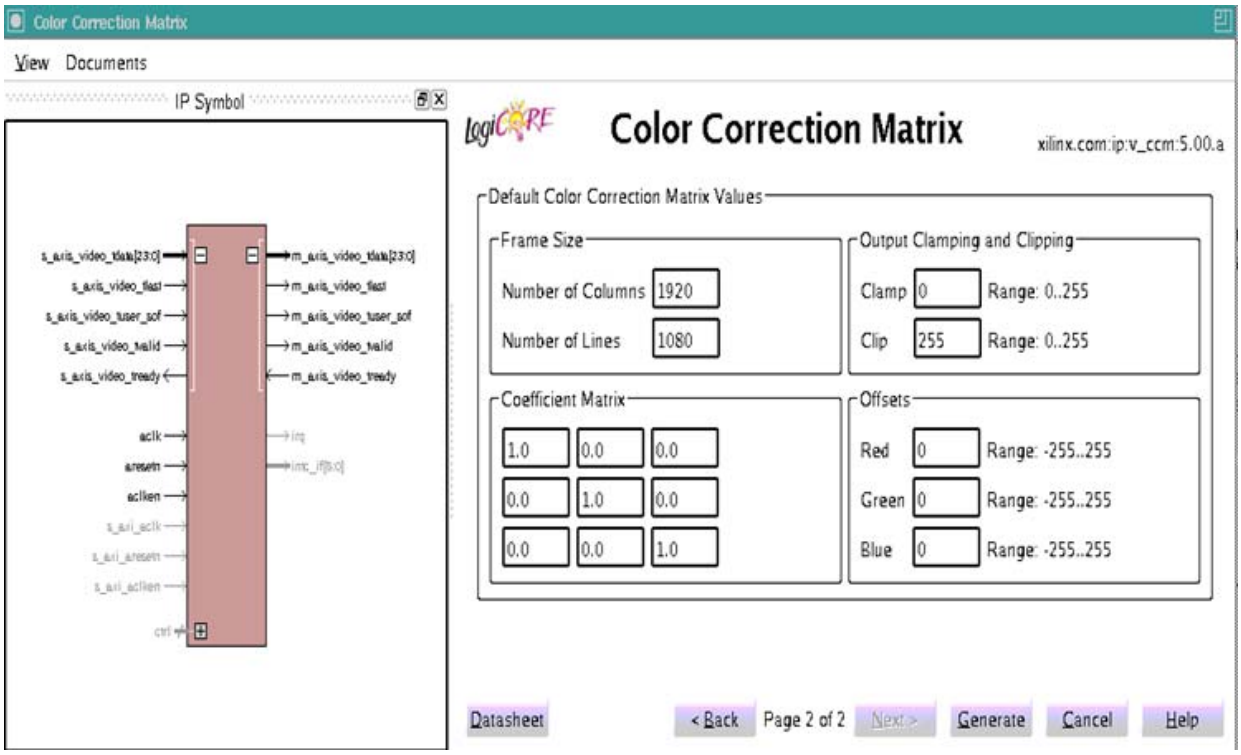

Figure 7-2: **Screen 2**

- **Frame Size**:
  - **Number of Columns**: When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the lower half-word of the ACTIVE_SIZE register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the horizontal size of the frames the generated core instance is to process.
  - **Number of Lines**: When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the upper half-word of the ACTIVE_SIZE register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the vertical size (number of lines) of the frames the generated core instance is to process.
- **Output Clamping and Clipping**:
  - **Clamp**: Sets the minimum value of the output data. When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the Clamp register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the minimum value of the output data for the generated core instance.
  - **Clip**: Sets the maximum value of the output data. When the AXI4-Lite control interface is enabled, the generated core uses the value specified in the CORE Generator GUI as the default value for the Clip register. When an AXI4-Lite interface

is not present, the GUI selection permanently defines the maximum value of the output data for the generated core instance.

- **Coefficient Matrix**: Enter the floating-point coefficients ranging from [-4, 4] (K in Equation 1-1) by specifying the 18 bit coefficients with 15 fractional bits of the coefficient matrix. The entered values are the default used to initialize the core and the values used when the core is reset. Enter the real valued coefficients as floating-point decimal values in the range [-4.0, 4.0] (K in Equation 1-1). When the core is generated, the floating-point decimal value is converted to an 18-bit vector with 15 fractional bits, which are used internally to the core.
- **Offsets**: Enter the offset coefficients (O in Equation 1-1). These signed coefficients have the same bit width as the output. Enter the offset values (O in Equation 1-1). These signed integer values must be in the range $[-2^{Out\_Data\_Width}, 2^{Out\_Data\_Width}-1]$, and are 1-bit wider than the Output Data Width specified on the first page of the GUI, as shown in Figure 7-3.

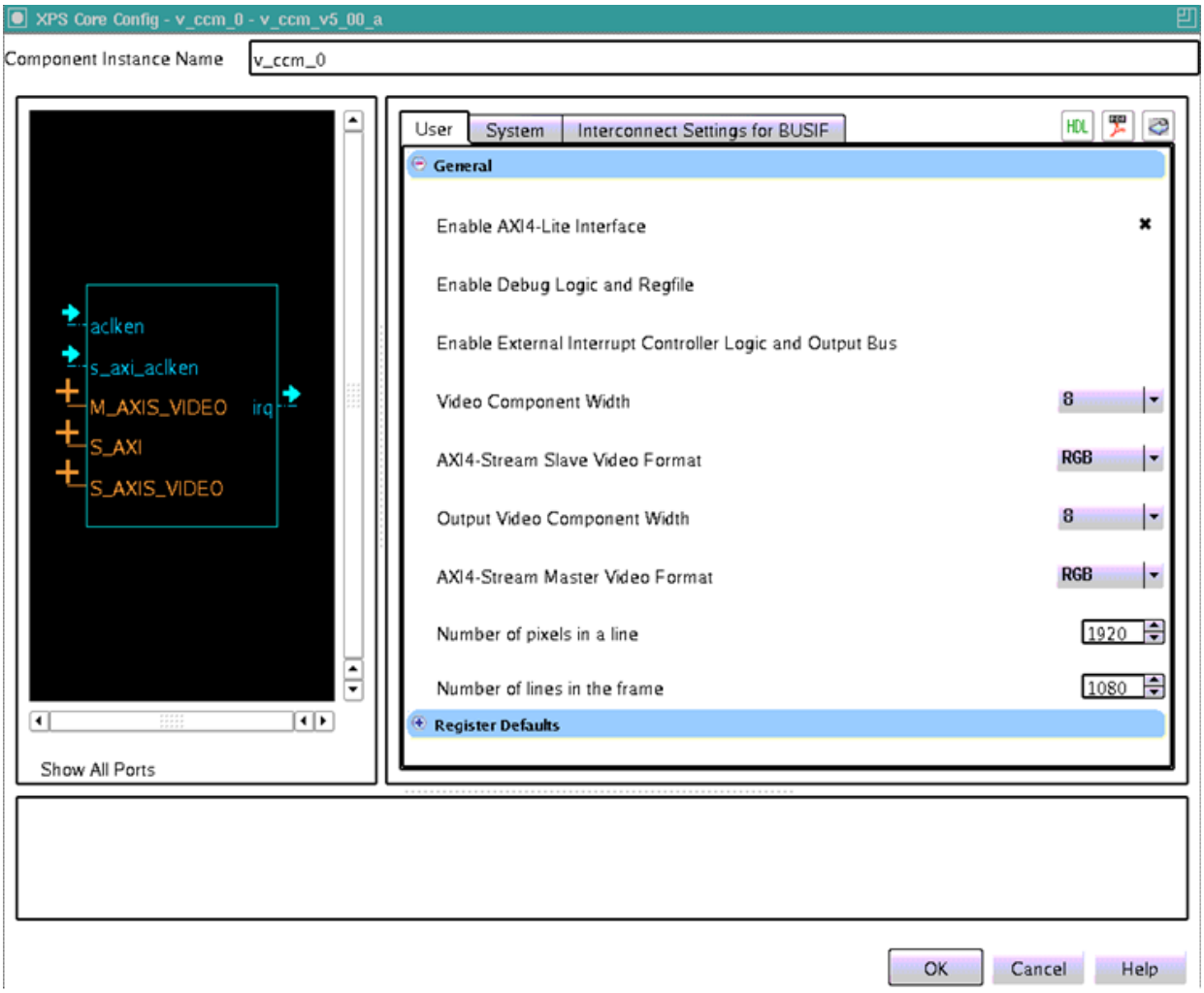

Figure 7-3: **EDK Graphical User Interface**

Definitions of the EDK GUI controls are identical to the corresponding CORE Generator GUI functions.

Parameter Values in the XCO File

Table 7-1 defines valid entries for the XCO parameters. Xilinx strongly suggests that XCO parameters are not manually edited in the XCO file; instead, use the CORE Generator software GUI to configure the core and perform range and parameter value checking. The XCO parameters are helpful in defining the interface to other Xilinx tools.

Table 7-1: **XCO Parameters**

XCO Parameter	Default Value
component_name	v_ccm_v5_00_a_u0
s_axis_video_data_width	8
m_axis_video_data_width	8
s_axis_video_format	RGB
m_axis_video_format	RGB
k11	1.0
k12	0.0
k13	0.0
k21	0.0
k22	1.0
k23	0.0
k31	0.0
k32	0.0
k33	1.0
roffset	0
goffset	0
boffset	0
clip	255
clamp	0
active_cols	1920
active_rows	1080
has_axi4_lite	false
has_debug	false
has_intc_if	false

Output Generation

CORE Generator outputs the core as a netlist that can be inserted into a processor interface wrapper or instantiated directly in an HDL design. The output is placed in the <project directory>.

File Details

The CORE Generator output consists of some or all the following files.

Name	Description
<component_name>_readme.txt	Readme file for the core.
<component_name>.ngc	The netlist for the core.
<component_name>.veo	The HDL template for instantiating the core.
<component_name>.vho	
<component_name>.v	The structural simulation model for the core. It is used for functionally simulating the core.
<component_name>.vhd	
<component_name>.xco	Log file from CORE Generator software describing which options were used to generate the core. An XCO file can also be used as an input to the CORE Generator software.

Constraining the Core

Required Constraints

The ACLK pin should be constrained at the pixel clock rate desired for your video stream.

Device, Package, and Speed Grade Selections

There are no device, package, or speed grade requirements for this core. For a complete listing of supported devices, see the release notes for this core. For a complete listing of supported devices, see the release notes for this core.

Clock Frequencies

The pixel clock (ACLK) frequency is the required frequency for the Color Correction Matrix core. See Maximum Frequencies in Chapter 2. The S_AXI_ACLK maximum frequency is the same as the ACLK maximum.

Clock Management

The core automatically handles clock domain crossing between the ACLK (video pixel clock and AXI4-Stream) and the S_AXI_ACLK (AXI4-Lite) clock domains. The S_AXI_ACLK clock can be slower or faster than the ACLK clock signal, but must not be more than 128x faster than ACLK.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking rules for this core.

Transceiver Placement

There are no Transceiver Placement requirements for the Color Correction Matrix core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

Detailed Example Design

Example Design

No example design is available at this time for the LogiCORE IP Color Correction Matrix v5.00.a core.

Demonstration Test Bench

A demonstration test bench is provided which enables core users to observe core behavior in a typical use scenario. The user is encouraged to make simple modifications to the test conditions and observe the changes in the waveform.

Test Bench Structure

The top-level entity, `tb_main.v`, instantiates the following modules:

- `DUT`

  The CCM core instance under test.

- `axi4lite_mst`

  The AXI4-Lite master module, which initiates AXI4-Lite transactions to program core registers.

- `axi4s_video_mst`

  The AXI4-Stream master module, which opens the stimuli txt file and initiates AXI4-Stream transactions to provide stimuli data for the core

- `axi4s_video_slv`

  The AXI4-Stream slave module, which opens the result txt file and verifies AXI4-Stream transactions from the core

- `ce_gen`

Programmable Clock Enable (ACLKEN) generator

Running the Simulation

- Simulation using ModelSim for Linux:
  From the console, type `source run_mti.sh`.
- Simulation using iSim for Linux:
  From the console, type `source run_isim.sh`.
- Simulation using ModelSim for Windows:
  Double-click the `run_mti.bat` file.
- Simulation using iSim:
  Double-click the `run_isim.bat` file.

Directory and File Contents

The directory structure underneath the top-level folder is:

- **expected**:

  Contains the pre-generated expected/golden data used by the test bench to compare actual output data.

- **stimuli**:

  Contains the pre-generated input data used by the test bench to stimulate the core (including register programming values).

- **Results**:

  Actual output data is written to a file in this folder.

- **Src**:

  Contains the .vhd simulation files and the .xco CORE Generator parameterization file of the core instance. The .vhd file is a netlist generated using CORE Generator. The .xco file can be used to regenerate a new netlist using CORE Generator.

The available core C-model can be used to generate stimuli and expected results for any user bmp image. For more information, refer to Chapter 4, C Model Reference.

The top-level directory contains packages and Verilog modules used by the test bench, as well as:

- `isim_wave.wcfg`

  Waveform configuration for ISIM

- `mti_wave.do`

  Waveform configuration for ModelSim

- `run_isim.bat`

  Runscript for iSim in Windows

- `run_isim.sh`

  Runscript for iSim in Linux

- `run_mti.bat`

  Runscript for ModelSim in Windows

- `run_mti.sh`

  Runscript for ModelSim in Linux

SECTION IV: APPENDICES

Verification, Compliance, and Interoperability

Migrating

Debugging

Application Software Development

Additional Resources

Appendix A

Verification, Compliance, and Interoperability

Simulation

A highly parameterizable test bench was used to test the Color Correction Matrix core. Testing included the following:

- Register accesses
- Processing multiple frames of data
- AXI4-Stream bidirectional data-throttling tests
- Testing detection, and recovery from various AXI4-Stream framing error scenarios
- Testing different `ACLKEN` and `ARESETn` assertion scenarios
- Testing of various frame sizes
- Varying parameter settings

Hardware Testing

The Color Correction Matrix core has been validated in hardware at Xilinx to represent a variety of parameterizations, including the following:

- A test design was developed for the core that incorporated a MicroBlaze™ processor, AXI4-Lite interconnect and various other peripherals. The software for the test system included pre-generated input and output data along with live video stream. The MicroBlaze processor was responsible for:
  - Initializing the appropriate input and output buffers
  - Initializing the Color Correction Matrix core
  - Launching the test
  - Comparing the output of the core against the expected results

- Reporting the Pass/Fail status of the test and any errors that were found

Interoperability

The core slave (input) AXI4 Stream interface can be configured in either RGB or YUV 4:4:4 format. This interface can work directly with any video core that produces the same format. The core master (output) interface can be configured in either RGB or YUV 4:4:4 format. It can work directly with any video core the consumes the same format. The AXI4-Stream interfaces need to be compliant to the AXI4-Stream Video Protocol as described in the *Video IP: AXI Feature Adoption* section of the (UG761) *AXI Reference Guide* [Ref 1].

Appendix B

Migrating

From version v3.0 to v4.00.a of the CCM core the following significant changes took place:

- XSVI interfaces were replaced by AXI4-Stream interfaces
- Since AXI4-Stream does not carry video timing data, the timing detector and timing generator modules were trimmed.
- The pCore, General Purpose Processor and Transparent modes became obsolete and were removed
- Native support for EDK have been added - the CCM core appears in the EDK IP Catalog
- Debugging features have been added
- The AXI4-Lite control interface register map is standardized between Xilinx video cores

From v4.00.a to v5.00.a of the CCM core, the following changes took place:

- The core originally had `aclk`, `aclken` and `aresetn` to control both the Video over AXI4-Stream and AXI4-Lite interfaces. Separate clock, clock enable and reset pins now control the Video over AXI4-Stream and the AXI4-Lite interfaces with clock domain crossing logic added to the core to handle the dissimilar clock domains between the AXI4-Lite and Video over AXI4-Stream domains.

Debugging

It is recommended to prototype the system with the AXI4-Lite interface enabled, so status and error detection, reset, and dynamic size programming can be used during debugging.

The following steps are recommended to bring-up/debug the core in a video/imaging system:

1. Bring up the AXI4-Lite interface
2. Bring up the AXI4-Stream interfaces

Once the core is working as expected, the user may consider 'hardening' the configuration by replacing the CCM core with an instance where GUI default values are set to the established register values, but the AXI4-Lite interface is disabled. This configuration reduces the core slice footprint.

Bringing up the AXI4-Lite Interface

Table C-1 describes how to troubleshoot the AXI4-Lite interface.

Table C-1: **Troubleshooting the AXI4-Lite Interface**

Symptom	Solution
Readback from the Version Register via the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Are the S_AXI_ACLK and ACLK pins connected? In EDK, verify that the S_AXI_ACLK and ACLK pin connections in the system.mhs file. The `VERSION_REGISTER` readout issue may be indicative of the core not receiving the AXI4-Lite interface.
Readback from the Version Register via the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Is the core enabled? Is `s_axi_aclken` connected to `vcc`? In EDK, verify that signal `ACLKEN` is connected in the **`system.mhs`** to either `net_vcc` or to a designated clock enable signal.

Table C-1: **Troubleshooting the AXI4-Lite Interface *(Cont'd)***

Symptom	Solution
Readback from the Version Register via the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Is the core in reset? S_AXI_ARESETn and ARESETn should be connected to `vcc` for the core not to be in reset. In EDK, verify that the S_AXI_ARESETn and ARESETn signals are connected in the **`system.mhs`** to either `net_vcc` or to a designated reset signal.
Readback value for the `VERSION_REGISTER` is different from expected default values	The core and/or the driver in a legacy EDK/SDK project has not been updated. Ensure that old core versions, implementation files, and implementation caches have been cleared.

Assuming the AXI4-Lite interface works, the second step is to bring up the AXI4-Stream interfaces.

Bringing up the AXI4-Stream Interfaces

Table C-2 describes how to troubleshoot the AXI4-Stream interface.

Table C-2: **Troubleshooting AXI4-Stream Interface**

Symptom	Solution
Bit 0 of the `ERROR` register reads back set.	Bit 0 of the `ERROR` register, EOL_EARLY, indicates the number of pixels received between the latest and the preceding End-Of-Line (EOL) signal was less than the value programmed into the `ACTIVE_SIZE` register. If the value was provided by the Video Timing Controller core, read out `ACTIVE_SIZE` register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, using Chipscope, measure the number of active AXI4-Stream transactions between EOL pulses.
Bit 1 of the `ERROR` register reads back set.	Bit 1 of the `ERROR` register, EOL_LATE, indicates the number of pixels received between the last End-Of-Line (EOL) signal surpassed the value programmed into the `ACTIVE_SIZE` register. If the value was provided by the Video Timing Controller core, read out `ACTIVE_SIZE` register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, using Chipscope, measure the number of active AXI4-Stream transactions between EOL pulses.
Bit 2 or Bit 3 of the `ERROR` register reads back set.	Bit 2 of the `ERROR` register, SOF_EARLY, and bit 3 of the `ERROR` register SOF_LATE indicate the number of pixels received between the latest and the preceding Start-Of-Frame (SOF) differ from the value programmed into the `ACTIVE_SIZE` register. If the value was provided by the Video Timing Controller core, read out `ACTIVE_SIZE` register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, using Chipscope, measure the number EOL pulses between subsequent SOF pulses.
s_axis_video_tready stuck low, the upstream core cannot send data.	During initialization, the CCM core keeps its `s_axis_video_tready` input low. Afterwards, the core should assert `s_axis_video_tready` automatically. Is `m_axis_video_tready` low? If so, the CCM core cannot send data downstream, and the internal FIFOs are full.

Table C-2: **Troubleshooting AXI4-Stream Interface**

Symptom	Solution
m_axis_video_tvalid stuck low, the downstream core is not receiving data	If the programmed active number of pixels per line is radically smaller than the actual line length, the core drops most of the pixels waiting for the (s_axis_video_tlast) End-of-line signal. Check the ERROR register.
Generated SOF signal (m_axis_video_tuser0) signal misplaced.	Check the ERROR register.
Generated EOL signal (m_axis_video_tlast) signal misplaced.	Check the ERROR register.
Data samples lost between Upstream core and the CCM core. Inconsistent EOL and/or SOF periods received.	1. Are the Master and Slave AXI4-Stream interfaces in the same clock domain? 2. Is proper clock-domain crossing logic instantiated between the upstream core and the CCM core (Asynchronous FIFO)? 3. Did the design meet timing? 4. Is the frequency of the clock source driving the CCM ACLK pin lower than the reported Fmax reached?
Data samples lost between Downstream core and the CCM core. Inconsistent EOL and/or SOF periods received.	1. Are the Master and Slave AXI4-Stream interfaces in the same clock domain? 2. Is proper clock-domain crossing logic instantiated between the upstream core and the CCM core (Asynchronous FIFO)? 3. Did the design meet timing? 4. Is the frequency of the clock source driving the CCM ACLK pin lower than the reported Fmax reached?

Debugging Features

The CCM core is equipped with optional debugging features which aim to accelerate system bring-up, optimize memory and data-path architecture and reduce time to market. The optional debug features can be turned on/off via the **Include Debug Features** checkbox on the GUI when an AXI4-Lite interface is present. Turning off debug features reduces the core Slice footprint.

Core Bypass Option

The bypass option facilitates establishing a straight through connection between input (AXI4-Stream slave) and output (AXI4-Stream master) interfaces bypassing any processing functionality.

Flag BYPASS (bit 4 of the CONTROL register) can turn bypass on (1) or off, when the core instance Debugging Features were enabled at generation. Within the IP this switch controls multiplexers in the AXI4-Stream path.

In bypass mode the CCM core processing function is bypassed, and the core repeats AXI4-Stream input samples on its output.

Starting a system with all processing cores set to bypass, then by turning bypass off from the system input towards the system output allows verification of subsequent cores with known good stimuli.

Built in Test-Pattern Generator

The optional built-in test-pattern generator facilitates to temporarily feed the output AXI4-Stream master interface with a predefined pattern.

Flag TEST_PATTERN (bit 5 of the CONTROL register) can turn test-pattern generation on (1) or off, when the core instance Debugging Features were enabled at generation. Within the IP this switch controls multiplexers in the AXI4-Stream path, switching between the regular core processing output and the test-pattern generator. When enabled, a set of counters generate 256 scan-lines of color-bars, each color bar 64 pixels wide, repetitively cycling through Black, Red, Green, Yellow, Blue, Magenta, Cyan, and White colors till the end of each scan-line. After the Color-Bars segment, the rest of the frame is filled with a monochrome horizontal and vertical ramp.

Starting a system with all processing cores set to test-pattern mode, then by turning test-pattern generation off from the system output towards the system input allows successive bring-up and parameterization of subsequent cores.

Throughput Monitors

Throughput monitors enable the user to monitor processing performance within the core. This information can be used to help debug frame-buffer bandwidth limitation issues, and if possible, allow video application software to balance memory pathways.

Often times video systems, with multi-port access to a shared external memory, have different processing islands. For example a pre-processing sub-system working in the input video clock domain may clean up, transform, and write a video stream, or multiple video streams, to memory. The processing sub-system may read the frames out, process, scale, encode, then write frames back to the frame buffer, in a separate processing clock domain. Finally, the output sub-system may format the data and read out frames locked to an external clock.

Typically, access to external memory using a multi-port memory controller involves arbitration between competing streams. However, to maximize the throughput of the system, different memory ports may need different specific priorities. To fine tune the

arbitration and dynamically balance frame rates, it is beneficial to have access to throughput information measured in different video data paths.

The SYSDEBUG0 (0x0014), or Frame Throughput Monitor, register indicates the number of frames processed since power-up or the last time the core was reset. The SYSDEBUG1 (0x0018), or Line Throughput Monitor, register indicates the number of lines processed since power-up or the last time the core was reset. The SYSDEBUG2 (0x001C), or Pixel Throughput Monitor, register indicates the number of pixels processed since power-up or the last time the core was reset.

Priorities of memory access points can be modified by the application software dynamically to equalize frame, or partial frame rates.

Interfacing to Third-Party IP

Table C-3 describes how to troubleshoot third-party interfaces.

Table C-3: **Troubleshooting Third-Party Interfaces**

Symptom	Solution
Severe color distortion or color-swap when interfacing to third-party video IP.	Verify that the color component logical addressing on the AXI4-Stream TDATA signal is in according to Data Interface in Chapter 2. If misaligned: In HDL, break up the TDATA vector to constituent components and manually connect the slave and master interface sides. In EDK, create a new vector for the slave side TDATA connection. In the MPD file, manually assign components of the master-side TDATA vector to sections of the new vector.
Severe color distortion or color-swap when processing video written to external memory using the AXI-VDMA core.	Unless the particular software driver was developed with the AXI4-Stream TDATA signal color component assignments described in Data Interface in Chapter 2 in mind, there are no guarantees that the software correctly identifies bits corresponding to color components. Verify that the color component logical addressing TDATA is in alignment with the data format expected by the software drivers reading/writing external memory. If misaligned: In HDL, break up the TDATA vector to constituent components, and manually connect the slave and master interface sides. In EDK, create a new vector for the slave side TDATA connection. In the MPD file, manually assign components of the master-side TDATA vector to sections of the new vector.

Appendix D

Application Software Development

Programmer's Guide

The software API is provided to allow easy access to the CCM AXI4-Lite registers defined in Table 2-9. To utilize the API functions, the following two header files must be included in the user C code:

```
#include "ccm.h"
#include "xparameters.h"
```

The hardware settings of your system, including the base address of your CCM core, are defined in the `xparameters.h` file. The `ccm.h` file contains the macro function definitions for controlling the CCM pCore.

For examples on API function calls and integration into a user application, the drivers subdirectory of the pCore contains a file, `example.c`, in the `ccm_v5_00_a0_a/example` subfolder. This file is a sample C program that demonstrates how to use the CCM pCore API.

Table D-1: **CCM Driver Function Definitions**

Function Name and Parameterization	Description
CCM_Enable (uint32 BaseAddress)	Enables a CCM instance.
CCM_Disable (uint32 BaseAddress)	Disables a CCM instance.
CCM_Reset (uint32 BaseAddress)	Immediately resets a CCM instance. The core stays in reset until the RESET flag is cleared.
CCM_ClearReset (uint32 BaseAddress)	Clears the reset flag of the core, which allows it to re-sync with the input video stream and return to normal operation.
CCM_FSync_Reset (uint32 BaseAddress)	Resets a CCM instance on the next SOF signal.
CCM_ReadReg (uint32 BaseAddress, uint32 RegOffset)	Returns the 32-bit unsigned integer value of the register. Read the register selected by RegOffset (defined in Table 2-12).

Table D-1: **CCM Driver Function Definitions *(Cont'd)***

Function Name and Parameterization	Description
CCM_WriteReg (uint32 BaseAddress, uint32 RegOffset, uint32 Data)	Write the register selected by RegOffset (defined in Table 2-12. Data is the 32-bit value to write to the register.
CCM_RegUpdateEnable (uint32 BaseAddress)	Enables copying double buffered registers at the beginning of the next frame. Refer to Double Buffering for more information.
CCM_RegUpdateDisable (uint32 BaseAddress)	Disables copying double buffered registers at the beginning of the next frame. Refer to Double Buffering for more information.

Software Reset

Software reset reinitializes registers of the AXI4-Lite control interface to their initial value, resets FIFOs, forces `m_axis_video_tvalid` and `s_axis_video_tready` to 0. `CCM_Reset()` and `CCM_AutoSyncReset ()` reset the core immediately if the core is not currently processing a frame. If the core is currently processing a frame calling `CCM_Reset()`, or setting bit 30 of the `CONTROL` register to 1 causes image tearing. After calling `CCM_Reset()`, the core remains in reset until `CCM_ClearReset()` is called.

Calling `CCM_AutoSyncReset()` automates this reset process by waiting until the core finishes processing the current frame, then asserting the reset signal internally, keeping the core in reset only for 32 `ACLK` cycles, then deasserting the signal automatically. After calling `CCM_AutoSyncReset()`, it is not necessary to call `CCM_ClearReset()` for the core to return to normal operating mode.

Note: Calling `CCM_FSync_Reset()` does not guarantee prompt, or real-time reseting of the core. If the AXI4-Stream communication is halted mid frame, the core does not reset until the upstream core finishes sending the current frame or starts a new frame.

Double Buffering

The `ACTIVE_SIZE` register and all of the core specific registers double-buffered to ensure no image tearing happens if values are modified during frame processing. Values from the AXI4-Lite interface are latched into processor registers immediately after writing, and processor register values are copied into the active register set at the Start Of Frame (SOF) signal. Double-buffering decouples AXI4-Lite register updates from the AXI4-Stream processing, allowing software a large window of opportunity to update processing parameter values without image tearing.

If multiple register values are changed during frame processing, simple double buffering would not guarantee that all register updates would take effect at the beginning of the same frame. Using a semaphore mechanism, the `RegUpdateEnable()` and `RegUpdateDisable()` functions allows synchronous commitment of register changes. The CCM core starts using the updated `ACTIVE_SIZE` and core-specific values only if the `REGUPDATE` flag of the `CONTROL` register is set (1), after the next Start-Of-Frame signal

(s_axis_video_tuser0) is received. Therefore, it is recommended to disable the register update before writing multiple double-buffered registers, then enable register update when register writes are completed.

Reading and Writing Registers

Each software register that is defined in Table 2-12 has a constant that is defined in ccm.h which is set to the offset for that register listed in Table D-2. It is recommended that the application software uses the predefined register names instead of register values when accessing core registers, so future updates to the CCM drivers which may change register locations does not affect the application dependent on the CCM driver.

Table D-2: **Predefined Constants Defined in ccm.h**

Constant Name Definition	Value	Target Register
CCM_CONTROL	0x0000	CONTROL
CCM_STATUS	0x0004	STATUS
CCM_ERROR	0x0008	ERROR
CCM_IRQ_ENABLE	0x000C	IRQ_ENABLE
CCM_VERSION	0x0010	VERSION
CCM_SYSDEBUG0	0x0014	SYSDEBUG0
CCM_SYSDEBUG1	0x0018	SYSDEBUG1
CCM_SYSDEBUG2	0x001C	SYSDEBUG2
CCM_ACTIVE_SIZE	0x0020	ACTIVE_SIZE
CCM_K11	0x0100	MATRIX COEFFICIENT
CCM_K12	0x0104	MATRIX COEFFICIENT
CCM_K13	0x0108	MATRIX COEFFICIENT
CCM_K21	0x010C	MATRIX COEFFICIENT
CCM_K22	0x0110	MATRIX COEFFICIENT
CCM_K23	0x0114	MATRIX COEFFICIENT
CCM_K31	0x0118	MATRIX COEFFICIENT
CCM_K32	0x011C	MATRIX COEFFICIENT
CCM_K33	0x0120	MATRIX COEFFICIENT
CCM_ROFFSET	0x0124	RED OFFSET
CCM_GOFFSET	0x0128	GREEN OFFSET
CCM_BOFFSET	0x012C	BLUE OFFSET
CCM_CLIP	0x0130	CLIP
CCM_CLAMP	0x0134	CLAMP

Appendix E

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

http://www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/company/terms.htm.

For a comprehensive listing of Video and Imaging application notes, white papers, reference designs and related IP cores, see the Video and Imaging Resources page at:

http://www.xilinx.com/esp/video/refdes_listing.htm#ref_des.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents provide supplemental material useful with this user guide:

1. UG761 AXI Reference Guide.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the *IP Release Notes Guide* (XTP025) for more information on this core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Resolved Issues
- Known Issues

Ordering Information

The Color Correction Matrix v4.00.a core is provided under the Xilinx Core License Agreement and can be generated using the Xilinx® CORE Generator™ system and EDK software. The CORE Generator system is shipped with Xilinx ISE® Design Suite software. The CORE Generator system and EDK are shipped with the Xilinx ISE Embedded Edition Design software.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/19/2011	1.0	Initial Xilinx release of Product Guide, replacing DS720 and UG830.
4/24/2012	2.0	Updated for core version. Added Zynq-7000 devices, added AXI4-Stream interfaces, deprecated GPP interface.
07/25/2012	3.0	Updated for core version. Added Vivado information.

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