LogiCORE IP Virtex-6 FPGA Integrated Block v2.5 for PCI Express

DS800 January 18, 2012 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-6 FPGA Integrated Block for PCI Express® core is a high-bandwidth, scalable, and reliable serial interconnect building block for use with Virtex-6 FPGAs. The Integrated Block for PCI Express (PCIe®) solution supports 1-lane, 2-lane, 4-lane, and 8-lane Endpoint and Root Port configurations at up to Gen2 (5 GT/s) speeds, all of which are compliant with the *PCI Express Base Specification, rev. 2.0*. This solution supports the AMBA® AXI4-Stream interface for the customer user interface.

PCI Express offers a serial architecture that alleviates many of the limitations of parallel bus architectures by using clock data recovery (CDR) and differential signaling. Using CDR (as opposed to source synchronous clocking) lowers pin count, enables superior frequency scalability, and makes data synchronization easier. The layered architecture of PCI Express provides for future attachment to copper, optical, or emerging physical signaling media. PCI Express technology, adopted by the PCI-SIG® as the next generation PCI™, is backward-compatible to the existing PCI software model.

With higher bandwidth per pin, low overhead, low latency, reduced signal integrity issues, and CDR architecture, the Integrated Block for PCIe sets the industry standard for a high-performance, cost-efficient third-generation I/O solution.

The Integrated Block for PCI Express solution is compatible with industry-standard application form factors such as the *PCI Express Card Electromechanical (CEM) v2.0* and the *PCI Industrial Computer Manufacturers Group (PICMG) 3.4* specifications.

LogiCORE IP Facts Table	
Core Specifics	
Supported FPGA Families(1)	Virtex-6(2)
Minimum Device	XC6VLX75T-1(3)
Supported User Interfaces	AXI4-Stream
Resources	See Table 2
Special Features	GTXE1 Transceivers, Virtex-6 FPGA Integrated Block for PCI Express, Virtex-6 FPGA MMCM, Block RAM
Provided with Core	
Documentation	Product Specification, User Guide, Instantiation Template
Design Files	Verilog RTL and VHDL Source and Simulation Models Verilog and VHDL Test Bench, Verilog and VHDL Example Design
Constraints File	User Constraints File (UCF)
Supported S/W Driver	N/A
Design Tool Support	
HDL Synthesis Tool	XST v13.4 Synopsys Synplify Pro(4)
Xilinx Implementation Tools	ISE® v13.4
Simulation Tools(5)	Cadence Incisive Enterprise Simulator Synopsys VCS and VCS MX Mentor Graphics ModelSim Xilinx ISim v13.4
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For the complete list of supported devices, see the release notes for this core.
2. Virtex-6 FPGA solutions require the latest production silicon; the LogiCORE IP warranty does not include production usage with engineering sample silicon.
3. Designs needing 8-lane operation with Gen2 (5 GT/s) speeds must use the 128-bit version of the product. See Table 1 for supported devices and speed grades.
4. For a listing of the supported tool versions, see the ISE Design Suite 13: Release Note Guide.
5. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator.

Table 1: **8-Lane Gen2 (5.0 GT/s) Product Support**

Speed Grade	CMPS	Supported Devices
-3	Up to 512 bytes	All LXT, SXT and HXT parts.
-2	Up to 256 bytes	All SXT, HXT and LXT parts except LX365T and LX550T.(1)
-1	-	Not supported.

1. XC6VLX365T and XC6VLX550T are not supported in a -2 speed grade device.

Table 2: **Resources Used**

Product	Interface Width	GTXE1	LUT(1)	FF(2)	Rx Buffers Size (KB)	Tx Buffers Size (KB)	CMPS(2) (Bytes)	Block RAM
1-lane Gen1(3)/Gen2(4)	64-bit	1	375	425	8 or 16	4-32	128-1024	4 or 8
2-lane Gen1/Gen2	64-bit	2	525	525				
4-lane Gen1/Gen2	64-bit	4	775	700				
8-lane, Gen1	64-bit	8	1300	1100				
8-lane, Gen2(5)	128-bit	8	1800	3300				

1. Numbers are for the default core configuration. Actual LUT and FF utilization values vary based on specific configurations.
2. Capability Maximum Payload Size (CMPS).
3. Gen1 = 2.5 GT/s.
4. Gen2 = 5.0 GT/s.
5. The 8-lane Gen2 product is only supported for the Endpoint configuration.

Features

- High-performance, highly flexible, scalable, and reliable, general-purpose I/O core
  - Compliant with the *PCI Express Base Specification, rev. 2.0*
  - Compatible with conventional PCI software model
- Incorporates Xilinx Smart-IP technology to guarantee critical timing
- Uses GTXE1 transceivers for Virtex-6 LXT, SXT and HXT devices
  - 2.5 GT/s and 5.0 GT/s line speeds
  - Supports 1-lane, 2-lane, 4-lane, and 8-lane operation
  - Elastic buffers and clock compensation
  - Automatic clock data recovery
- Supports Endpoint and Root Port configurations
- 8B/10B encode and decode
- Supports Lane Reversal and Lane Polarity Inversion per PCI Express specification requirements
- Standardized user interface
  - Supports AXI4-Stream interface
  - Easy-to-use packet-based protocol
  - Full-duplex communication
  - Back-to-back transactions enable greater link bandwidth utilization
  - Supports flow control of data and discontinuation of an in-process transaction in transmit direction
  - Supports flow control of data in receive direction

- Compliant with PCI and PCI Express power management functions
- Supports a maximum transaction payload of up to 1024 bytes
- Supports Multi-Vector MSI for up to 32 vectors and MSI-X
- Up-configure capability enables application driven bandwidth scalability
- Compliant with PCI Express transaction ordering rules

Applications

The Integrated Block for PCI Express architecture enables a broad range of computing and communications target applications, emphasizing performance, cost, scalability, feature extensibility and mission-critical reliability. Typical applications include

- Data communications networks
- Telecommunications networks
- Broadband wired and wireless applications
- Cross-connects
- Network interface cards
- Chip-to-chip and backplane interconnect
- Crossbar switches
- Wireless base stations

Functional Description

For information about the internal architecture and detailed descriptions of the interfaces of the Virtex-6 FPGA Integrated Block, see *Virtex-6 FPGA Integrated Block for PCI Express User Guide*. Figure 1 illustrates the interfaces to the core.

- System (SYS) Interface
- PCI Express (PCI EXP) Interface
- Physical Layer Control and Status (PL) Interface
- Configuration (CFG) Interface
- AXI4-Stream Interface

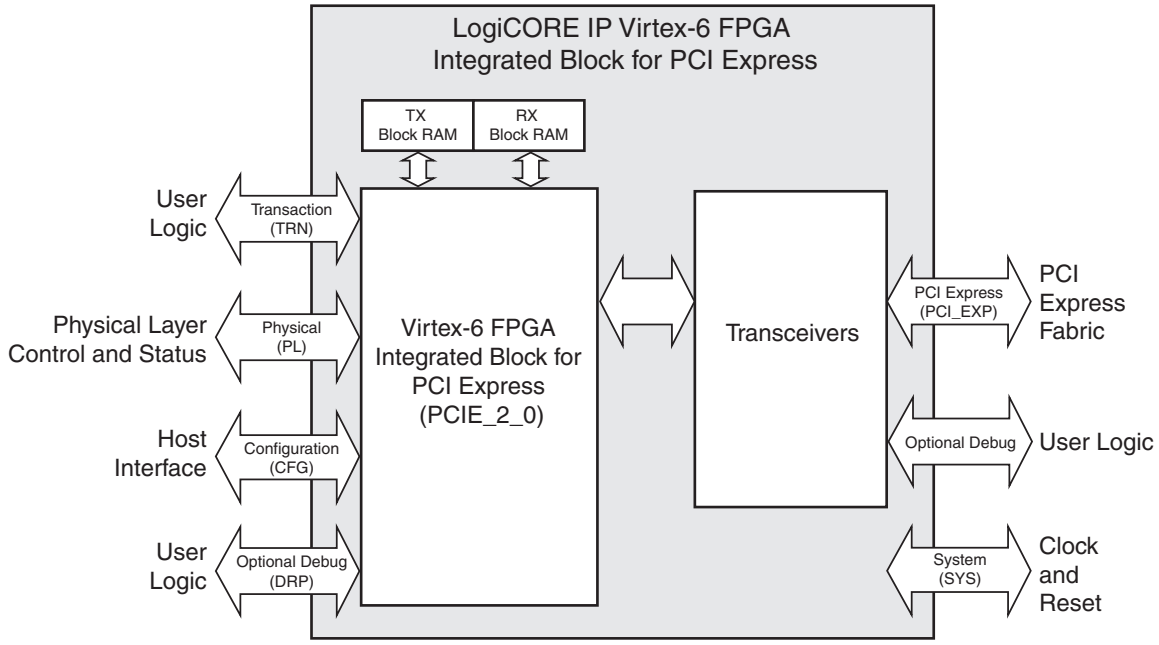

Figure 1: **Integrated Block for PCI Express Top-Level Functional Blocks and Interfaces**

Protocol Layers

The Integrated Block for PCIe follows the *PCI Express Base Specification, rev. 2.0* layering model, which consists of the Physical, Data Link, and Transaction Layers. The protocol uses packets to exchange information between layers. Packets are formed in the Transaction and Data Link Layers to carry information from the transmitting component to the receiving component. Necessary information is added to the packet being transmitted, which is required to handle the packet at specific layers.

At the receiving end, each layer of the receiving element processes the incoming packet, strips the relevant information and forwards the packet to the next layer. As a result, the received packets are transformed from their Physical Layer representation to their Data Link Layer representation and Transaction Layer representation.

The functions of the protocol layers include:

- Generating and processing of TLPs
- Flow-control management
- Initialization and power management functions
- Data protection
- Error checking and retry functions
- Physical link interface initialization
- Maintenance and status tracking
- Serialization, deserialization, and other circuitry for interface operation

Each of the protocol layers are defined in the sections that follow.

Physical Layer

The Physical Layer exchanges information with the Data Link Layer in an implementation-specific format. This layer is responsible for converting information received from the Data Link Layer into an

appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

Data Link Layer

The Data Link Layer acts as an intermediate stage between the Transaction Layer and the Physical Layer. Its primary responsibility is to provide a reliable mechanism for the exchange of Transaction Layer Packets (TLPs) between the two Components on a Link.

Services provided by the Data Link Layer include data exchange (TLPs), error detection and recovery, initialization services and the generation and consumption of Data Link Layer Packets (DLLPs). DLLPs are the mechanism used to transfer information between Data Link Layers of two directly connected components on the Link. DLLPs are used for conveying information such as Flow Control and TLP acknowledgments.

Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The primary function of the Transaction Layer is the assembly and disassembly of Transaction Layer Packets (TLPs). Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. TLPs are used to communicate transactions, such as read and write, as well as certain types of events. To maximize the efficiency of communication between devices, the Transaction Layer implements a pipelined, full split-transaction protocol and manages credit-based flow control of TLPs.

Configuration Management

The Configuration Management Layer supports generation and reception of System Management Messages by communicating with the other layers and the user application. This layer contains the device configuration space and other system functions. The Configuration layer implements PCI and PCI Express power management capabilities, and facilitates exchange of power management messages, including support for PME event generation. Also implemented are user-triggered error message generation, and user-read access to the device configuration space.

PCI Configuration Space

The configuration space consists of three primary parts. These include:

- Legacy PCI v3.0 Type 0/1 Configuration Space Header
  - Type 0 Configuration Space Header, used by Endpoint applications
  - Type 1 Configuration Space Header, used by Root Port applications
- Legacy Extended Capability Items
  - PCIe Capability Item
  - Power Management Capability Item
  - Message Signaled Interrupt (MSI) Capability Item
  - MSI-X Capability Item (optional)
- PCIe Extended Capabilities
  - Device Serial Number Extended Capability (optional)
  - Virtual Channel Extended Capability (optional)
  - Vendor Specific Extended Capability (optional)

These capabilities, together with the standard Type 0/1 header, support software driven *Plug and Play* initialization and configuration.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Virtex-6 FPGA Integrated Block for PCI Express is included with the ISE CORE Generator™ tool. No license key is required.

References

These documents provide supplemental information useful with this data sheet:

- *AMBA AXI4-Stream Protocol Specification*
- *PCI Express Base Specification 2.0* (www.pcisig.com/specifications)
- Xilinx Documentation (xilinx.com/support)
  - UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
  - UG671, *Virtex-6 FPGA Integrated Block for PCI Express User Guide*
  - UG761, *Xilinx AXI Reference Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/21/10	1.0	Initial Xilinx release.
12/14/10	2.0	Updated for core v2.2 and ISE 12.4 software release.
03/01/11	3.0	Updated for core v2.3 and ISE 13.1 software release.
06/22/11	4.0	Updated for core v2.4 and ISE 13.2 software release.
01/18/12	4.1	Updated for core v2.5 and ISE 13.4 software release.

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