LogiCORE IP Virtex-6 FPGA GTH Transceiver Wizard v1.6

DS738 December 14, 2010 **Product Specification**

Introduction

The LogiCORE™ IP GTH Transceiver Wizard automates the task of creating HDL wrappers to configure the high-speed serial GTH transceivers in the Virtex®-6 HXT family (specifically, XC6VHX255T, XC6VHX380T, and XC6VHX565T).

The menu-driven interface allows one or more GTH transceivers to be configured using predefined templates for popular industry standards, or from scratch, to support a wide variety of custom protocols. The Wizard produces a wrapper, an example design, and a test bench for rapid integration and verification of the serial interface with your custom function.

Features

- Creates customized HDL wrappers to configure Virtex-6 family GTH transceivers
- Virtex-6 family GTH transceivers can be configured to conform to industry standard protocols using predefined templates, or tailor the templates for custom protocols
- Templates include support for the following specifications: 10G Base-R, CAUI, OC-48, OC-192, OTU-1, OTU-2, OTU-4, XLAUI, and Aurora 64B/66B
- Automatically configures analog settings
- Each custom wrapper includes the example design, test bench, and both implementation and simulation scripts.

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family (1)	Virtex-6 (2) HXT				
Supported User Interfaces	Not Applicable				
	Resources				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	Not Applicable				
Provided with Core					
Documentation	Product Specification Getting Started Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Test Bench	Verilog and VHDL				
Constraints File	User Constraints File (.ucf)				
Simulation Model	Verilog and VHDL				
Tested Design Tools					
Design Entry Tools	ISE® software 12.4 CORE Generator™ tool 12.4				
Simulation	ISim 12.4 Mentor Graphics ModelSim 6.5c Cadence IES (3) 9.2 Synopsys VCS and VCS MX 2009.12				
Synthesis Tools	XST 12.4				
Support					
Provided by Xilinx, Inc.					

Notes:

1. For a complete list of supported devices, see the release notes for this core.
2. For more information on the Virtex-6 devices, see the *Virtex-6 Family Overview* [Ref 1].
3. Cadence Incisive Enterprise Simulator (IES)

Functional Overview

Figure 1 shows the steps required to configure GTH transceivers using the Wizard. Start the CORE Generator software and select the GTH Transceiver Wizard, then follow the chart to configure the transceivers and generate a wrapper that includes an accompanying example design.

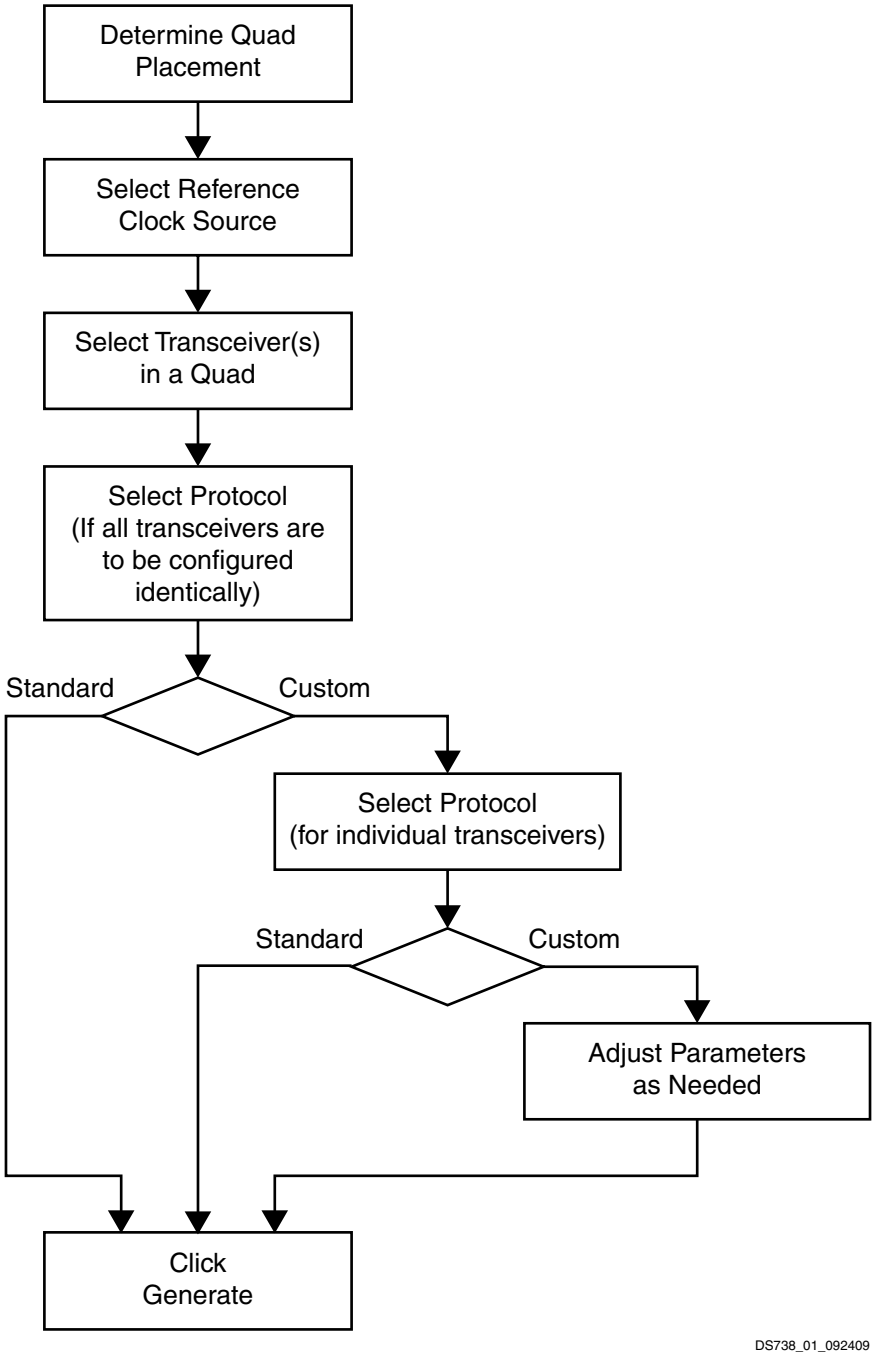

Figure 1: **GTH Wizard Configuration Steps**

See the *Virtex-6 FPGA GTH Transceivers User Guide* [Ref 3] for details on the various transceiver features and parameters available.

Wrapper Overview

Figure 2 shows the block diagram of the wrapper, example design, and test bench produced by the Wizard.

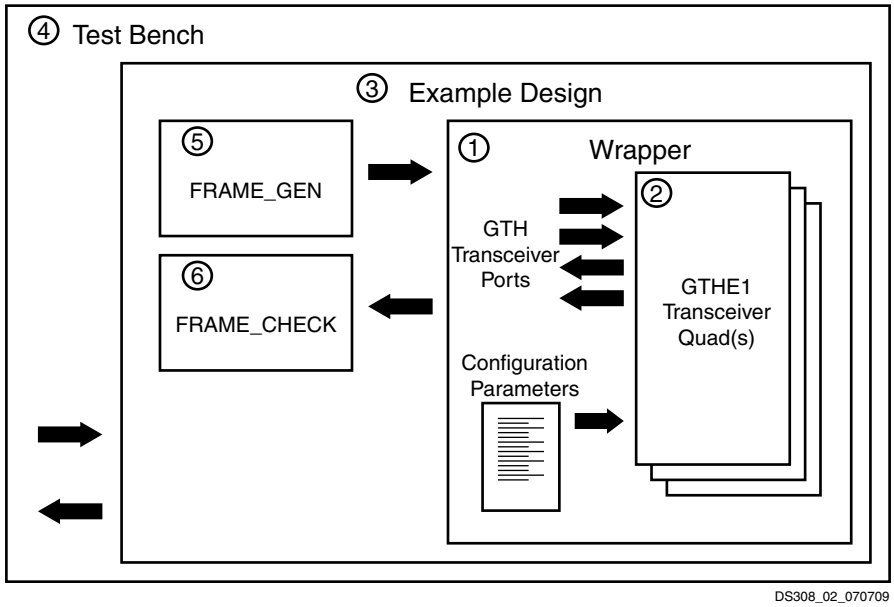

Figure 2: **Wrapper Block Diagram**

The wrapper comprises six components:

1. Wrapper: The specific GTH transceiver configuration parameters set with the Wizard.
2. GTHE1 Transceiver Quad(s): Instantiated transceivers selected with the Wizard.
3. Example Design: Temporary top-level design that will be replaced with the actual application.
4. Test Bench: Top-level test bench to aid in simulation of the design.
5. FRAME_GEN Module: Generates a user-definable data stream for simulation analysis.
6. FRAME_CHECK Module: Tests for correct transmission of data stream for simulation analysis.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Virtex-6 FPGA GTH Transceiver Wizard LogiCORE IP core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated by the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.4. For more information, please visit the Architecture Wizards web page. Information about additional Xilinx LogiCORE modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. DS150: *Virtex-6 Family Overview*
2. UG619: *LogiCORE IP Virtex-6 FPGA GTH Transceiver Wizard v1.6 Getting Started Guide* for a general overview of the wrapper creation procedure
3. UG371: *Virtex-6 FPGA GTH Transceivers User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
09/16/09	1.1	Initial Xilinx release.
12/02/09	1.2	Tools and Wizard updates.
04/19/10	1.3	Tools and Wizard 1.3 updates. Added Ordering Information.
07/23/10	1.4	Tools and Wizard updates.
09/21/10	1.5	Tools and Wizard updates.
12/14/10	1.6	Tools and Wizard updates.

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