Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC Wrapper v4.8

DS307 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-4 Embedded Tri-Mode Ethernet Media Access Controller (MAC) Wrapper automates the generation of HDL wrapper files for the Tri-Mode Ethernet MAC in Virtex-4 FX devices using the CORE Generator™ software.

VHDL and Verilog instantiation templates are available in the Libraries Guide for the Virtex-4 FPGA Ethernet MAC primitive; however, due to the complexity and the large number of ports, the CORE Generator software simplifies integration of the Ethernet MAC by providing HDL examples based on user-selectable configurations.

Features

- Allows selection of one or both Ethernet MACs (EMAC0/EMAC1) from the Embedded Ethernet MAC primitive
- Connects the EMAC0/EMAC1 tie-off pins based on user options
- Provides user-configurable Ethernet MAC physical interfaces, including
  - ♦ Supports MII, GMII, RGMII v1.3, RGMII v2.0, SGMII, and 1000BASE-X PCS/PMA interfaces
  - ♦ Instantiates clock buffers, DCMs, RocketIO™ Multi-Gigabit Transceivers (MGTs), and logic as required for the selected physical interfaces
- Provides a simple FIFO-loopback example design, which is connected to the MAC client interfaces
- Provides a simple demonstration test bench based on the selected configuration
- Includes an example of a low-level driver for DCR accesses
- Generates VHDL or Verilog

LogiCORE IP Facts	
Supported Family[1]	Virtex-4 FX
Performance	10 Mbps, 100 Mbps, 1 Gbps
Example Design Resources	
Slices	510-1510[2]
LUTs	460-1450[2]
FFs	490-1450[2]
Block RAMs	4-10[2]
DCM	0-2[2]
BUFG	2-8[2]
Wrapper Highlights	
Optimized Clocking Logic	HDL Example Design
Hardware Verified	Demonstration Test Bench
Provided with Wrapper	
Documentation	Product Specification Getting Started Guide User Guide[3]
Design File Formats	HDL Example Design, Demonstration Test Bench, Scripts
Constraints File	User Constraints File (UCF)
Example Designs	Example FIFO connected to client I/F
	Demonstration Test Environment
Design Tool Requirements	
Supported HDL	VHDL and/or Verilog
Synthesis	XST 12.1
Xilinx Tools	ISE® 12.1
Simulation Tools[4]	Mentor Graphics ModelSim v6.5c Cadence Incisive Enterprise Simulator (IES) v9.2[5]

1. For the complete list of supported devices, see the 12.1 release notes for this core.
2. The precise number depends on the user configuration; see "Device Utilization" on page 7.
3. The *Virtex-4 Embedded Tri-Mode Ethernet MAC User Guide* is available from the Virtex-4 User Guides page.
4. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.
5. Scripts provided for Mentor ModelSim and Cadence INCISIV only.

Ethernet Architecture Overview

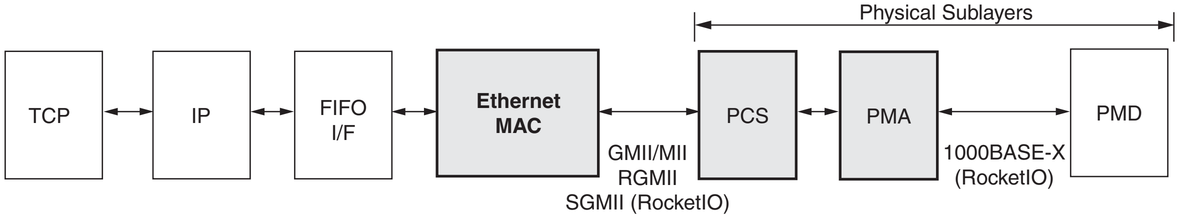

Figure 1: **Typical Ethernet Architecture**

Figure 1 displays the Ethernet MAC architecture from the MAC to the right, as defined in the *IEEE 802.3* specification, and also illustrates where the supported physical interfaces fit into the architecture.

MAC

The Ethernet MAC is defined in the *IEEE 802.3* specification clauses 2, 3, and 4. A MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can connect to, any type of physical sublayer.

GMII/MII

The Media Independent Interface (MII), defined in *IEEE 802.3* clause 22, is a parallel interface that connects a 10-Mbps and/or 100-Mbps capable MAC to the physical sublayers. The Gigabit Media Independent Interface (GMII), defined in *IEEE 802.3* clause 35, is an extension of the MII used to connect a 1-Gbps capable MAC to the physical sublayers. MII can be considered a subset of GMII, and as a result, GMII/MII can carry Ethernet traffic at 10 Mbps, 100 Mbps, and 1 Gbps.

RGMII

The Reduced-GMII (RGMII) is an alternative to the GMII/MII. RGMII achieves a 45 percent reduction in the pin count, achieved by the use of double-data-rate (DDR) flip-flops. For this reason, RGMII is preferred over GMII by PCB designers. RGMII can carry Ethernet traffic at 10 Mbps, 100 Mbps, and 1 Gbps.

SGMII

The Serial-GMII (SGMII) interface is an alternative to the GMII/MII. SGMII converts the parallel interface of the GMII/MII into a serial format using a RocketIO transceiver, radically reducing the I/O count. For this reason, it is often the preferred interface of PCB designers. SGMII can carry Ethernet traffic at 10 Mbps, 100 Mbps, and 1 Gbps.

PCS, PMA, PMD

The combination of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and the Physical Medium Dependent (PMD) sublayer comprise the physical layers of the Ethernet protocol.

Two main physical standards are specified for Ethernet:

- BASE-T, a copper standard using twisted pair cabling systems
- BASE-X, usually a fibre optical physical standard using short and long wavelength laser

BASE-T devices, supporting 10 Mbps, 100 Mbps, and 1 Gbps Ethernet speeds, are readily available as off-the-shelf parts. As illustrated in Figures 1 and 2, these can be connected using GMII/MII, RGMII, or SGMII to provide a tri-speed Ethernet port.

The Ethernet MAC has built-in 1000BASE-X PCS/PMA functionality and can be connected to a RocketIO transceiver to provide a 1 Gbps fibre optic port, as illustrated in Figure 3.

Applications

Typical applications for the Ethernet MAC core include

- Ethernet Tri-Speed BASE-T Port
- Ethernet 1000BASE-X Port

Ethernet Tri-Speed BASE-T Port

Figure 2 illustrates a typical application for a single Ethernet MAC. The PHY side of the core is implementing an external GMII/MII by connecting it to IOBs; the external GMII/MII is connected to an off-the-shelf Ethernet PHY device, which performs the BASE-T standard at 1 Gbps, 100 Mbps, and 10 Mbps speeds. Alternatively, the external GMII/MII can be replaced with an RGMII (as shown) or as an SGMII (which requires the use of a RocketIO transceiver). GMII, RGMII, and SGMII functionality are demonstrated in the HDL examples provided with the example design.

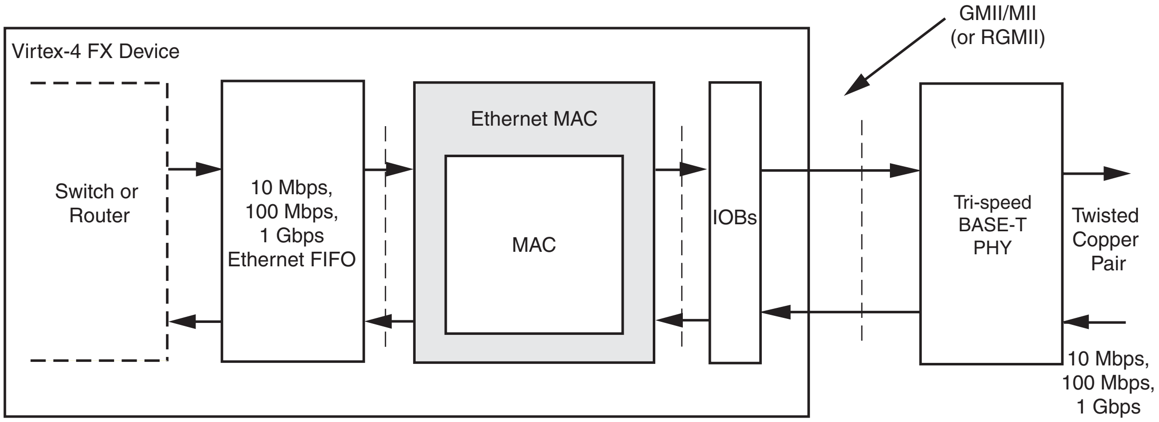

Figure 2: **Typical 1000BASE-T Application**

Ethernet 1000BASE-X Port

Figure 3 illustrates a typical application for a single Ethernet MAC. The PHY side of the MAC is connected to a RocketIO transceiver, which in turn is connected to an external off-the-shelf GBIC or SFP optical transceiver. The 1000BASE-X logic can be optionally provided by the Ethernet MAC, as displayed. 1000BASE-X functionality is demonstrated in the HDL examples provided with the example design.

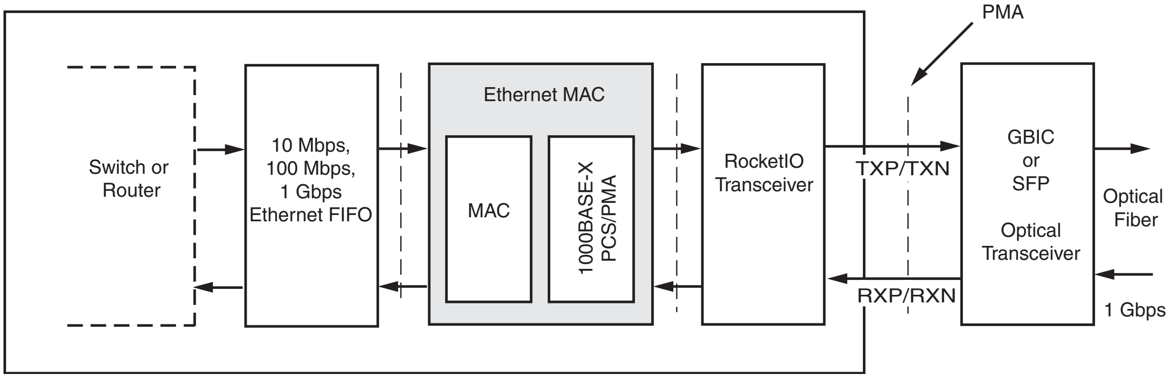

Figure 3: **Typical 1000BASE-X Application**

Example Design Overview

Figure 4 displays the major functional blocks of the Virtex-4 FPGA Tri-Mode Ethernet MAC example design. All illustrated components are provided in HDL with the exception of the Ethernet MAC itself.

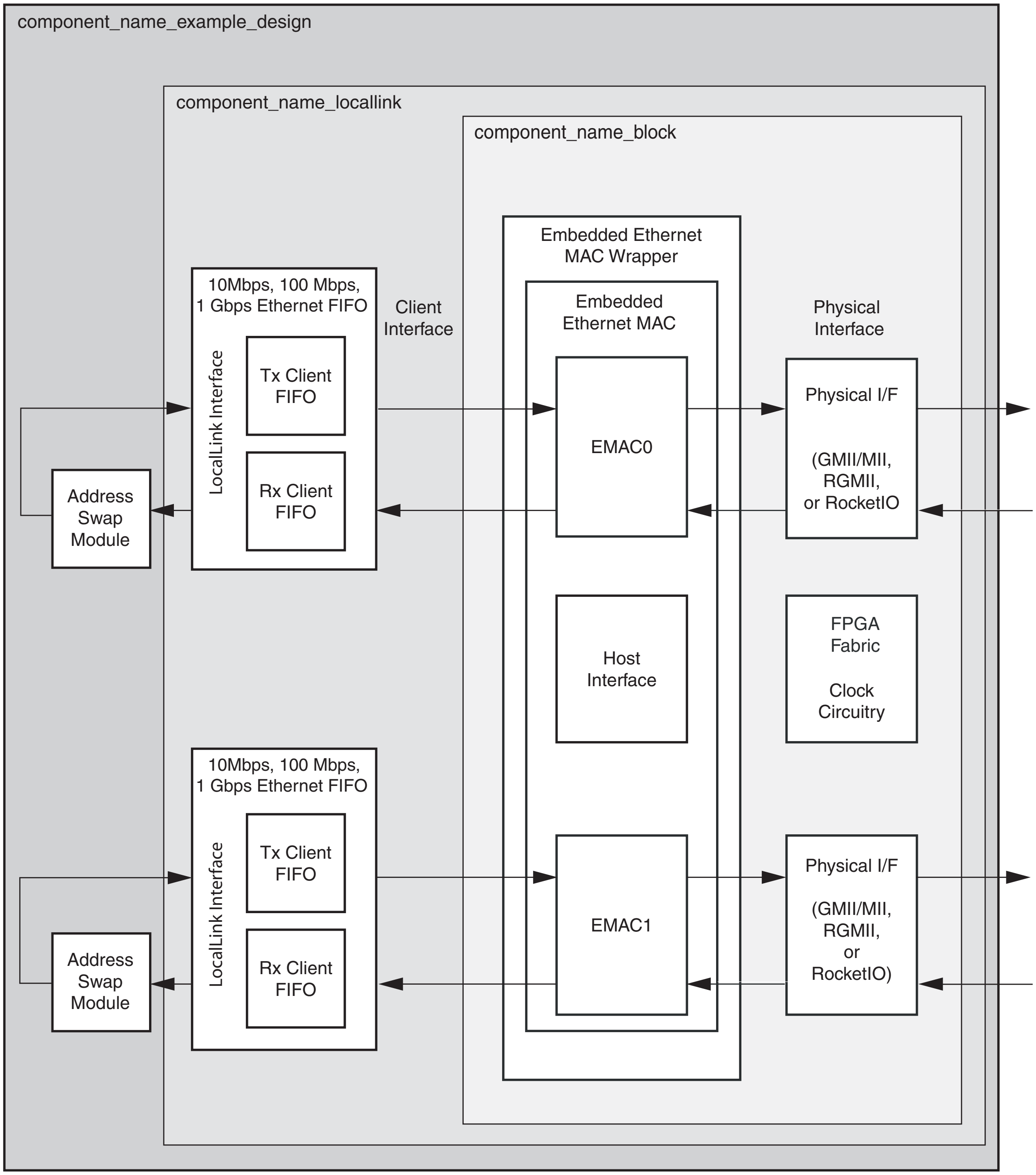

Figure 4: **Example Design**

Ethernet MAC Example Design

The example design is designed for quick adaptation and can be downloaded onto an FPGA to provide a real hardware test environment, and includes all the clock management logic required to operate the Ethernet MAC and its example design. DCMs, BUFGs, and so forth, are instantiated as required.

In the example design, the data is looped back at the client interface, enabling the Ethernet MAC to be quickly connected to a protocol tester—frames injected into the Ethernet MAC PHY Receive port are relayed back through the Ethernet MAC and out through the Ethernet MACs PHY Transmit port. Using this method, they are received back at the protocol tester.

The design includes an Address Swapping Module and a FIFO. Frames received by the Ethernet MAC are passed through the Receive side of the FIFO. Data from the Receive side of the FIFO is passed into the Address Swap Module and then on to the Transmit side of the FIFO using a LocalLink interface. The Transmit FIFO queues frames for transmission and connects directly to the client side Transmit interface of the Ethernet MAC.

Address Swap Module

The Address Swap Module switches the Destination Address and Source Address within the received MAC frame. Using this method, frames received from a link partner, for example a protocol tester, are relayed back to the correct Destination Address.

10 Mbps, 100 Mbps, 1 Gbps Ethernet FIFO

The 10 Mbps, 100 Mbps, 1 Gbps Ethernet FIFO is a wrapper file around the Receive and Transmit FIFO components. These components can be used in more complex client applications, as illustrated in Figures 2 and 3. To use the FIFOs, the component_name_locallink component can be instantiated in the user design.

Receive Client FIFO

The Receive (Rx) Client FIFO, a 4k-byte FIFO implemented in block RAMs, can be used for more complex client applications and can be connected directly to the Rx Client Interface of the Ethernet MAC. The Rx Client provides a LocalLink connection for the user.

- The FIFO operates at all Ethernet speeds supported by the Ethernet MAC.
- The FIFO drops all frames marked as bad from the Ethernet MAC so that only error-free frames are passed to the Ethernet client.

Transmit (Tx) Client FIFO

The Transmit (Tx) Client FIFO, a 4k-byte FIFO implemented in block RAMs, can used for more complex client applications and can be connected directly to the Tx Client Interface of the Ethernet MAC. The Tx Client FIFO provides a LocalLink connection for the user.

- The FIFO operates at all Ethernet speeds supported by the Ethernet MAC.
- The FIFO is capable of half-duplex re-transmission. For this reason, if a collision occurs on the medium, the Ethernet MAC indicates a collision on the Tx Client interface and the FIFO automatically re-queues the frame for re-transmission.

Ethernet MAC Wrapper

The Ethernet MAC wrapper file instantiates the full Ethernet MAC primitive. For one or both Ethernet MACs (EMAC0/EMAC1), the following applies:

- All unused input ports on the primitive are tied to the appropriate logic level; all unused output ports are left unconnected.
- Tie-off vectors are connected based on options selected in the CORE Generator tool.
- Only used ports are connected to the ports of the wrapper file.

This simplified wrapper should be used as the instantiation template for the Ethernet MAC in customer designs.

Physical I/F

An appropriate Physical Interface is provided for each selected EMAC0/EMAC1. This interface connects the physical interface of the Ethernet MAC block to the I/O of the FPGA. As required, the following components are provided:

- For GMII/MII, this component contains Input/Output block (IOB) buffers and IOB flip-flops.
- For RGMII, this component contains contain IOB buffers and IOB Double-Data Rate flip-flops.
- For 1000BASE-X PCS/PMA or SGMII, this component instantiates and connects RocketIO transceiver(s).

Device Utilization

The following sections provide approximate device-utilization figures for common configurations of the Ethernet MAC and its example design, and are separated into the following sections:

- 1 Gbps Only Operation
- Tri-speed Operation
- 100 Mbps or 10 Mbps Operation

Of interest is the utilization of clock resources, specifically the global clock usage (BUFGs), which should influence the type of interface selected. These clock resource figures do not consider any clock buffers, which may be required for the Host Interface.

1 Gbps Only Operation

Table 1 defines approximate utilization figures for common configurations of the Tri-Mode Ethernet MAC and its example design when supporting 1 Gbps only operation.

Table 1: **Device Utilization for 1 Gbps Operation**

Parameter Values		Device Resources					
Physical Interface	**Ethernet MAC Usage**	**Slices**	**LUTs**	**Registers**	**Block RAMs**	**BUFGs**	**DCMs**
GMII	Single EMAC	560	490	500	4	2	1
	Both EMACs	950	990	980	8	3	2
RGMII 1.3	Single EMAC	540	490	490	4	2	1
	Both EMACs	970	990	960	8	3	2
RGMII 2.0	Single EMAC	540	490	490	4	2[1]	1
	Both EMACs	980	990	960	8	3[1]	2
SGMII	Single EMAC	610	675	620	4	2	0
	Both EMACs	1140	1280	1110	8	2	0
1000BASE-X (8-bit client)	Single EMAC	610	680	620	4	2	0
	Both EMACs	1140	1280	1110	8	2	0
1000BASE-X (16-bit client)	Single EMAC	760	670	780	4	6	1
	Both EMACs	1400	1220	1390	8	6	1

[1] These implementations use IDELAY elements, which require a 200 MHz reference clock for the associated IDELAYCTRL. The reference clock's BUFG is not accounted for.

Tri-speed Operation

Table 2 provides approximate utilization figures for common configurations of the Tri-Mode Ethernet MAC and its example design when operating at 10 Mbps, 100 Mbps, or 1 Gbps.

Table 2: **Device Utilization for Tri-speed Operation**

Parameter Values		Device Resources					
Physical Interface	**Ethernet MAC Usage**	**Slices**	**LUTs**	**Registers**	**Block RAMs**	**BUFGs**	**DCMs**
GMII/MII (standard clocking)	Single EMAC	590	540	530	4	4	1
	Both EMACs	1140	1040	1060	8	8	2
GMII/MII (advanced clocking: full duplex mode only)	Single EMAC	570	480	530	4	2	1
	Both EMACs	1040	950	1060	8	4	2
RGMII 1.3	Single EMAC	510	490	490	4	4	1
	Both EMACs	980	990	970	8	8	2
RGMII 2.0	Single EMAC	530	500	490	4	4[1]	1
	Both EMACs	1000	1000	970	8	8[1]	2
SGMII	Single EMAC	780	790	780	5	3	0
	Both EMACs	1510	1450	1450	10	4	0

[1] These implementations use IDELAY elements, which require a 200 MHz reference clock for the associated IDELAYCTRL. The reference clock's BUFG is not accounted for.

100 Mbps or 10 Mbps Operation

Table 3 provides approximate utilization figures for common configurations of the Tri-Mode Ethernet MAC and its example design when operating at 10 Mbps or 100 Mbps.

Note: For all other interfaces, see Tri-speed Operation.

Table 3: **Device Utilization for 10 Mbps, 100 Mbps Operation**

Parameter Values		Device Resources					
Physical Interface	**Ethernet MAC Usage**	**Slices**	**LUTs**	**Registers**	**Block RAMs**	**BUFGs**	**DCMs**
MII (standard clocking)	Single EMAC	530	510	480	4	4	0
	Both EMACs	970	970	950	8	8	0
MII (advanced clocking: clock enables)	Single EMAC	480	460	490	4	2	0
	Both EMACS	890	910	970	8	4	0

Ordering Information

The Ethernet MAC wrapper is provided under the End User License Agreement and can be generated using CORE Generator software v12.1 and higher. The CORE Generator software is shipped with Xilinx ISE Design Suite Series Development software.

In ISE v12.1 and later, a license key is not required to access the IP. To access the wrapper in ISE v11.4 and older, a no cost full license must be obtained from Xilinx. See the product page:

www.xilinx.com/products/ipcenter/Embedded_TEMAC_Wrapper.htm

Contact your local Xilinx sales representative for pricing and availability of other Xilinx LogiCORE IP modules and software. Information on additional LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

Date	Version	Revision
10/19/04	1.0	Initial Xilinx release.
2/25/05	2.0	Added support for SGMII and 1000BASE-X PCS/PMA physical interfaces.
7/26/05	3.1	Updated Features section to match version 3.1 of the wrapper.
1/18/06	4.1	Restructured document for new wrapper architecture.
7/13/06	4.2	Updated core to version 4.2; Xilinx tools 8.2i.
9/21/06	4.3	Updated core to version 4.3.
2/15/07	4.4	Updated core to version 4.4; ISE tools to 9.1i.
8/8/07	4.5	Updated core to version 4.5; ISE tools 9.2i.
3/24/08	4.6	Updated core to version 4.6; ISE tools 10.1.
4/24/09	4.7	Updated core to version 4.7, and ISE tools to version 11.1.
4/19/10	4.8	Updated core to version 4.8, and ISE tools to version 12.1.

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