LogiCORE IP 3GPP Mixed Mode Turbo Decoder v1.0

PB009 January 18, 2012 **Product Brief**

Introduction

The 3GPP Mixed Mode Turbo Decoder LogiCORE™ provides a flexible turbo convolutional decode function for both LTE and WCDMA air interfaces. The implementation is compliant with the requirements set out in both [Ref 1] and [Ref 2]. The core provides an optimized turbo decode function for base stations at all form factors, from femto to macrocells. The decoder, when used with a TCC encoder, provides an effective way of transmitting data reliably over noisy data channels.

Features

- Three versions of this core can be generated, each supporting different standard options:
  - LTE only
  - UMTS only
  - both LTE and UMTS
- When UMTS and LTE are both supported the core can switch between different standards on a block by block basis.
- Each core is completely self contained, requiring nothing else to decode data.
- All 3GPP LTE block sizes supported: 188 different block sizes in the range 40–6144
- All 3GPP UMTS block sizes supported, that is block sizes in the range 40-5114.
- Configurable with either 1, 2 ,4 or 8 decode units, allowing resource utilization to be optimized while meeting system performance requirements at all base station form factors.
- Dynamically selectable number of iterations 1-15.
- Support for MAX, MAX_SCALE and MAX_STAR algorithms.
- AXI4-Stream interfaces used for control and data input/output.
- C model and Matlab MEX function available for bit accurate modelling of error correcting performance.
- Number representation: Two's complement fractional.
- Data Input: 7 or 8 bits (4 or 5 integer bits with 3 fractional bits)
- Hardware DSP units can be used instead of logic resources to tailor the core resource usage to specific user applications.
- Demonstration test bench to show an example of core usage.
- Integrated scheduler ensures that decode latency remains virtually constant with variable block sizes.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000, Virtex®-7, Kintex™-7, Artix™-7, Virtex-6, Virtex-5
Supported User Interfaces	AXI4-Stream
Provided with Core	
Design Files	Netlist
Example Design	VHDL
Test Bench	VHDL
Constraints File	Not Provided
Simulation Model	Verilog or VHDL Structural Behavioral, C Model and MATLAB® Model
Supported S/W Driver	N/A
Tested Design Tools	
Design Entry Tools	CORE Generator™ tool 13.4
Simulation(2)	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator Synopsys VCS and VCS MX ISim
Synthesis Tools(2)	XST
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For a complete listing of supported devices, see the release notes for this core.
2. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Overview

The TCC decoder is used in conjunction with a TCC encoder to provide an effective way of transmitting data reliably over noisy data channels. The turbo decoder operates very well under low signal-to-noise conditions and provides a performance close to the theoretical optimal performance defined by the Shannon limit [Ref 3].

References

1. 3GPP TS 25.212 "Multiplexing and channel coding (FDD)", v10.1.0
2. 3GPP TS 36.212 "Multiplexing and channel coding", v10.3.0
3. C. Berrou, A. Glavieux, and P. Thitimajshima, Near Shannon Limit Error-correcting Coding and Decoding Turbo Codes, IEEE Proc 1993 Int Conf. Comm., pp1064-1070

Additional Documentation and Supporting Materials

A full product guide and additional supporting materials (C models) are available for this core. Access to this material may be requested by clicking on this registration link:
http://www.xilinx.com/member/mm_tcc_dec_eval/index.htm

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the IP Release Notes Guide (XTP025) for more information on this core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Resolved Issues
- Known Issues

Ordering Information

The 3GPP Mixed Mode Turbo Decoder core is provided under the Xilinx Turbo Code LogiCORE IP License Terms and can be generated using the Xilinx® CORE Generator™ system. The CORE Generator system is shipped with Xilinx ISE® Design Suite software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the 3GPP Mixed Mode Turbo Decoder product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Licensing

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VAT/TURBOCODES,
38, rue du Général Leclerc,
92794 Issy Moulineaux,
Cedex 9,
France.

Evaluation License

An evaluation license is available for this core. The evaluation version of the core operates in the same way as the full version for several hours, depending on clock frequency. Operation is then disabled and the data output does not change. If you notice this behavior in hardware, it means that you are using an evaluation version of the core. The Xilinx tools warn that an evaluation license is being used during netlist implementation. If a full license is installed in order for the core to run on hardware, delete the old XCO file and re-create the core from new.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
01/18/12	1.0	Xilinx initial release.

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