LogiCORE IP 3GPP LTE Turbo Decoder v2.0

XMP020 August 15, 2011 **Product Brief**

Introduction

The Turbo Convolution Code (TCC) decoder core is used in conjunction with a TCC encoder to provide an extremely effective way of transmitting data reliably over noisy data channels. The TCC decoder is designed to meet the *3GPP Mobile Communication System* specification.

Features

- Implements the 3GPP Long Term Evaluation (LTE) specification [Ref 1]
- Core contains the full interleaver
- Full 3GPP LTE block size range supported, that is, 188 different block sizes in the range 40 - 6144
- Dynamically selectable number of Iterations 1-15
- Number representation: two's complement fractional numbers
- Data input: 7 or 8 bits (4 or 5 integer bits with 3 fractional bits.
- Internal calculations 11 or 12 bits (8 or 9 integer bits with 3 fractional bits).
- Support for multiple processing units (1, 2, 4, 8) to provide increased throughput
- Support for the MAX, MAX_SCALE and MAX* algorithms.
- Optional extrinsic data input and output ports.
- Input and output selectable between word serial or word parallel.
- Selection between DSP or fabric resources
- Support for rate 1/3 coded input
- C model available for fast simulation of BER performance.
- Variation in soft input data width with automatic selection of internal calculation precision
- New data interfaces with enhanced data throttling
- Support for extrinsic data input and output
- Parallel data input and output capability
- Support for 1 PU (Processing Unit)
- Higher average throughput with more efficient scheduling
- Up to 20% resource saving (depending on the number of DU)
- Available through the Xilinx® CORE Generator™ 13.2 software

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex®-7, Kintex™-7, Artix™-7, Zynq™-7000, Virtex-6, Virtex-5, Spartan®-6 Virtex-5, Virtex-4, Spartan-3A DSP, Spartan-3
Supported User Interfaces(2)	N/A
Provided with Core	
Documentation	Product Brief Product Specification C Model User Guide (Contact Xilinx sales representative)
Design Files	Netlist
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	N/A
Simulation Model	Verilog VHDL C Model
Tested Design Tools	
Design Entry Tools	CORE Generator tool 13.2
Simulation(3)	Mentor Graphics ModelSim
Synthesis Tools	N/A
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.
2. Interface similar to AXI and can be connected to an AXI4- Stream Interface.
3. For the supported version of the tools, see the ISE Design Suite 13: Release Notes Guide

General Description

The TCC decoder is used in conjunction with a TCC encoder to provide an extremely effective way of transmitting data reliably over noisy data channels. The turbo decoder operates very well under low signal-to-noise conditions and provides a performance close to the theoretical optimal performance defined by the Shannon limit.

When a decoding operation is started, the core accepts the block size and the number of iterations from two input ports. A data load stage follows, in which the systematic and parity data is read into the core in parallel on a clock-by-clock basis and stored in internal block RAM. The core then starts the decoding process and implements the required number of iterations. Finally, the decoded bit sequence is output. All interleaving operations required in the 3GPP LTE specification are handled automatically within the core.

The core expects two's complement fractional numbers as inputs and also uses this format for the internal calculations. Each fractional input number represents the Log Likelihood Ratio (LLR) divided by 2 for each input bit. This LLR value can be considered to be the confidence level that a particular bit is a one or zero.

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_turbo_dec_eval/index.htm.

References

1. 3G TS.36.212 V1.0.0 (2007-03), *Multiplexing and Channel Coding (Release 8)*, Technical Specification Group Radio Access Network, 3rd Generation Partnership Project.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

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The Turbo Decoder core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator v13.2. The CORE Generator software is shipped with Xilinx ISE® Design Suite software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the Turbo Decoder product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional modules is available from the Xilinx IP Center.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/25/08	1.0	Initial Xilinx release.
06/24/09	1.5	Enhanced core, added support for Virtex-6 and Spartan-6.
06/22/11	1.6	Add new family support. Update to ISE 13.2.
08/15/11	1.7	Updated to include web registration information.

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