IEEE 802.16e CTC Decoder v4.0

XMP004 December 2, 2009 **Product Brief**

Introduction

The IEEE 802.16e CTC decoder core performs iterative decoding of channel data that has been encoded as described in Section 8.4.9.2.3 of the IEEE Std 802.16e-2005 specification and corrigendum IEEE P802.16Rev2/D0b (June 2007). The IEEE 802.16e code is a parallel concatenated convolutional code with an input data block of 2N bits. Through parallel processing with parameterizable number of SISOs, this LogiCORE™ IP decoder core is capable of achieving high throughput. The decoded data rate reaches up to 220 Mbps with five iterations using eight SISOs at 286 MHz clock frequency.

Features

- Supports Virtex®-6, Virtex-5, Virtex-4, Spartan®-6, Spartan-3, Spartan-3E, and Spartan-3A DSP FPGA families
- Supports all interleaver block sizes of the CTC OFDMA PHY mode including the HARQ and IR HARQ modes: 24, 36, 48, 72, 96, 108, 120, 144, 180, 192, 216, 240, 480, 960, 1440, 1920, and 2400 pairs
- Performs parallel processing with parameterizable number of SISOs to achieve high throughput and reduce latency
- Supports dynamic block size switching without interruption
- Programmable number of iterations dynamically changeable per block
- Adaptive rate change via puncturing interface
- Uses MAX-LOG-MAP algorithm with extrinsic scaling
- Parameterizable options for soft data input and extrinsic bits
- Clock speed exceeds 162 MHz in Virtex-4 speed grade -10, 196 MHz in Virtex-5 speed grade -1, and 225 MHz in Virtex-6 speed grade -1
- Decoded data rate depends on block size and varies between 44 Mbps to 63 Mbps when targeting Virtex-4, between 53 Mbps to 76 Mbps when targeting Virtex-5, and between 61 Mbps to 88 Mbps when targeting Virtex-6 (slowest speed grade, five iterations, and four SISO option)
- Latency depends on block size and varies between 5 µs to 76 µs when targeting Virtex-4, between 4 µs to 63 µs when targeting Virtex-5, and between 4 µs to 55 µs when targeting Virtex-6 (slowest speed grade, five iterations, and four SISO option)
- Fully synchronous design with single clock domain
- Double-buffered input to accommodate burst or continuous data
- Available using the CORE Generator™ v11.2 software, which is included with the ISE® 11.2 software

LogiCORE™ Facts	
Core Specifics	
Supported Device Family	Virtex®-4, Virtex-5, Virtex-6, Spartan®-3, Spartan-3E, Spartan-3A DSP, Spartan-6
Resources Used	See Resource Utilization: Table 9 through Table 12 in the Data Sheet
Provided with Core	
Documentation	Data Sheet (DS634)
Design File Formats	NGC netlist and VHDL or Verilog Simulation Model
Constraints File	UCF
Verification	VHDL Test Bench
Instantiation Template	VHDL Wrapper
Design Tool Requirements	
Xilinx Implementation Tools	ISE 11.2
Verification	ModelSim PE 6.2c
Simulation	ModelSim PE 6.2c
Synthesis	XST
Support	
Provided by Xilinx, Inc.	

Ordering Information

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The IEEE 802.16e CTC Decoder core is provided under the SignOnce IP Site License and can be generated using the Xilinx ISE CORE Generator v11.2 or higher. The CORE Generator software is shipped with Xilinx ISE Foundation™ Series Development software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the IEEE 802.16e CTC Decoder Product Page.

Contact your local Xilinx sales representative for more information, including the full decoder data sheet, licensing, pricing and availability on Xilinx LogiCORE™ IP products and software.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/10/07	1.0	Initial Xilinx release.
06/24/09	2.0	Updated for core v4.0.
12/02/09	2.1	ISE version numbers revised.

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