LogiCORE IP System Management Wizard v1.0

Product Guide

Vivado Design Suite

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Appendix B: Additional Resources and Legal Notices

Introduction

The LogiCORE IP System Management Wizard provides a complete solution for system-monitoring Xilinx UltraScale™ architecture-based devices. This IP generates an HDL wrapper to configure the SYSMONE1 primitive for user-specified external channels, internal sensor channels, modes of operation and alarms. This IP supports monitoring of up to four user supplies. In addition, the System Management Wizard configures various interfaces for accessing SYSMONE1 registers.

Features

- On-chip voltage and temperature measurements
- 10-bit 0.2 MSPS analog-to-digital conversion
- Access to 16 pairs of IO pins as input channels
- Stand-alone measurement of system functionality including sequences and alarms
- Triple access (FPGA Fabric/JTAG/I2C) DRP including control and status registers
- Optional AXI4-Lite interface based on the AXI4 specification
- Easy configuration of various modes and parameters
- Simple interface for channel selection and configuration
- Ability to select/deselect alarm outputs and set alarm limits
- Calculates all parameters and register values based on requirements

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™ Architecture
Supported User Interfaces	AXI4-Lite, DRP
Resources	See Table 2-1.
Provided with Core	
Design Files	Verilog and VHDL
Example Design	Verilog and VHDL
Test Bench	Verilog and VHDL
Constraints File	XDC
Simulation Model	Not Provided
Supported S/W Driver	Standalone
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog .
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The System Management Wizard guides you to configure the SYSMONE1 primitive through a user-friendly GUI and generates Verilog or VHDL Register Transfer Level (RTL) source files for Xilinx UltraScale™ FPGAs. An example design and simulation test bench demonstrate how to integrate the core into user designs.

The top-level block diagram for the System Management Wizard is shown in Figure 1-1.

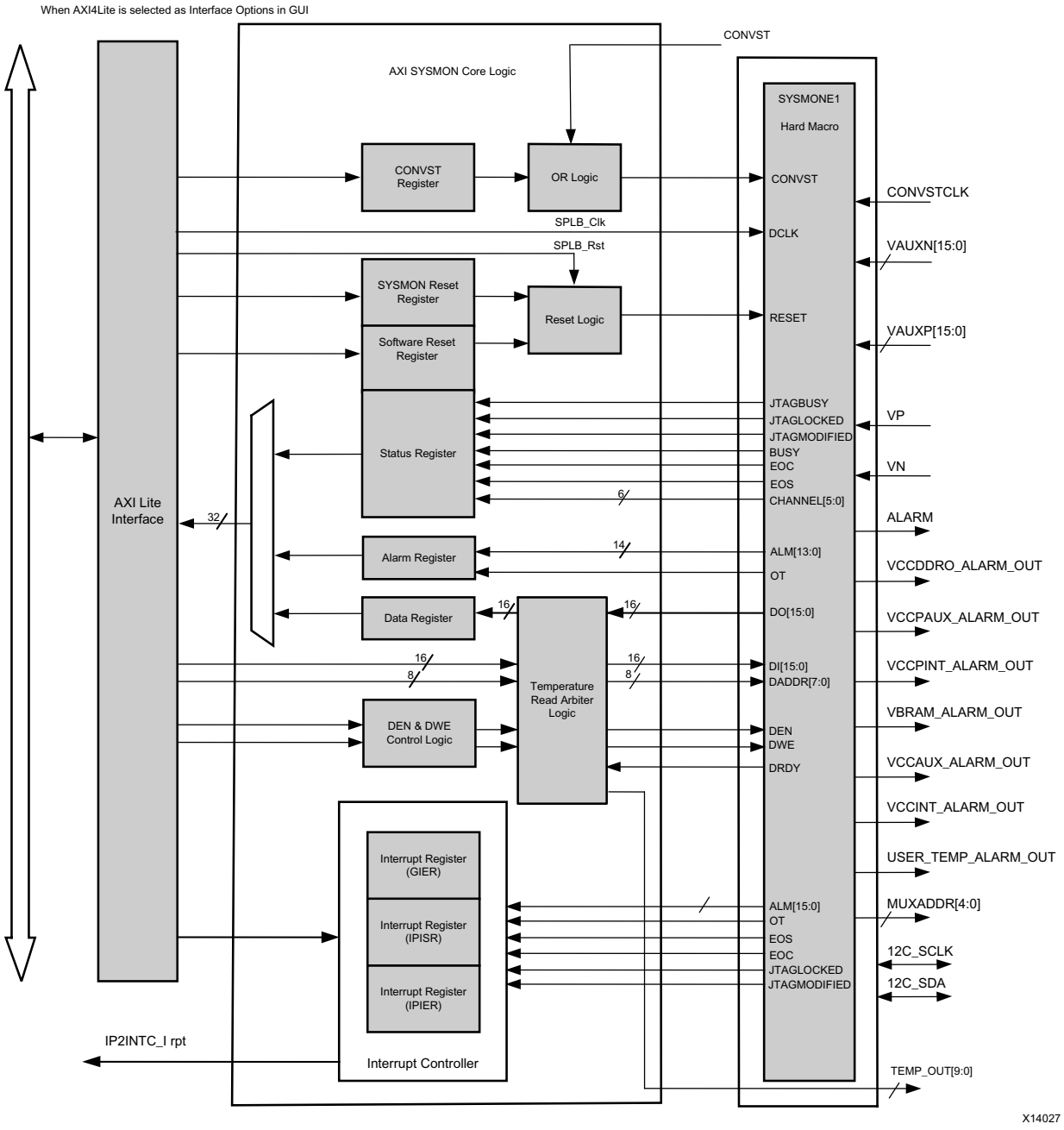

Figure 1-1: **System Management Wizard Block Diagram**

Applications

The System Management Wizard enables you to easily configure the integrated system management functions of the FPGA, such as monitoring user supplies and temperature.

Licensing and Ordering Information

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado design tools: Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

License Type

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

The System Management Wizard instantiates a SYSMONE1 block configured to your requirements. The wizard allows you to select the channels, enable alarms, and set the alarm limits. For interfaces, you can select AXI4-Lite, DRP, or None.

SYSMONE1 Functional Features

Major functional SYSMONE1 features can be used to determine an appropriate mode of operation. These features include:

- FPGA temperature and voltage monitoring
- Analog-to-digital conversion for seventeen external analog inputs
- Alarm generation based on up to 17 set parameters

Standards

The System Management Wizard core contains AXI4-Lite interfaces, which is based on the AMBA® AXI4 specification.

Performance

If you enable averaging of the channel, data capture rate is reduced depending on the averaging selected. Choose the appropriate value to match your requirement. Analog input noise from the supply or board can alter the expected 10-bit digital output.

Maximum Frequencies

The maximum `s_axi_aclk/dclk` clock frequency supported is 250 MHz.

Resource Utilization

Table 2-1 provides approximate resource counts when AXI4-Lite is selected as the interface. These are measured with Xilinx UltraScale™ architecture-based devices with interrupt logic enabled and TEMP_BUS enabled or disabled.

Table 2-1: **Device Utilization**

Parameter Values		Device Resources		Performance
C_HAS_TEMP_BUS	Enable_AXI	Slice Flip-Flops	LUTs	FMAX (MHz)
0	1	249	185	200
1	1	451	389	200

When only the DRP interface is selected, the System Management Wizard uses SYSMONE1 primitive only. Therefore, no LUTs are used as resource.

The maximum clock frequency results are post-implementation using the default tool settings. The resource usage results do not include the characterization registers and represent the true logic used by the core. LUT counts include SRL16s or SRL32s.

Clock frequency does not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification. The maximum achievable clock frequency and the resource counts might also be affected by other tool options, additional logic in the FPGA, different versions of Xilinx tools, and other factors.

Port Descriptions

Table 2-2 lists the input and output ports provided from the System Management Wizard. Availability of ports is controlled by user-selected parameters. For example, when Dynamic Reconfiguration is selected, only ports associated with Dynamic Reconfiguration are exposed. Any port that is not exposed is tied off or connected to a signal labeled as unused in the delivered source code.

Table 2-2: **SYSMONE1 I/O Signals**

Port	Direction	Description
di_in[15:0](2)	Input	Input data bus for the dynamic reconfiguration port (DRP).
do_out[15:0]	Output	Output data bus for the dynamic reconfiguration port.
daddr_in[7:0]	Input	Address bus for the dynamic reconfiguration port.
den_in	Input	Enable signal for the dynamic reconfiguration port.
dwe_in	Input	Write enable for the dynamic reconfiguration port.
dclk_in	Input	Clock input for the dynamic reconfiguration port.

Table 2-2: **SYSMONE1 I/O Signals *(Cont'd)***

Port	Direction	Description
drdy_out	Output	Data ready signal for the dynamic reconfiguration port.
reset_in(2)	Input	Reset signal for the SYSMONE1 control logic and maximum/ minimum registers.
convst_in	Input	Convert start input. This input is used to control the sampling instant on the ADC input and is only used in Event Mode Timing (see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1]).
convstclk_in	Input	Convert start input. This input is connected to a global clock input on the interconnect. Like CONVST, this input is used to control the sampling instant on the ADC inputs and is only used in Event Mode Timing. The frequency of this clock should be greater than or equal to the sampling rate.
vp_in vn_in	Input	One dedicated analog-input pair. The SYSMONE1 has one pair of dedicated analog-input pins that provide a differential analog input.
vauxp15[15:0] vauxn15[15:0]	Inputs	16 auxiliary analog-input pairs. Also, the SYSMONE1 uses 16 differential digital-input pairs as low-bandwidth differential analog inputs. These inputs are configured as analog during FPGA configuration.
user_temp_alarm_out	Output	SYSMONE1 temperature-sensor alarm output.
vccint_alarm_out	Output	SYSMONE1 VCCINT-sensor alarm output.
vccaux_alarm_out	Output	SYSMONE1 VCCAUX-sensor alarm output.
ot_out	Output	Over-Temperature alarm output.
channel_out[5:0]	Outputs	Channel selection outputs. The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.
eoc_out	Output	End of Conversion signal. This signal transitions to an active-High at the end of an ADC conversion when the measurement result is written to the status registers. For detailed information, see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
eos_out	Output	End of Sequence. This signal transitions to an active-High when the measurement data from the last channel in the Channel Sequencer is written to the status registers. For detailed information, see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
busy_out	Output	ADC busy signal. This signal transitions High during an ADC conversion. This signal transitions High for an extended period during calibration.
i2c_sclk	INOUT	I^2C clock signal.
i2c_sda	INOUT	I^2C serial data signal.
jtaglocked_out(2)	Output	Used to indicate that drp port has been locked by the JTAG interface.
jtagmodified_out(2)	Output	Used to indicate that a JTAG write to the drp has occurred.

Table 2-2: **SYSMONE1 I/O Signals *(Cont'd)***

Port	Direction	Description
jtagbusy_out[2]	Output	Used to indicate that a JTAG drp transaction is in progress.
vbram_alarm_out	Output	SYSMONE1 VBRAM sensor alarm output.
muxaddr_out[4:0]	Output	Use in external multiplexer mode to decode external MUX channel.
alarm_out	Output	Logic OR of alarms. Can be used to flag occurrence of any alarm.
s_axi_aclk	Input	AXI Clock.
s_axi_aresetn[2]	Input	AXI Reset, Active-Low
s_axi_awaddr[10:0]	Input	AXI Write address. The write address bus gives the address of the write transaction.
s_axi_awvalid	Input	Write address valid. This signal indicates that a valid write address and control information are available.
s_axi_awready	Output	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
s_axi_wdata[31:0]	Input	Write data.
s_axi_wstb[3:0]	Input	Write strobes. This signal indicates which byte lanes to update in memory.
s_axi_wvalid	Input	Write valid. This signal indicates that valid write data and strobes are available.
s_axi_wready	Output	Write ready. This signal indicates that the slave can accept the write data.
s_axi_bresp[1:0]	Output	Write response. This signal indicates the status of the write transaction: • 00 = OKAY (normal response) • 10 = SLVERR (error condition) • 11 = DECERR (not issued by core)
s_axi_bvalid	Output	Write response valid. This signal indicates that a valid write response is available.
s_axi_bready	Input	Response ready. This signal indicates that the master can accept the response information.
s_axi_araddr[10:0]	Input	Read address. The read address bus gives the address of a read transaction.
s_axi_arvalid	Input	Read address valid. This signal indicates, when High, that the read address and control information is valid and remains stable until the address acknowledgement signal, s_axi_arready, is High.
s_axi_arready	Output	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
s_axi_rdata[31:0]	Output	Read data.

Table 2-2: **SYSMONE1 I/O Signals *(Cont'd)***

Port	Direction	Description
s_axi_rresp[1:0]	Output	Read response. This signal indicates the status of the read transfer. • 00 = OKAY (normal response) • 10 = SLVERR (error condition) • 11 = DECERR (not issued by core)
s_axi_rvalid	Output	Read valid. This signal indicates that the required read data is available and the read transfer can complete.
s_axi_rready	Input	Read ready. This signal indicates that the master can accept the read data and response information.
temp_out[9:0](3)	Output	10-bit temperature output bus for MIG. This should be connected to temperature input port of MIG.

Notes:

1. AXI4-Lite ports are available only with the AXI4-Lite interface.
2. DRP, JTAG, and reset_in ports are not available when AXI4-Lite interface is selected.
3. The temp_out port is available only when AXI4-Lite interface is enabled.

Register Space

The SYSMONE1 functionality is configured through control registers. For more details, see control and status register information in *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].

Table 2-3 lists the attributes associated with these control registers. Control registers can be initialized using HDL by attaching HDL attributes to the SYSMONE1 primitive instance and configuring them according to the information provided in Table 2-3. The control registers can also be initialized through the AXI4-Lite or DRP interfaces at runtime. The System Management Wizard simplifies the initialization of these control registers in the HDL instantiation by automatically configuring them to implement the operating behavior you specify in the Vivado® Integrated Design Environment (IDE).

Table 2-3: **SYSMONE1 Attributes**

Attribute	Name	Control Reg Address	Description
INIT_40	Configuration Register 0	40h	SYSMONE1 configuration registers. For detailed information, see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
INIT_41	Configuration Register 1	41h	
INIT_42	Configuration Register 2	42h	
INIT_43	Configuration Register 3	43h	

Table 2-3: **SYSMONE1 Attributes *(Cont'd)***

Attribute	Name	Control Reg Address	Description
INIT_48 to INIT_4F	Sequence Registers	48h to 4Fh	Sequence registers used to program the Channel Sequencer function in the SYSMONE1. For detailed information, see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
INIT_50 to INIT_6F	Alarm Limits Registers	50h to 6Fh	Alarm threshold registers for the SYSMONE1 alarm function. For detailed information, see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
SIM_MONITOR_ FILE	Simulation Analog Entry File	–	This is the text file that contains the analog input stimulus. This is used for simulation.

System Management Wizard Register Descriptions for AXI4-Lite Interface

Table 2-4 lists the System Management Wizard IP Core registers and corresponding addresses.

Table 2-4: **IP Core Registers**

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
System Management Wizard Local Register Grouping				
C_BASEADDR + 0x00	Software Reset Register (SRR)	N/A	W(1)	Software Reset Register
C_BASEADDR + 0x04	Status Register (SR)	N/A	R(2)	Status Register
C_BASEADDR + 0x08	Alarm Output Status Register (AOSR)	0x0	R(2)	Alarm Output Status Register
C_BASEADDR + 0x0C	CONVST Register (CONVSTR)	N/A	W(1)	• Bit[0] = ADC convert start register(3) • Bit[1] = Enable temperature update logic • Bit[17:2] = Wait cycle for temperature update
C_BASEADDR + 0x10	SYSMONE1 Reset Register (SYSMONRR)	N/A	W(1)	SYSMONE1 Hard Macro Reset Register

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
System Management Wizard Interrupt Controller Register Grouping				
C_BASEADDR + 0x5C	Global Interrupt Enable Register (GIER)	0x0	R/W	Global Interrupt Enable Register
C_BASEADDR + 0x60	IP Interrupt Status Register (IPISR)	N/A	R/TOW(4)	IP Interrupt Status Register
C_BASEADDR + 0x68	IP Interrupt Enable Register (IPIER)	0x0	R/W	IP Interrupt Enable Register
System Management Wizard Hard Macro Register Grouping(5)				
C_BASEADDR + 0x400	Temperature	N/A	R(6)	10-bit Most Significant Bit (MSB) justified result of on-device temperature measurement is stored in this register.
C_BASEADDR + 0x404	V_{CCINT}	N/A	R(6)	The 10-bit MSB justified result of on-device V_{CCINT} supply monitor measurement is stored in this register.
C_BASEADDR + 0x408	V_{CCAUX}	N/A	R(6)	The 10-bit MSB justified result of on-device V_{CCAUX} Data supply monitor measurement is stored in this register.
C_BASEADDR + 0x40C	V_P/V_N	0x0	R/W(7)	• When read: The 10-bit MSB justified result of A/D conversion on the dedicated analog input channel (Vp/Vn) is stored in this register. • When written: Write to this register resets the SYSMONE1 hard macro. No specific data is required.
C_BASEADDR + 0x410	V_{REFP}	0x0	R(6)	The 10-bit MSB justified result of A/D conversion on the reference input V_{REFP} is stored in this register.
C_BASEADDR + 0x414	V_{REFN}	0x0	R(6)	The 10-bit MSB justified result of A/D conversion on the reference input V_{REFN} is stored in this register.
C_BASEADDR + 0x418	V_{BRAM}	0x0	R(6)	The 10-bit MSB justified result of A/D conversion on the reference input V_{BRAM} is stored in this register.
C_BASEADDR + 0x41C	Undefined	Undefined	N/A	These locations are unused and contain invalid data.

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
C_BASEADDR + 0x420	Supply Offset	N/A	R[6]	The calibration coefficient for the supply sensor offset is stored in this register.
C_BASEADDR + 0x424	ADC Offset	N/A	R[6]	The calibration coefficient for the ADC offset calibration is stored in this register.
C_BASEADDR + 0x428	Gain Error	N/A	R[6]	The calibration coefficient for the gain error is stored in this register.
C_BASEADDR + 0x42C to C_BASEADDR + 0x43C	Undefined	Undefined	N/A	These locations are unused and contain invalid data.
C_BASEADDR + 0x440	VAUXP[0]/ VAUXN[0]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 0 is stored in this register.
C_BASEADDR + 0x444	VAUXP[1]/ VAUXN[1]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 1 is stored in this register.
C_BASEADDR + 0x448	VAUXP[2]/ VAUXN[2]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 2 is stored in this register.
C_BASEADDR + 0x44C	VAUXP[3]/ VAUXN[3]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 3 is stored in this register.
C_BASEADDR + 0x450	VAUXP[4]/ VAUXN[4]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 4 is stored in this register.
C_BASEADDR + 0x454	VAUXP[5]/ VAUXN[5]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 5 is stored in this register.
C_BASEADDR + 0x458	VAUXP[6]/ VAUXN[6]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 6 is stored in this register.
C_BASEADDR + 0x45C	VAUXP[7]/ VAUXN[7]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 7 is stored in this register.
C_BASEADDR + 0x460	VAUXP[8]/ VAUXN[8]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 8 is stored in this register.
C_BASEADDR + 0x464	VAUXP[9]/ VAUXN[9]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 9 is stored in this register.

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
C_BASEADDR + 0x468	VAUXP[10]/ VAUXN[10]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 10 is stored in this register.
C_BASEADDR + 0x46C	VAUXP[11]/ VAUXN[11]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 11 is stored in this register.
C_BASEADDR + 0x470	VAUXP[12]/ VAUXN[12]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 12 is stored in this register.
C_BASEADDR + 0x474	VAUXP[13]/ VAUXN[13]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 13 is stored in this register.
C_BASEADDR + 0x478	VAUXP[14]/ VAUXN[14]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 14 is stored in this register.
C_BASEADDR + 0x47C	VAUXP[15]/ VAUXN[15]	0x0	R[6]	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 15 is stored in this register.
C_BASEADDR + 0x480	Max Temp	N/A	R[6]	The 10-bit MSB justified maximum temperature measurement.
C_BASEADDR + 0x484	Max VCCINT	N/A	R[6]	The 10-bit MSB justified maximum VCCINT measurement.
C_BASEADDR + 0x488	Max VCCAUX	N/A	R[6]	The 10-bit MSB justified maximum VCCAUX measurement.
C_BASEADDR + 0x48C	Max VBRAM	N/A	R[6]	The 10-bit MSB justified maximum VBRAM measurement.
C_BASEADDR + 0x490	Min Temp	N/A	R[6]	The 10-bit MSB justified minimum temperature measurement
C_BASEADDR + 0x494	Min VCCINT	N/A	R[6]	The 10-bit MSB justified minimum VCCINT measurement
C_BASEADDR + 0x498	Min VCCAUX	N/A	R[6]	The 10-bit MSB justified minimum VCCAUX measurement.
C_BASEADDR + 0x49C	Min VBRAM	N/A	R[6]	The 10-bit MSB justified minimum VBRAM measurement.
C_BASEADDR + 0x4A0 - C_BASEADDR + 0x4F8	Undefined	Undefined	N/A	These locations are unused and contain invalid data.
C_BASEADDR + 0x4E0	I2C Address	N/A	R	The I^2C address captured by initial conversion on V_p/V_n channel.

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
C_BASEADDR + 0x4FC	Flag Register	N/A	R[6]	The 16-bit register gives general status information of ALARM, Over Temperature (OT), disable information of SYSMONE1 and information about whether the SYSMONE1 is using internal reference voltage or external reference voltage.
C_BASEADDR + 0x500	Configuration Register 0	0x0	R/W	SYSMONE1 Configuration Register 0.
C_BASEADDR + 0x504	Configuration Register 1	0x0	R/W	SYSMONE1 Configuration Register 1.
C_BASEADDR + 0x508	Configuration Register 2	0x1E00	R/W	SYSMONE1 Configuration Register 2.
C_BASEADDR + 0x50C	Configuration Register 3	0x000F	R/W	SYSMONE1 Configuration Register 3.
C_BASEADDR + 0x510	Test Register	N/A	N/A	SYSMONE1 Test Register (For factory test only).
C_BASEADDR + 0x514	Analog Bus Register	N/A	N/A	Configuration register for the Analog Bus.
C_BASEADDR + 0x518	Sequence Register 8	0x0	R/W	Sequencer channel selection (Vuser0-3).
C_BASEADDR + 0x51C	Sequence Register 9	0x0	R/W	Sequencer average selection (Vuser0-3).
C_BASEADDR + 0x520	Sequence Register 0	0x0	R/W	SYSMONE1 Sequence Register 0 (ADC channel selection).
C_BASEADDR + 0x524	Sequence Register 1	0x0	R/W	SYSMONE1 Sequence Register 1 (ADC channel selection).
C_BASEADDR + 0x528	Sequence Register 2	0x0	R/W	SYSMONE1 Sequence Register 2 (ADC channel averaging enable).
C_BASEADDR + 0x52C	Sequence Register 3	0x0	R/W	SYSMONE1 Sequence Register 3 (ADC channel averaging enable).
C_BASEADDR + 0x530	Sequence Register 4	0x0	R/W	SYSMONE1 Sequence Register 4 (ADC channel analog-input mode).
C_BASEADDR + 0x534	Sequence Register 5	0x0	R/W	SYSMONE1 Sequence Register 5 (ADC channel analog-input mode).
C_BASEADDR + 0x538	Sequence Register 6	0x0	R/W	SYSMONE1 Sequence Register 6 (ADC channel acquisition time).
C_BASEADDR + 0x53C	Sequence Register 7	0x0	R/W	SYSMONE1 Sequence Register 7 (ADC channel acquisition time).

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
C_BASEADDR + 0x540	Alarm Threshold Register 0	0x0	R/W	The 10-bit MSB justified alarm threshold register 0 (Temperature Upper).
C_BASEADDR + 0x544	Alarm Threshold Register 1	0x0	R/W	The 10-bit MSB justified alarm threshold register 1 (V_{CCINT} Upper).
C_BASEADDR + 0x548	Alarm Threshold Register 2	0x0	R/W	The 10-bit MSB justified alarm threshold register 2 (V_{CCAUX} Upper).
C_BASEADDR + 0x54C	Alarm Threshold Register 3	0x0	R/W(8)	The 10-bit MSB justified alarm threshold register 3 (OT Upper).
C_BASEADDR + 0x550	Alarm Threshold Register 4	0x0	R/W	The 10-bit MSB justified alarm threshold register 4 (Temperature Lower).
C_BASEADDR + 0x554	Alarm Threshold Register 5	0x0	R/W	The 10-bit MSB justified alarm threshold register 5 (V_{CCINT} Lower).
C_BASEADDR + 0x558	Alarm Threshold Register 6	0x0	R/W	The 10-bit MSB justified alarm threshold register 6 (V_{CCAUX} Lower).
C_BASEADDR + 0x55C	Alarm Threshold Register 7	0x0	R/W	The 10-bit MSB justified alarm threshold register 7 (OT Lower)
C_BASEADDR + 0x560	Alarm Threshold Register 8	0x0	R/W	The 10-bit MSB justified alarm threshold register 8 (V_{BRAM} Upper)
C_BASEADDR + 0x570	Alarm Threshold Register 12	0x0	R/W	The 10-bit MSB justified alarm threshold register 12 (V_{BRAM} Lower)
C_BASEADDR + 0x580	Alarm Threshold Register 16	0x0	R/W	The 10-bit MSB justified alarm threshold register 16 (V_{USER0} Upper)
C_BASEADDR + 0x584	Alarm Threshold Register 17	0x0	R/W	The 10-bit MSB justified alarm threshold register 17 (V_{USER1} Upper)
C_BASEADDR + 0x588	Alarm Threshold Register 18	0x0	R/W	The 10-bit MSB justified alarm threshold register 18 (V_{USER2} Upper)

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
C_BASEADDR + 0x58C	Alarm Threshold Register 19	0x0	R/W	The 10-bit MSB justified alarm threshold register 19 (V_{USER3} Upper)
C_BASEADDR + 0x5A0	Alarm Threshold Register 22	0x0	R/W	The 10-bit MSB justified alarm threshold register 14 (V_{USER0} Lower).
C_BASEADDR + 0x5A4	Alarm Threshold Register 23	0x0	R/W	The 10-bit MSB justified alarm threshold register 15 (V_{USER1} Lower).
C_BASEADDR + 0x5A8	Alarm Threshold Register 24	0x0	R/W	The 10-bit MSB justified alarm threshold register 16 (V_{USER2} Lower).
C_BASEADDR + 0x5AC	Alarm Threshold Register 25	0x0	R/W	The 10-bit MSB justified alarm threshold register 17 (V_{USER3} Lower).
C_BASEADDR + 0x600	V_{USER0}	N/A	R	The 10-bit MSB justified result of the on-chip V_{USER0} supply monitor measurement is stored at this location.
C_BASEADDR + 0x604	V_{USER1}	N/A	R	The 10-bit MSB justified result of the on-chip V_{USER1} supply monitor measurement is stored at this location.
C_BASEADDR + 0x608	V_{USER2}	N/A	R	The 10-bit MSB justified result of the on-chip V_{USER2} supply monitor measurement is stored at this location.
C_BASEADDR + 0x60C	V_{USER3}	N/A	R	The 10-bit MSB justified result of the on-chip V_{USER3} supply monitor measurement is stored at this location.
C_BASEADDR + 0x680	Max V_{USER0}	N/A	R	Maximum V_{USER0} measurement recorded since power-up or the last System Monitor reset.
C_BASEADDR + 0x684	Max V_{USER1}	N/A	R	Maximum V_{USER1} measurement recorded since power-up or the last System Monitor reset.
C_BASEADDR + 0x688	Max V_{USER2}	N/A	R	Maximum V_{USER2} measurement recorded since power-up or the last System Monitor reset.
C_BASEADDR + 0x68C	Max V_{USER3}	N/A	R	Maximum V_{USER3} measurement recorded since power-up or the last System Monitor reset.
C_BASEADDR + 0x6A0	Min V_{USER0}	N/A	R	Minimum V_{USER0} measurement recorded since power-up or the last System Monitor reset.

Table 2-4: **IP Core Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Reset Value (hex)	Access Type	Description
C_BASEADDR + 0x6A4	Min V_{USER1}	N/A	R	Minimum V_{USER1} measurement recorded since power-up or the last System Monitor reset.
C_BASEADDR + 0x6A8	Min V_{USER2}	N/A	R	Minimum V_{USER2} measurement recorded since power-up or the last System Monitor reset.
C_BASEADDR + 0x6Ac	Min V_{USER3}	N/A	R	Minimum V_{USER3} measurement recorded since power-up or the last System Monitor reset.

1. Reading of this register returns an undefined value.
2. Writing into this register has no effect.
3. Used in event-driven sampling mode only.
4. TOW = Toggle On Write. Writing a 1 to a bit position within the register causes the corresponding bit position in the register to toggle.
5. These are 16-bit registers internal to SYSMONE1. These are mapped to the lower-half word boundary on 32-bit System Management Wizard IP core registers.
6. Writing to this SYSMONE1 hard macro register is not allowed. The SYSMONE1 hard macro data registers are 16 bits in width. The SYSMONE1 hard macro specification guarantees the first 10 MSB bits accuracy; so only these bits are used for reference.
7. Writing to this register resets the SYSMONE1 hard macro. No specific data pattern is required to reset the SYSMONE1 hard macro.
8. Read the SYSMONE1 User Guide, for setting the different bits available in configuration registers for UltraScale devices.
9. The OT upper register is a user-configurable register for the upper threshold level of temperature. If this register is left unconfigured, then the SYSMONE1 considers 125°C as the upper threshold value for OT. While configuring this register, the last four bits must be set to 0011, that is, Alarm Threshold Register 3[3:0] = 0011. The upper 12 bits of this register are user configurable.

System Management Wizard Local Register Grouping for AXI4-Lite Interface

It is expected that the System Management Wizard IP core registers are accessed in their preferred-access mode only. If a write attempt is made to read-only registers, there is no affect on register contents. If the write-only registers are read, the result is undefined data. All internal registers of the core must be accessed in 32-bit format. If there is any other kind of access (half-word or byte access) for local 32-bit registers, the transaction is completed with errors for the corresponding transaction.

Software Reset Register (SRR)

The Software Reset register permits you to reset the System Management Wizard IP core including the SYSMONE1 hard macro output ports (except JTAG-related outputs) independently of other IP cores in the systems. To activate a software reset, write

0x0000_000A to the register. Any other access, read or write, has undefined results. The bit assignment in the Software Reset register is shown in Figure 2-1 and described in Table 2-5.

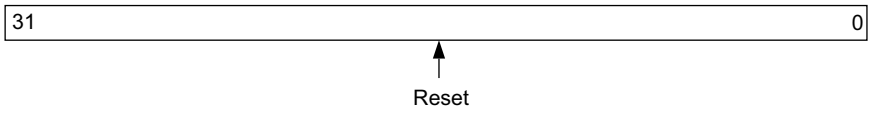

Figure 2-1: **Software Reset Register**

Table 2-5: **Software Reset Register Description (C_BASEADDR + 0x00)**

Bits	Name	Reset Value	Access Type	Description
31:0	Reset	N/A	W	The only allowed operation on this register is a write of 0x0000_000A, which resets the System Management Wizard IP Core. The reset is active only for 16 clock cycles.

Status Register (SR)

The Status register contains the System Management Wizard IP core channel status, EOC, EOS, and JTAG access signals. This register is read only. Any attempt to write the bits of the register is not able to change the bits. The Status Register bit definitions are shown in Figure 2-2 and explained in Table 2-6.

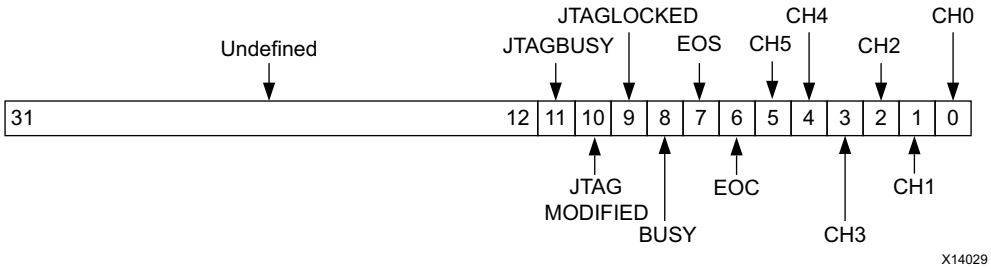

Figure 2-2: **Status Register**

Table 2-6: **Status Register (C_BASEADDR + 0x04)**

Bits	Name	Reset Value	Access Type	Description
31:12	Undefined	N/A	N/A	Undefined
11	JTAGBUSY	0	R	Used to indicate that a JTAG DRP transaction is in progress.
10	JTAG MODIFIED	0	R	Used to indicate that a write to DRP through JTAG interface has occurred. This bit is cleared when a successful DRP read/ write operation through the FPGA logic is performed. The DRP read/
9	JTAG LOCKED	0	R	Used to indicate that a DRP port lock request has been made by the

Table 2-6: **Status Register (C_BASEADDR + 0x04) *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
8	BUSY	N/A	R	ADC busy signal. This signal transitions High during an ADC conversion.
7	EOS	N/A	R	End of Sequence. This signal transitions to an active-High when the measurement data from the last channel in the auto sequence is written to the status registers. This bit is cleared when a read
6	EOC	N/A	R	End of Conversion signal. This signal transitions to an active-High at the end of an ADC conversion when the measurement is written to the SYSMONE1 hard macro status register. This bit is cleared when a read operation is performed
5:0	CHANNEL [5:0]	N/A	R	Channel selection outputs. The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.

Alarm Output Status Register (AOSR)

The Alarm Output Status register contains all the alarm outputs for the System Management Wizard IP core. This register is read-only. Any attempt to write the bits of the register is not able to change the bits. The Alarm Output Status register bit definitions are shown in Figure 2-3 and explained in Table 2-7.

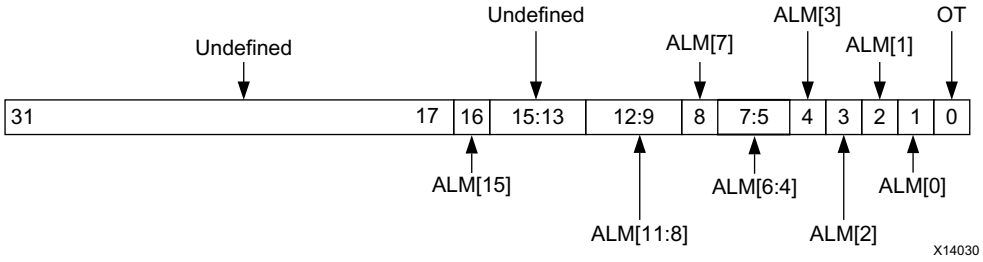

Figure 2-3: **Alarm Output Status Register**

Table 2-7: **Alarm Output Status Register (C_BASEADDR + 0x08)**

Bits	Name	Reset Value	Access Type	Description
31:17	Undefined	N/A	N/A	Undefined
16	ALM[15]	0	R	Logical ORing of ALARM bits 8 to 14. This is direct output from the SYSMONE1 macro.
15:13	Undefined	N/A	N/A	Reserved
12:9	ALM[11:8]	0	R	Alarms for User Supplies 0-3

Table 2-7: **Alarm Output Status Register (C_BASEADDR + 0x08) *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
8	ALM[7]	0	R	Logical ORing of ALARM bits 0 to 6. This is direct output from the SYSMONE1 macro.
7:5	ALM[6:4]	0	R	Reserved
4	ALM[3]	0	R	SYSMONE1 VBRAM-Sensor Status. SYSMONE1 VBRAM-sensor alarm output interrupt occurs when VBRAM exceeds user-defined threshold.
3	ALM[2]	0	R	SYSMONE1 VCCAUX-Sensor Status. SYSMONE1 VCCAUX-sensor alarm output interrupt occurs when VCCAUX exceeds user-defined threshold.
2	ALM[1]	0	R	SYSMONE1 VCCINT-Sensor Status. SYSMONE1 VCCINT-sensor alarm output interrupt occurs when VCCINT exceeds user-defined threshold.
1	ALM[0]	0	R	SYSMONE1 Temperature-Sensor Status. SYSMONE1 temperature-sensor alarm output interrupt occurs when device temperature exceeds user-defined threshold.
0	OT	0	R	SYSMONE1 Over-Temperature Alarm Status. Over-Temperature alarm output interrupt occurs when the die temperature exceeds a factory set limit of 125°C.

CONVST Register (CONVSTR)

The CONVST register is used for initiating a new conversion in the event-driven sampling mode. The output of this register is logically ORed with the external CONVST input signal. This register also defines enable for the Temperature Bus update logic and the wait cycle count. The attempt to read this register results in undefined data. The CONVST Register bit definitions are shown in Figure 2-4 and explained in Table 2-8.

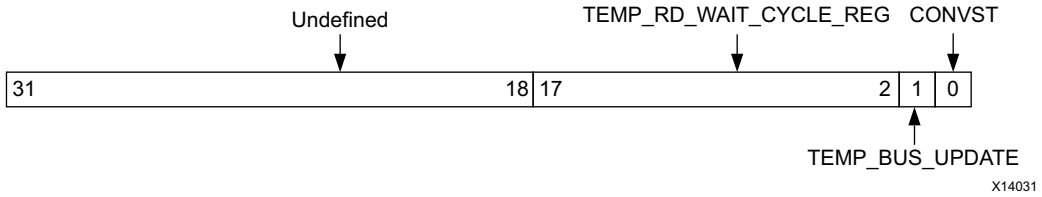

Figure 2-4: **CONVST Register**

Table 2-8: **CONVST Register (C_BASEADDR + 0x0C)**

Bits	Name	Reset Value	Access Type	Description
31:18	Undefined	N/A	N/A	Undefined
17:2	TEMP_RD_WAIT_CYCLE_REG	0x03E8	W	Wait cycle for temperature update. Temperature update logic waits for this count of the S_AXI_ACLK.
1	TEMP_BUS_UPDATE	0	W	Enable temperature update logic enables the temperature read from SYSMONE1 and updates of TEMP_OUT port.
0	CONVST	0	W	A rising edge on the CONVST input initiates start of ADC conversion in event-driven sampling mode. For the selected channel the CONVST bit in the register needs to be set to 1 and again reset to 0 to start a new conversion cycle. The conversion cycle ends with EOC bit going High.

SYSMONE1 Reset Register

The SYSMONE1 Reset register is used to reset only the SYSMONE1 hard macro. As soon as the reset is released the ADC begins with a new conversion. If sequencing is enabled this conversion is the first in the sequence. This register resets the OT and ALM[n] output from the SYSMONE1 hard macro. This register does not reset the interrupt registers if they are included in the design. Also any reset from the FPGA logic does not affect the RFI (Register File Interface) contents of SYSMONE1 hard macro. The attempt to read this register results in undefined data. The SYSMONE1 Reset register bit definitions are shown in Figure 2-5 and explained in Table 2-9.

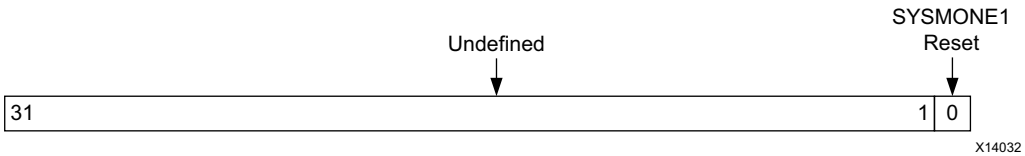

Figure 2-5: **SYSMONE1 Reset Register**

Table 2-9: **SYSMONE1 Reset Register (C_BASEADDR + 0x10)**

Bits	Name	Reset Value	Access Type	Description
31:1	Undefined	N/A	N/A	Undefined
0	SYSMONE1 Reset	0	Write	Writing 1 to this bit position resets the SYSMONE1 hard macro. The reset is released only after 0 is written to this register.

Interrupt Controller Register Grouping for AXI4-Lite Interface

The Interrupt Controller Module is included in the System Management Wizard IP core design when C_INCLUDE_INTR = 1. The System Management Wizard has several distinct interrupts that are sent to the Interrupt Controller Module, which is one of the submodules of System Management Wizard IP Core. The Interrupt Controller Module allows each interrupt to be enabled independently (by the IP Interrupt Enable register (IPIER)). All the interrupt signals are rising-edge sensitive.

Interrupt registers are strictly 32-bit accessible. If byte/half-word or without byte enables access is made, the core behavior is not guaranteed.

The interrupt registers are in the Interrupt Controller Module. The System Management Wizard permits multiple conditions for an interrupt or an interrupt strobe which occurs only after the completion of a transfer.

Global Interrupt Enable Register (GIER)

The Global Interrupt Enable register is used to globally enable the final interrupt output from the Interrupt Controller as shown in Figure 2-6 and described in Table 2-10. This bit is a read/write bit and is cleared upon reset.

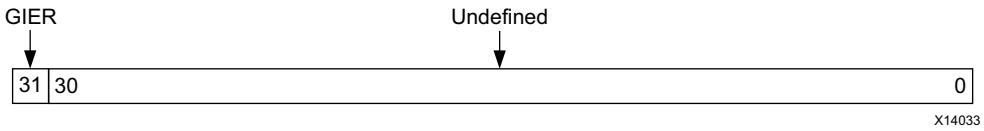

Figure 2-6: **Global Interrupt Enable Register (GIER)**

Table 2-10: **Global Interrupt Enable Register (GIER) Description (C_BASEADDR + 0x5C)**

Bits	Name	Reset Value	Access Type	Description
31	GIER	0	R/W	Global Interrupt Enable Register. It enables all individually enabled interrupts to be passed to the interrupt controller. • 0 = Disabled • 1 = Enabled
30:0	Undefine	N/A	N/A	Undefined.

IP Interrupt Status Register (IPISR)

Six unique interrupt conditions are possible in the System Management Wizard IP core. The Interrupt Controller has a register that can enable each interrupt independently. Bit assignment in the Interrupt register for a 32-bit data bus is shown in Figure 2-7 and described in Table 2-11. The interrupt register is a read/toggle on write register and by

writing a 1 to a bit position within the register causes the corresponding bit position in the register to toggle. All register bits are cleared upon reset.

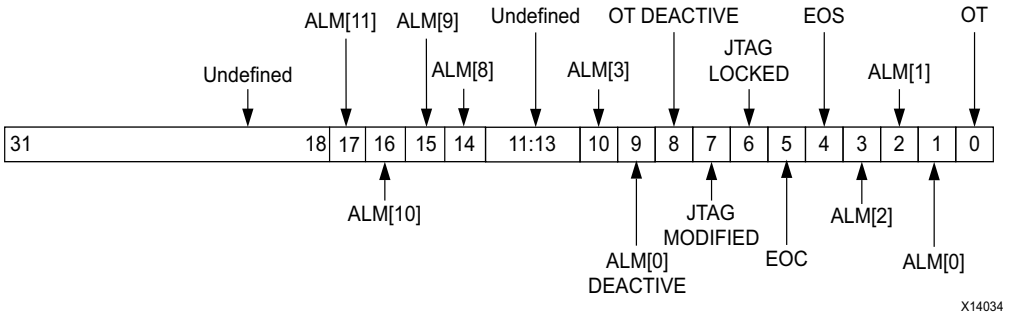

Figure 2-7: **IP Interrupt Status Register**

Table 2-11: **IP Interrupt Status Register (IPISR) Description (C_BASEADDR + 0x60)**

Bits	Name	Reset Value	Access Type	Description
31:18	Undefined	N/A	N/A	Undefined
17	ALM[11]	0	R/TOW(1)(2)	SYSMONE1 VUSER3-Sensor Interrupt. The SYSMONE1 VUSER3 sensor alarm output interrupt occurs when VUSER0 exceeds the user-defined threshold.
16	ALM[10]	0	R/TOW(1)(2)	SYSMONE1 VUSER2-Sensor Interrupt. The SYSMONE1 VUSER2-sensor alarm output interrupt occurs when VUSER2 exceeds the user-defined threshold.
15	ALM[9]	0	R/TOW(1)(2)	SYSMONE1 VUSER1-Sensor Interrupt. The SYSMONE1 VUSER1-sensor alarm output interrupt occurs when VUSER1 exceeds the user-defined threshold.
14	ALM[8]	0	R/TOW(1)(2)	SYSMONE1 VUSER0-Sensor Interrupt. The SYSMONE1 VUSER0-sensor alarm output interrupt occurs when VUSER0 exceeds the user-defined threshold.
11:13	ALM[4:6]	0	N/A	Undefined
10	ALM[3]	0	R/TOW(1)(2)	SYSMONE1 VBRAM-Sensor Interrupt. SYSMONE1 VBRAM-sensor alarm output interrupt occurs when VBRAM exceeds user-defined threshold.
9	ALM[0] Deactive	0	R/TOW	ALM[0] Deactive Interrupt. This signal indicates that the falling edge of the Over Temperature signal is detected. It is cleared by writing 1 to this bit position. The ALM[0] signal is generated locally from the core. This signal indicates that the SYSMONE1 macro has deactivated the Over Temperature signal output.
8	OT Deactive	0	R/TOW(1)	OT Deactive Interrupt. This signal indicates that falling edge of the Over Temperature signal is detected. It is cleared by writing 1 to this bit position. The OT Deactive signal is generated locally from the core. This signal indicates that the SYSMONE1 macro has deactivated the Over Temperature signal output.

Table 2-11: **IP Interrupt Status Register (IPISR) Description (C_BASEADDR + 0x60) *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
7	JTAG MODIFIED	0	R/TOW(1)(2)	JTAGMODIFIED Interrupt. This signal indicates that a write to DRP through the JTAG interface has occurred. It is cleared by writing 1 to this bit position.
6	JTAG LOCKED	0	R/TOW(1)(2)	JTAGLOCKED Interrupt. This signal is used to indicate that a DRP port lock request has been made by the Joint Test Action Group (JTAG) interface.
5	EOC	N/A	R/TOW(1)(2)	End of Conversion Signal Interrupt. This signal transitions to an active-High at the end of an ADC conversion when the measurement is written to the SYSMONE1 hard macro status register.
4	EOS	N/A	R/TOW(1)(2)	End of Sequence Interrupt. This signal transitions to an active-High when the measurement data from the last channel in the auto sequence is written to the status registers.
3	ALM[2]	0	R/TOW(1)(2)	SYSMONE1 V_{CCAUX}-Sensor Interrupt. SYSMONE1 V_{CCAUX}-sensor alarm output interrupt occurs when V_{CCAUX} exceeds the user-def ined threshold.
2	ALM[1]	0	R/TOW(1)(2)	SYSMONE1 V_{CCINT}-Sensor Interrupt. SYSMONE1 V_{CCINT}-sensor alarm output interrupt occurs when V_{CCINT} exceeds the user-def ined threshold.
1	ALM[0]	0	R/TOW(1)(2)	SYSMONE1 Temperature-Sensor Interrupt. SYSMONE1 temperature-sensor alarm output interrupt occurs when device temperature exceeds the user-defined threshold.
0	OT	0	R/TOW(1)(2)	Over-Temperature Alarm Interrupt. Over-Temperature alarm output interrupt occurs when the die temperature exceeds a factory set limit of 125 °C.

Notes:

1. TOW = Toggle On Write. Writing a 1 to a bit position within the register causes the corresponding bit position in the register to toggle.
2. This interrupt signal is directly generated from the SYSMONE1 hard macro.

IP Interrupt Enable Register (IPIER)

The IPIER has an enable bit for each defined bit of the IPISR as shown in Figure 2-8 and described in Table 2-12. All bits are cleared upon reset.

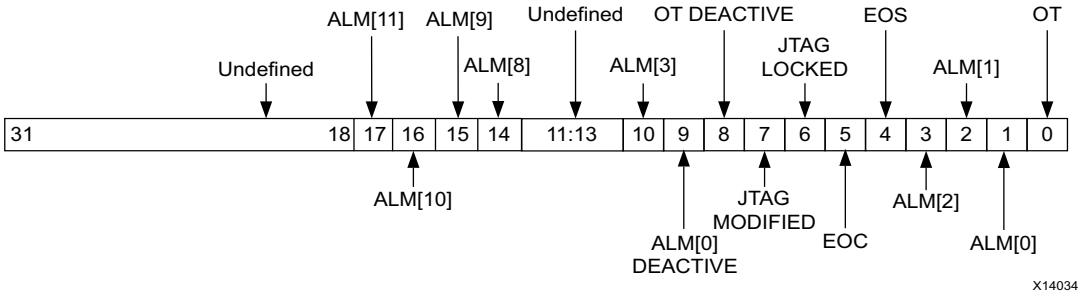

Figure 2-8: **IP Interrupt Enable Register (IPIER)**

Table 2-12: **IP Interrupt Enable Register (IPIER) Description (C_BASEADDR + 0x68)**

Bits	Name	Reset Value	Access Type	Description
31:18	Undefined	N/A	N/A	Undefined
17	ALM[11]	0	R/W	SYSMONE1 VUSER3-Sensor Interrupt • 0 = Disabled • 1 = Enabled
16	ALM[10]	0	R/W	SYSMONE1 VUSER2-Sensor Interrupt • 0 = Disabled • 1 = Enabled
15	ALM[9]	0	R/W	SYSMONE1 VUSER1-Sensor Interrupt • 0 = Disabled • 1 = Enabled
14	ALM[8]	0	R/W	SYSMONE1 VUSER0-Sensor Interrupt • 0 = Disabled • 1 = Enabled
11:13	ALM[4:6]	0	N/A	Undefined.
10	ALM[3]	0	R/W	SYSMONE1 VBRAM-Sensor Interrupt • 0 = Disabled • 1 = Enabled
9	ALM[0] Deactive	0	R/W	ALM[0] Deactive Interrupt • 0 = Disabled • 1 = Enabled
8	OT Deactive	0	R/W	OT Deactive Interrupt • 0 = Disabled • 1 = Enabled
7	JTAG MODIFIED	0	R/W	JTAGMODIFIED Interrupt • 0 = Disabled • 1 = Enabled
6	JTAG LOCKED	0	R/W	JTAGLOCKED Interrupt • 0 = Disabled • 1 = Enabled

Table 2-12: **IP Interrupt Enable Register (IPIER) Description (C_BASEADDR + 0x68) *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
5	EOC	0	R/W	End of Conversion Signal Interrupt • 0 = Disabled • 1 = Enabled
4	EOS	0	R/W	End of Sequence Interrupt • 0 = Disabled • 1 = Enabled
3	ALM[2]	0	R/W	SYSMONE1 V_{CCAUX}-Sensor Interrupt • 0 = Disabled • 1 = Enabled
2	ALM[1]	0	R/W	SYSMONE1 V_{CCINT}-Sensor Interrupt • 0 = Disabled • 1 = Enabled
1	ALM[0]	0	R/W	SYSMONE1 Temperature-Sensor Interrupt • 0 = Disabled • 1 = Enabled
0	OT	0	R/W	Over-Temperature Alarm Interrupt • 0 = Disabled • 1 = Enabled

Locally Generated Interrupt Bits in IPIER and IPISR

The interrupt bits ranging from Bit[16] to Bit[0] in IPISR as well as IPIER are direct output signals of the SYSMONE1 hard macro. The signals like OT Deactive (Bit[8]), ALM[0] Deactive (Bit[9]), are locally generated in the core. These interrupts are generated on the falling edge of the Over Temperature and AML[0] signals. The falling edge of these signals can be used in controlling external things like controlling the fan or air-conditioning of the system.

Hard Macro Register (DRP Register) Grouping for AXI4-Lite Interface

The SYSMONE1 hard macro register set consists of all the registers present in the SYSMONE1 hard macro on 7 series FPGAs. The addresses of these registers are shown in Table 2-4. Because these registers are 16 bits wide but the processor data bus is 32 bits wide, the hard macro register data resides on the lower 16 bits of the 32-bit data bus. See Figure 2-9.

The 10-bit MSB aligned A/D converted value of different channels from SYSMONE1 hard macro are left-shifted and reside from bit position 15 to 6 of the processor data bus. The remaining bit positions from 5 to 0 should be ignored while considering the ADC data for different channels. Along with 16-bit data, the JTAGMODIFIED and JTAGLOCKED bits are passed that can be used by the software driver application for determining the validity of the DRP read data.

The JTAGMODIFIED bit is cleared when a DRP read/write operation through the FPGA logic is successful. If JTAGLOCKED = 1, a DRP read/write through the FPGA logic fails. The JTAGLOCKED signal is independently controlled through JTAG TAP. These SYSMONE1 hard macro registers should be accessed in their preferred access-mode only. The System Management Wizard IP core is not able to differentiate any non-preferred access to the SYSMONE1 hard macro registers.

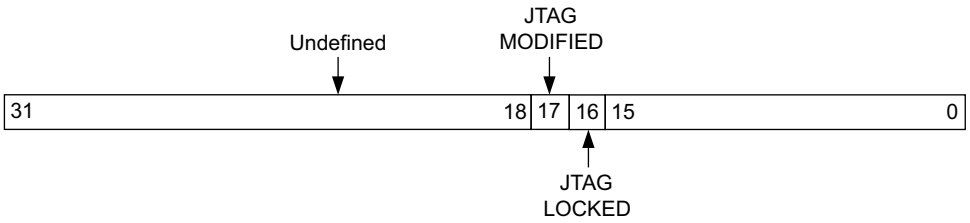

Figure 2-9: **DRP Register**

DRP registers are accessed as part of the core local registers.

IMPORTANT: *These registers must be accessed through the core local registers. Any attempt to access these registers in byte or half-word method returns an error response from core.*

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Clocking

The clock to SYSMONE1 primitive is `dclk`. When AXI4-Lite is selected as the bus interface, `dclk` is connected to the `s_axi_aclk` clock . So, the `adcclk` division factor must be programmed in correlation with the `s_axi_aclk` frequency.

When DRP or None interface is selected, `dclk` clock is at the top-level of the IP, and `adcclk` division factor must be programmed in correlation with the `dclk` frequency.

When Streaming is enabled for DRP or None interface selection, `m_axis_aclk` is connected to `dclk`.

Resets

When AXI4-Lite is selected as the bus interface, certain registers of the IP can be reset by writing a value 0xA to register 0x00. The AXI4-Lite and AXI4-Stream interfaces also have individual reset pins.

When DRP or None interface is selected, `reset_in` is the input port at the top-level of the IP.

Protocol Description

For more detailed information, see the AXI4-Lite protocol specifications. Figure 3-1 shows the simulation snapshots for Temperature value read from SYSMONE1 register.

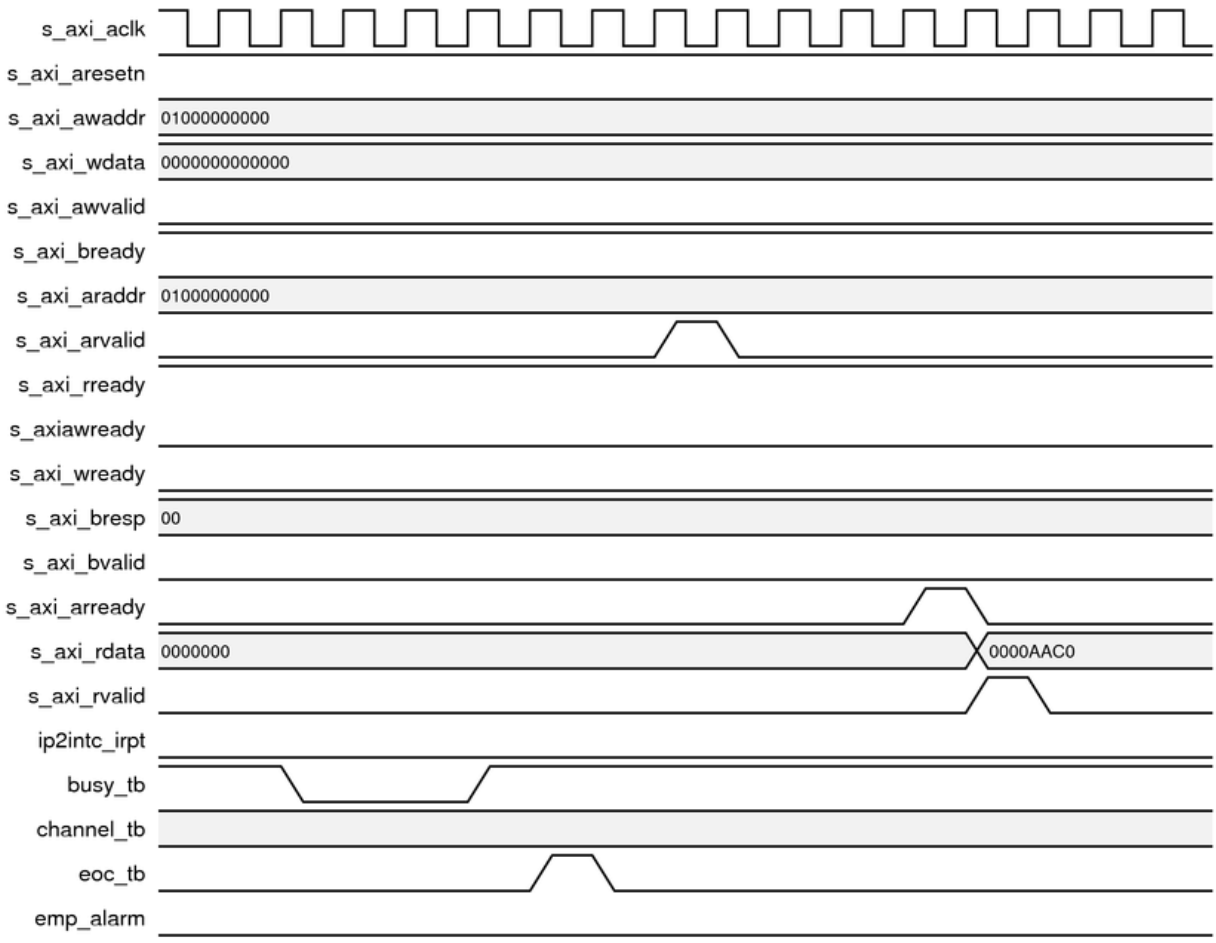

Figure 3-1: **AXI4-Lite Interface Reading Temperature Values in Simulation**

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows in the IP Integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 2]
- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 7]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the Vivado IP Integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref X] for detailed information. IP Integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

This chapter describes the use of system Management Wizard v1.0 in Vivado® Integrated Design Environment (IDE).

TIP: *Tool tips are available in the Vivado IDE for most features. Place your mouse over the relevant text, and additional information is provided in a dialog box.*

Vivado Integrated Design Environment (IDE)

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog under **FPGA Features and Design**.
2. **Double-click System Management Wizard** or select the Customize IP command from the toolbar or right-click menu .

For details, see the sections, "Working with IP" and "Customizing IP for the Design" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the "Working with the Vivado IDE" section in the *Vivado Design Suite User Guide: Getting Started* (UG910).

Note: Figures in this chapter are illustrations of the Vivado IDE. This layout might vary from the current version.

TIP: *This section describes how to set up a project in the Vivado Design Suite flow. Before generating the example design, set up the project as described in Creating a Directory and Setting the Project Options of this guide.*

The Component Name is a user selectable component name. Component names must not contain any reserved words in Verilog or VHDL.

Basic Tab

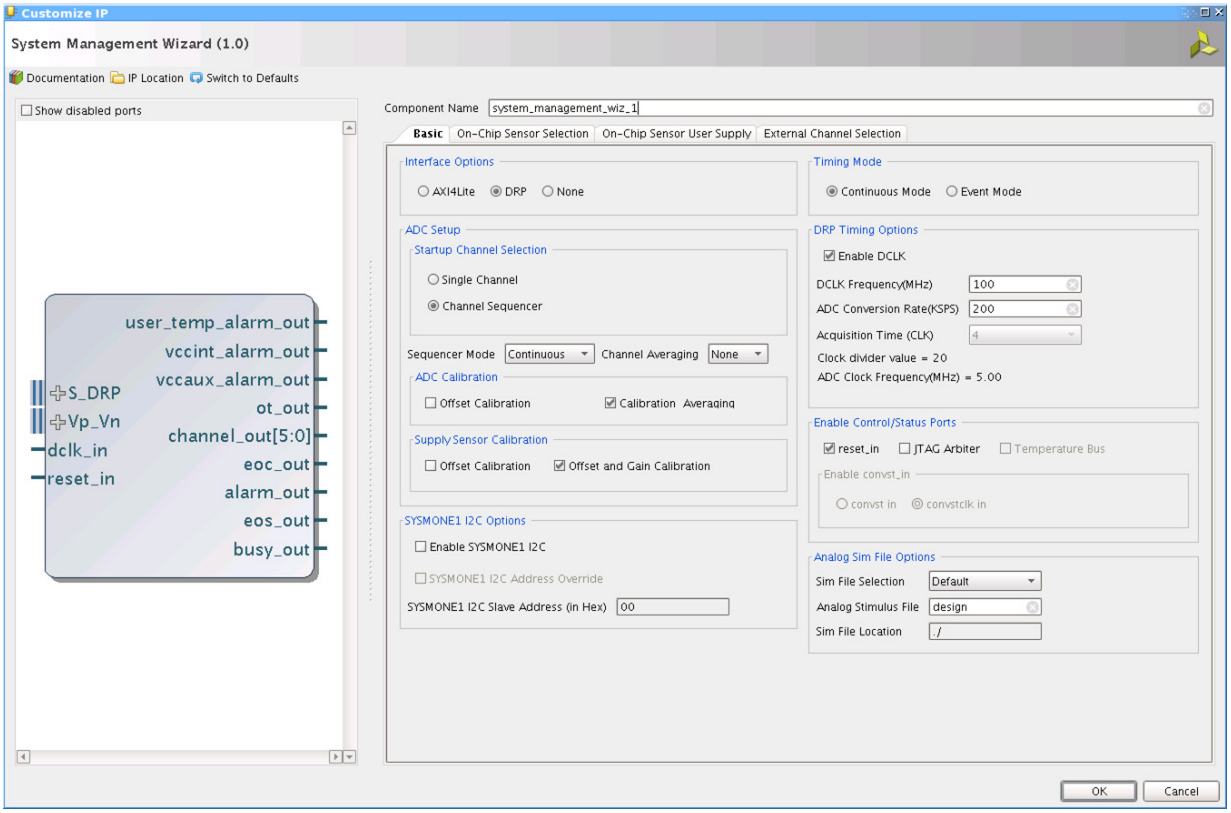

Figure 4-1: **Basic Tab**

The parameters on the Basic tab are as follows:

- **Interface Options**: Selects the interface for the System Management Wizard. DRP is the default option. You can select AXI4-Lite, DRP, or None. The DRP port is the FPGA logic interface for SYSMONE1. It facilitates access to the register file interface of the SYSMONE1. The SYSMONE1 control registers can be read or written using this port. This port can only be enabled when DCLK clock is present.
- ADC Setup
  - **Startup Channel Selection**: SYSMONE1 can be configured in one of the following modes:
    - Single Channel: In this mode, you can select only one channel to monitor. All channels and alarms shown in the GUI for Sequencer mode are also available for single-channel mode in the drop-down list, allowing only one channel on any tab.
    - Channel Sequencer: Allows you to select any number of channels to monitor. The channels to be used for this mode can be selected on all other tabs.

      For more information about the Channel Sequencer mode, see the *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
  - **Sequencer Mode**: If the SYSMONE1 is configured for Channel Sequencer mode, you can choose the required sequencer mode. The available options are Continuous, One-pass or Default mode.
  - **Channel Averaging**: Select the required averaging value. The available options are None, 16, 64, and 256.
  - **ADC Calibration/Supply Sensor Calibration**: You can select ADC offset calibration and the type of supply sensor calibration by checking the respective check boxes. Calibration averaging is enabled by default in SYSMONE1. You can disable this by deselecting the box.
- **SYSMONE1 I^2C Options**: Enables SYSMONE1 I2C pins and configuration to get access to the DRP registers pre and post configuration. SYSMONE1 calculates it's own I^2C address (at power-up the voltage on the dedicated analog input channel VP/VN is measured and the four MSBs of the measured value are used to decode the I^2C slave address), but you can override this by enabling SYSMONE1 I^2C Address Override option in the Vivado IDE.

Table 4-1: **I^2C Slave Address Decoding**

MSBs of Measured Voltage	I^2C Slave Address
0000	0110010
0001	0001011
0010	0010011
0011	0011011
0100	0100011

Table 4-1: **I²C Slave Address Decoding *(Cont'd)***

MSBs of Measured Voltage	I²C Slave Address
0101	0101011
0110	0110011
0111	0111011
1000	1000011
1001	1001011
1010	1010011
1011	1011011
1100	1100011
1101	1101011
1110	1110011
1111	0111010

- **Timing Mode**:
  - **Continuous Mode**: In this mode, the SYSMONE1 continues to sample and convert the selected channel/channels.
  - **Event Mode**: This mode requires an external trigger event, CONVST or CONVSTCLK, to start a conversion on the selected channel. Event Mode should only be used with external channels.
- **DRP Timing Options**: The SYSMONE1 clock (ADCCLK) is derived from the dynamic reconfiguration port (DRP) clock DCLK. The SYSMONE1 supports a DRP clock frequency of up to 250 MHz. The SYSMONE1 can also operate in the absence of DCLK. For more information on the DRP see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].

  The ADC Clock Frequency should be 1-5.2 MHz. To support this lower frequency clock, the SYSMONE1 has an internal clock divider. Specify the external DCLK frequency and required ADC conversion rate (maximum 0.2 Msps) in the Vivado® IDE. Based on the value of DCLK clock, the wizard calculates the appropriate clock divider value based on the values of DCLK clock and ADC conversion. The wizard also displays the ADC Clock frequency value and the actual conversion rate of the ADC.
- **Enable Control/Status Ports**: The Control/Status Port Selection allows you to select the I/O ports on the SYSMONE1 primitive.
  - **reset_in**: Allows an external input reset signal to be connected to the SYSMONE1.
  - **Enable convst_in**: Sets convst_in or convstclk_in as trigger sources for Event Mode Timing.
  - **Temperature Bus**: There is only one SYSMONE1 primitive available in a FPGA for use. If the System Management Wizard core is used in a system using MIG, the

TEMP_OUT bus should be connected to the device_temp_i input port of the MIG block. This disables inference of the SYSMONE1 hard block in MIG. Enabling temperature bus provides a 10-bit TEMP_OUT port with the temperature update logic. This checkbox is available when the interface option is AXI4-Lite.

- **JTAG Arbiter**: Enables JTAG status ports to check the status of JTAG access to SYSMONE1 registers. Other output status signals are also provided to facilitate interfacing of the SYSMONE1 to a user design. For more information, see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].
- **Analog Sim File Options**: You can provide the relative or absolute path and update the name of the Analog Stimulus File in this section.
  - **Sim File Selection**: The default name and path for the analog stimulus is design.txt. It is generated in the core simulation area. By changing the default option to relative path, you can set a custom path.
  - **Analog Stimulus File**: Customizes the name of the SYSMONE1 analog stimulus file.
  - **Sim File Location**: Enabled when Sim File Selection is not default. Relative or absolute path of the analog stimulus can be provided in this box. Relative path is with respect to the simulation directory. If the example design behavioral simulation is run, the relative path is with respect to `project_1/system_management_wiz_0_example/system_management_wiz_0_example.sim/sim_1/behav` directory.

On-Chip Sensor Setup

All on-chip sensor channels (Temperature, VCCINT, VCCAUX, and others) are available for selection in this tab.

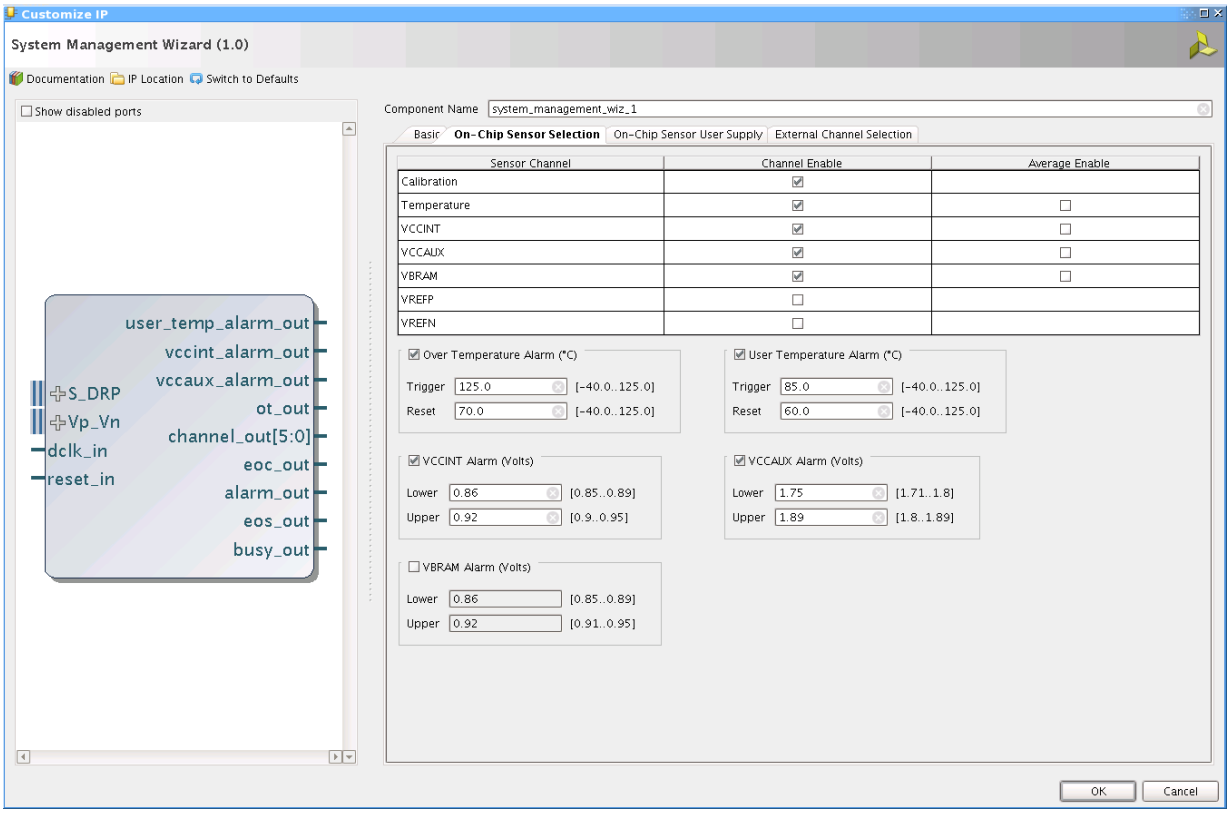

Figure 4-2: **On-Chip Sensor Selection and Alarms for Channel Sequencer**

The alarms listed in this tab (Figure 4-2) allows the alarm outputs to be enabled for the on-chip sensors. If a measurement of an on-chip sensor lies outside the specified limits, then a logic output goes active if enabled. For a detailed description of the alarm functionality see *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580) [Ref 1].

Use the checkboxes to enable alarm logic outputs.

- **Over Temperature Alarm and User Temperature Alarm**: Trigger and Reset levels for temperature alarm output can be entered using these fields. Both fields can be set.
- **VCCINT Alarm, VCCAUX Alarm, and VBRAM Alarm**: Both upper and lower alarm thresholds can be specified for the on-chip power supplies. If the measured value moves outside these limits, the alarm logic output goes active. The alarm output is reset when a measurement inside these limits is generated. The default limits in the Vivado IDE represent ±5% on the nominal supply value.

On-Chip Sensor User Supply Tab

On-Chip Sensor User supply (VUSER 0 - 3) can be enabled for monitoring up to three supplies for HP banks and up to four supplies for HR banks. User supplies are hooked to four SYSMONE1 analog bus in each quadrant of UltraScale architecture-based devices. A range of banks depending on the position with respect to SYSMONE1 block in FPGA are

placed into four quadrants NE, SW, SE, NW respectively. Select the bank and supply for each enabled VUSER supply or alarm. The System Management Wizard runs DRC to check the valid configuration of the VUSER bank and supply.

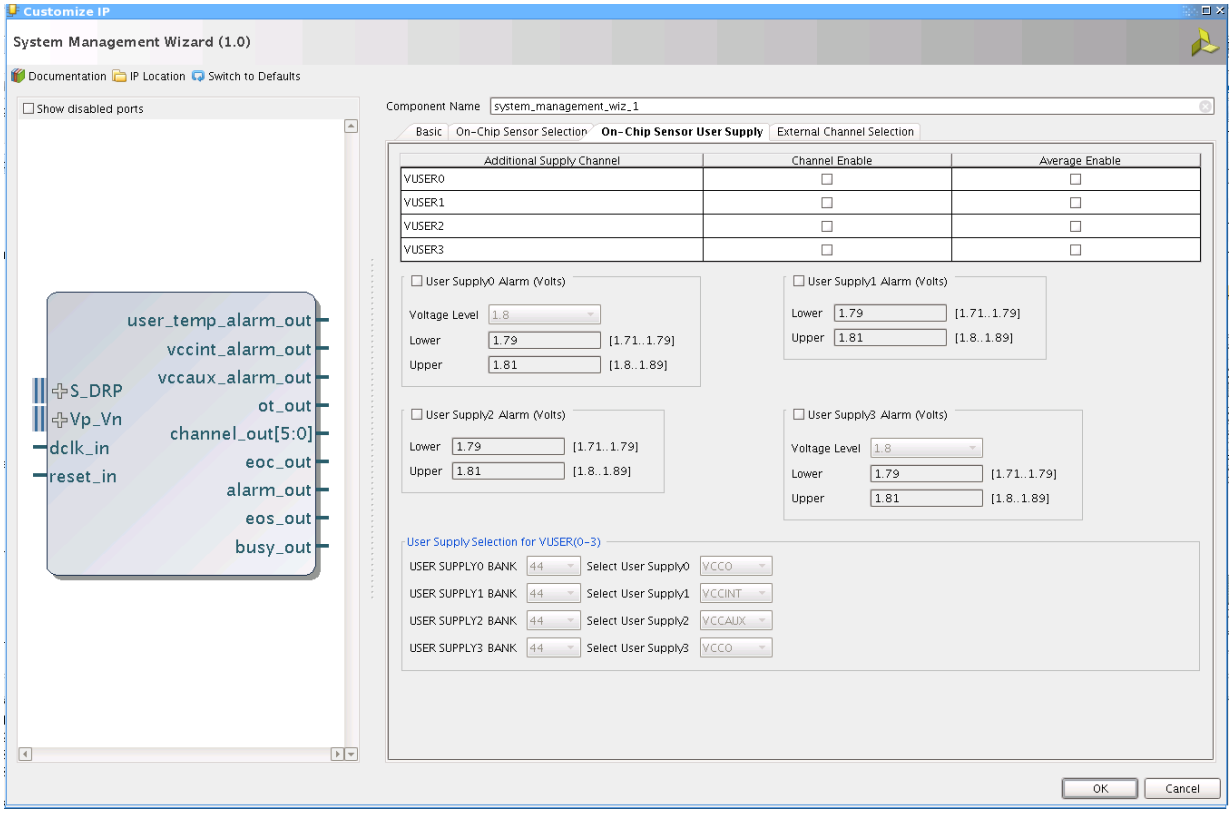

Figure 4-3: **On-Chip Sensor User Supply and Alarms Tab for Channel Sequencer**

- **Channel Enable and Average Enable**: Use the checkboxes to enable alarm logic outputs.
  - VUSER0
  - VUSER1
  - VUSER2
  - VUSER3
- **User Supply0, User Supply1, User Supply2, User Supply3 Alarms**: Both upper and lower alarm thresholds can be specified for the selected user supplies. The range varies with the type of the supply. If the measured value moves outside these limits, the alarm logic output goes active. The alarm output is reset when a measurement inside these limits is generated. The default limit is ±5% on the nominal supply value.

External Channel Selection Tab

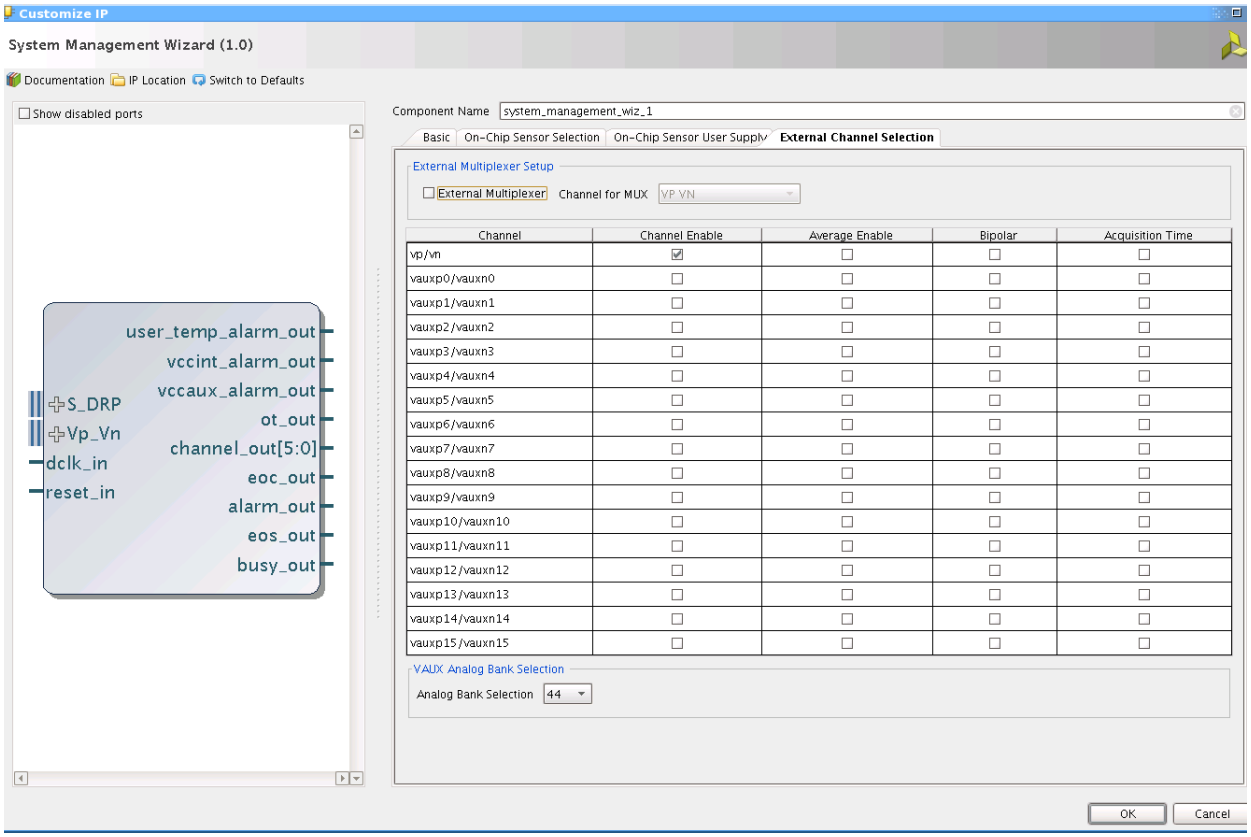

Figure 4-4: **External Channel Selection Tab for Channel Sequencer**

- **External Multiplexer Setup**: SYSMONE1 supports a timing mode that uses an external analog multiplexer when device I/O resources might be limited, or when auxiliary analog I/O are more valuable when used to implement another interface.
  - **External Multiplexer**: Enables the external multiplexer.
  - **Channel for MUX**: Specifies the external channel to which the MUX connects.
  - **External Channel Configuration**: All external channels Vp/Vn and VAUXP/N [0-15] are available in this tab. Use this to select channels for monitoring, enable averaging, enable bipolar mode and increase the acquisition time for selected channels.
- **VAUX Analog Bank Selection**: Available banks of selected part that contains the VAUX pin pairs. Constraints (XDC) for the enabled VAUX channels are written by the System Management Wizard for the selected bank.

Generating the HDL Wrapper

After selecting the configuration options, click **OK** on the System Management Wizard screen to generate the HDL wrapper and other System Management Wizard outputs.

The output files are placed in the `<project_name>/<project_name>.srcs/sources_1/ip/<component_name>/` directory you selected or created when setting up a new Vivado Design Environment project.

Output Generation

For details, see "Generating IP Output Products" in the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Core

This section contains information about constraining the core in the Vivado® Design Suite.

Required Constraints

For the AXI4-Lite interface, the required constraint is:

create_clock -period <*period-in-ns*> [get_ports s_axi_aclk]

For the DRP interface, required constraint is:

create_clock -period <*period-in-ns*> [get_ports dclk_in]

Clock Frequencies

The System Management Wizard supports clock frequencies 8 to 250 MHz.

Clock Management

Depending on the configuration, the ADC clock is internally divided by the SYSMONE1 primitive to achieve the desired sampling rate.

Simulation

This section contains information about simulating IP in the Vivado® Design Suite.

Analog waveform simulation is performed using the `design.txt` file which contains the time reference and the analog values for a selected channel. This file is generated by default. The analog and its digital equivalence comparison is in the example design test bench to verify the SYSMONE1 behavior.

You can provide your own waveform in a file using the relative path option in the Vivado IDE. In this case, the comparison values should be updated with respect to the analog stimulus to complete the example design simulation without error.

Simulation of channel averaging is not supported in the System Management Wizard example design test bench.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5].

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado® Design Suite.

UltraScale™ architecture-based devices need LOC constraints for VAUXP/VAUXN pin pairs to be specified in XDC. VP/VN is a dedicated input and does not need any pin LOC constraint. Each UltraScale device bank contains 16 dual IO pin pairs to support analog IO functionality. The System Management Wizard generates these constraints depending on the user selected bank for VAUX pin pairs.

To support the I^2C interface, System Management Wizard generates pin LOC constraints on the dual purpose I^2C pin for the implementation.

For details about synthesis and implementation, see "Synthesizing IP" and "Implementing IP" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

The following files describe the top-level example design for the System Management Wizard core.

VHDL

```
<project_name>/<project_name>.srcs/sources_1/ip/<component_name>/ example_design/
<component_name>_exdes.vhd
```

Verilog

```
<project_name>/<project_name>.srcs/sources_1/ip/<component_name>/example_design/
<component_name>_exdes.v
```

The example design, instantiates the SYSMONE1 core that is generated by the wizard.

Open Example Project Flow

In the Vivado Design Environment, use the following command to create an example project flow:

```
open_example_project [get_ips <component_name>]
```

Use of this command in the Tcl Console invokes a separate example design project that creates `<component_name>_exdes` as the top module for synthesis and `<component_name>_tb` as the top module for simulation. Implementation or simulation of the example design can be run from the example project.

Test Bench

This chapter contains information about the test bench provided in the Vivado® Design Suite.

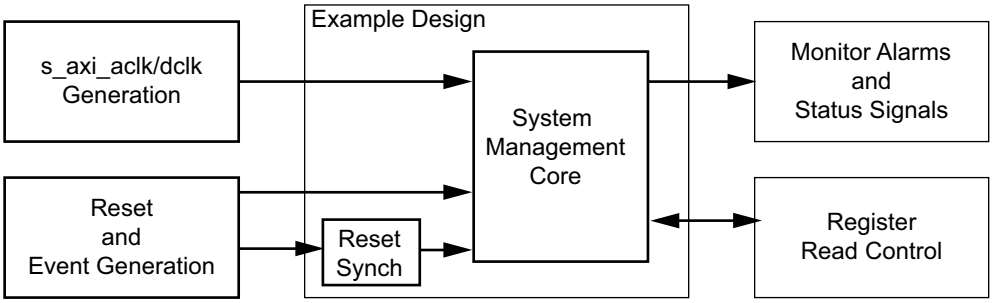

Figure 6-1: **System Management Wizard Test Bench**

The following files describe the demonstration test bench.

VHDL

```
<project_name>/<project_name>.srcs/sources_1/ip/<component_name>/simulation/
<component_name>_tb.vhd
```

Verilog

```
<project_name>/<project_name>.srcs/sources_1/ip/<component_name>/simulation/
<component_name>_tb.v
```

The demonstration test bench is a simple VHDL or Verilog program to exercise the example design and the core. The demonstration test bench performs the following tasks:

- Generates the input `s_axi_aclk/dclk` clock signal.
- Applies a reset to the example design.
- Monitors the alarms and other status outputs.
- Reads the respective registers when a conversion is complete.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

TIP: *If the IP generation halts with an error, there might be a license issue. See License Checkers in Chapter 1 for more details.*

Finding Help on Xilinx.com

To help in the design and debug process when using the System Management Wizard, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the System Management Wizard. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name

- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the System Management Wizard

AR: 58763

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Additional Resources.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Log in to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address System Management Wizard design issues. It is important to know which tools are useful for debugging various situations.

Vivado Lab Tools

Vivado® lab tools insert logic analyzer and virtual I/O cores directly into your design. Vivado lab tools also allow you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature represents the functionality in the Vivado IDE that is used for logic debugging and validation of a design running in Xilinx devices in hardware.

The Vivado lab tools logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 6].

Reference Boards

Various Xilinx development boards support thethe System Management Wizard. These boards can be used to prototype designs and establish that the core can communicate with the system.

Simulation Debug

The simulation debug flow for Questa® SIM is illustrated below. A similar approach can be used with other simulators.

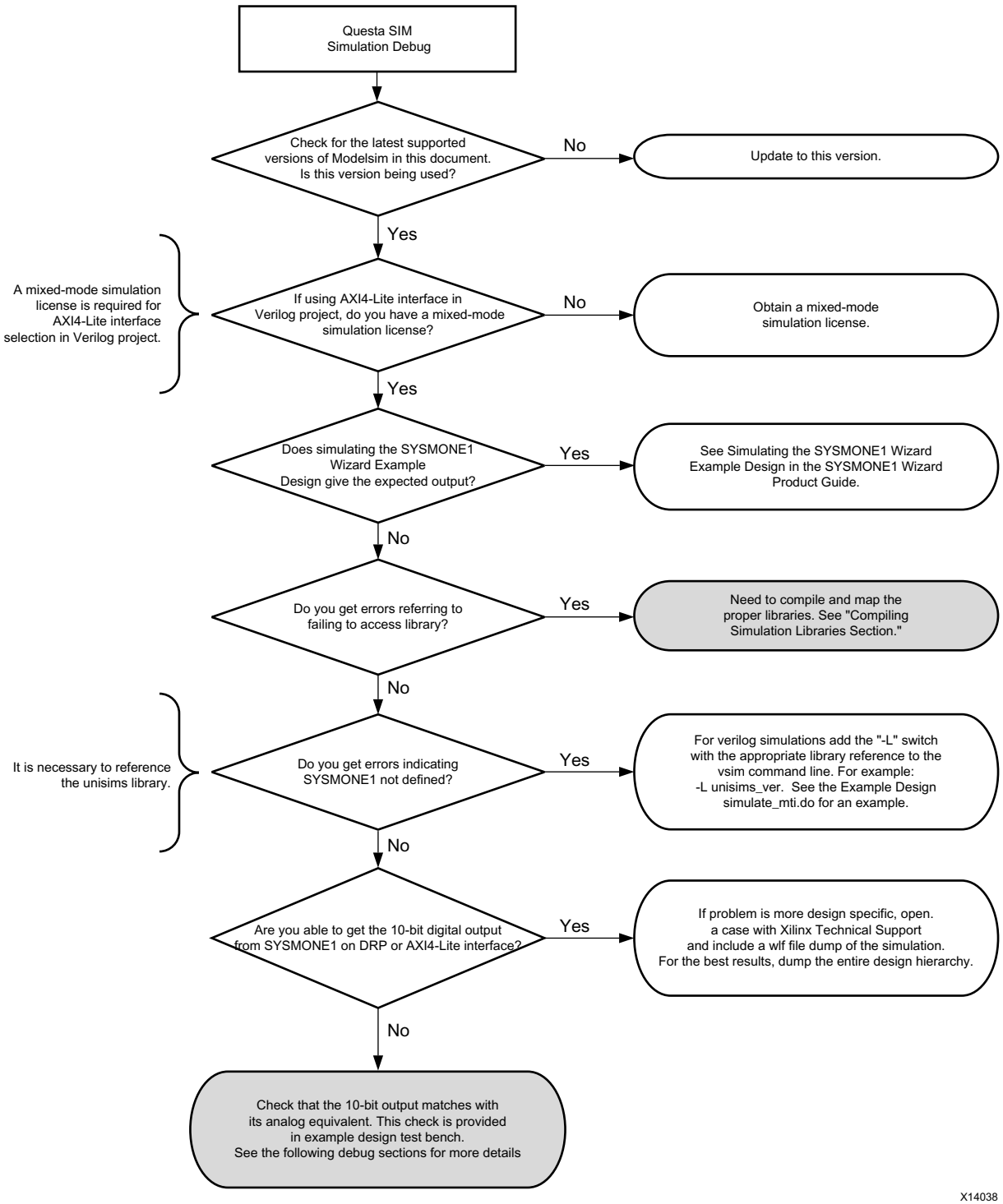

Figure A-1: **Questa SIM Debug Flow Diagram**

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado lab tools are a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the Vivado lab tools for debugging the specific problems.

General Checks

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the `locked` port.
- If your outputs go to 0, check your licensing.

Interface Debug

AXI4-Lite Interfaces

Read from a register that does not have all 0s as a default to verify that the interface is functional. Output `s_axi_arready` asserts when the read address is valid, and output `s_axi_rvalid` asserts when the read data/response is valid. If the interface is unresponsive, ensure that the following conditions are met:

- The `s_axi_aclk and aclk` inputs are connected and toggling.
- The interface is not being held in reset, and `s_axi_areset` is an active-Low reset.
- The interface is enabled, and `s_axi_aclken` is active-High (if used).
- The main core clocks are toggling and that the enables are also asserted.
- If the simulation has been run, verify in simulation and/or a Vivado Lab tools capture that the waveform is correct for accessing the AXI4-Lite interface.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary.

References

These documents provide supplemental material useful with this product guide:

1. *UltraScale Architecture System Monitor Advanced Specification User Guide* (UG580)
2. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
3. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
4. *Vivado Design Suite User Guide: Implementation* (UG904)
5. *Vivado Design Suite User Guide: Designing with IP* (UG896)
6. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
7. *Vivado Design Suite User Guide: Getting Started* (UG910)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/2014	1.0	Updated IP core registers.
12/18/2013	1.0	Initial Xilinx release.

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