XILINX®

LogiCORE IP Serial RapidIO v5.6

DS696 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP Serial RapidIO Endpoint solution comprises a highly flexible and optimized Serial RapidIO Physical Layer core and a Logical (I/O) and Transport Layer interface. This IP solution is a netlist for RapidIO interconnect that supports 1x and 4x lane widths. It comes with a configurable buffer design, reference clock module, reset module, and register manager reference design, which allows complete flexibility in selecting primitives. This solution is fully verified and supports both Verilog® and VHDL design environments.

Features

- Designed to *RapidIO Interconnect Specification v2.1*
- Supports 1x and 4x operation with the ability to train down to 1x from 4x
- Supports speeds of 1.25, 2.5, 3.125, and 5.0 Gbaud

Logical Layer

- Supports a peak, unidirectional bandwidth of 16 Gbps when operating at 250 MHz
- Concurrent Initiator and Target operations
- Doorbell and Message support
- 64-bit internal data path
- Dedicated port for maintenance transactions
- Simple handshaking mechanism to control data flow
- Programmable source ID on all outgoing packets
- Optional large system support for 16-bit Device IDs

Buffer

- Independently configurable TX and RX Buffer depths of 8, 16, or 32 packets
- Support for independent clocks
- Optional TX Flow Control support

Physical Layer

- Supports critical request flow
- Optional support of priority-based, retransmit suppression
- Support for multicast events
- Supports removal of corrupted packets for error detection and initiates automatic error recovery
- Design verified using the RapidIO Trade Association Bus Functional Model
- For sub-features, use only as necessary

LogiCORE IP Facts				
Core Specifics				
Supported Family[1]	Virtex-6	Spartan-6	Virtex-5	Virtex-4[2]
Minimum Supported Device	6VLX75T-1[3]	6SLX25T-2[4]	5VLX30T-1	4VFX20-10
Width	1x, 4x	1x, 4x	1x, 4x	1x, 4x
Perf. Gbps	1.25 2.5 3.125 5.0[5]	1.25 2.5 3.125	1.25 2.5 3.125	1.25 2.5 3.125
Resources Used	See Table 1.			
Provided with Core				
Documentation	Product Specification User Guide			
Design File Formats	Verilog and VHDL Simulation Models NGC Netlist			
Constraints File	User Constraints File (ucf)			
Example Design	Register Manager Design			
Design Tools				
Supported HDL	Verilog and VHDL[6]			
Synthesis	XST Synopsys Synplify Pro E-2011.03			
Xilinx Tools	ISE v13.1			
Simulation Tools[7]	Cadence Incisive Enterprise Simulator (IES) v10.2 Synopsys VCS and VCS MX 2010.06 Mentor Graphics ModelSim v6.6d			

1. For the complete list of supported devices, see the release notes for this core.
2. Virtex®-4 FX FPGA solutions require the latest silicon stepping.
3. 4x cores running at 5.0 Gbps require -2 or faster silicon.
4. 1x at 3.125 Gbps, 4x cores require -3 or faster silicon.
5. 5.0 Gbps is not supported for Virtex-6 CXT devices.
6. Not available for Virtex-4 FPGA designs.
7. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Table 1: **Core Resources Used**

	Logical Layer							
	Virtex-6		**Spartan-6**		**Virtex-5**		**Virtex-4**	
LUTs	1850		1800		1800		2400	
Flip Flops	1800		1800		2200		2200	
Slices[1]	800		800		1400		1500	
	Buffer							
	Virtex-6		**Spartan-6**		**Virtex-5**		**Virtex-4**	
	Min[2]	**Max**[3]	**Min**[2]	**Max**[4]	**Min**[5]	**Max**[3]	**Min**[5]	**Max**[3]
LUTs	500	700	500	550	450	800	600	1150
Flip Flops	800	950	800	850	600	950	600	950
Slices[1]	250	400	250	350	350	500	550	950
Block RAM	2	8	2	4	2	8	4	16
	Physical Layer							
	Virtex-6		**Spartan-6**		**Virtex-5**		**Virtex-4**	
	1x	4x	x1	x4	1x	4x	1x	4x
LUTs	3450	3950	3100	4050	3100	3800	4200	5600
Flip Flops	2650	3250	2650	3300	2800	3400	2800	3800
Slices[1]	1200	1300	1200	1350	2100	2400	2300	3100
DCM/PLL/MMCM	1	1	1	1	1	1	1	1
BUFG	2	2	4	4	4	4	4	5
Transceiver	1	4	1	1	1	4	1	4

1. Slice count values are only an estimate, the exact number of slices depends on user core configuration and level of resource sharing with adjacent logic.
2. Buffer configured with 8 deep TX and RX buffers, asynchronous clock support, and RX Flow Control.
3. Buffer configured with 32 deep TX and RX buffers, asynchronous clock support, and TX/RX Flow Control (Virtex-6 CXT devices do not support 32 deep buffers).
4. Buffer configured with 16 deep TX and RX buffers, asynchronous clock support, and TX/RX Flow Control (Spartan-6 devices do not support 32 deep buffers).
5. Buffer configured with 8 deep TX and RX buffers, no asynchronous clock support, and RX Flow Control only.

Applications

The Serial RapidIO Endpoint solution is well suited for control and data operations in communication and embedded systems requiring high-speed I/O with low latency. Typical applications include:

- Wireless Base Stations as interconnect on Channel Cards or Radio Equipment controller
- DSP farms for image & signal processing—ideal for multi-processor communication interconnect
- Scientific, military, and industrial equipment
- High-availability enterprise storage as reliable, low latency, and high bandwidth memory interface
- Edge Networking – multimedia data compression

Functional Overview

The Xilinx RapidIO Endpoint solution is comprised of the LogiCORE IP Serial RapidIO Physical Layer (PHY) core, LogiCORE IP RapidIO Logical (I/O) and Transport Layer core (LOGIO), LogiCORE IP Serial RapidIO Buffer core, and reference designs to handle clocking, reset and configuration accesses. The Xilinx Serial RapidIO Endpoint Solution functional overview is shown in Figure 1.

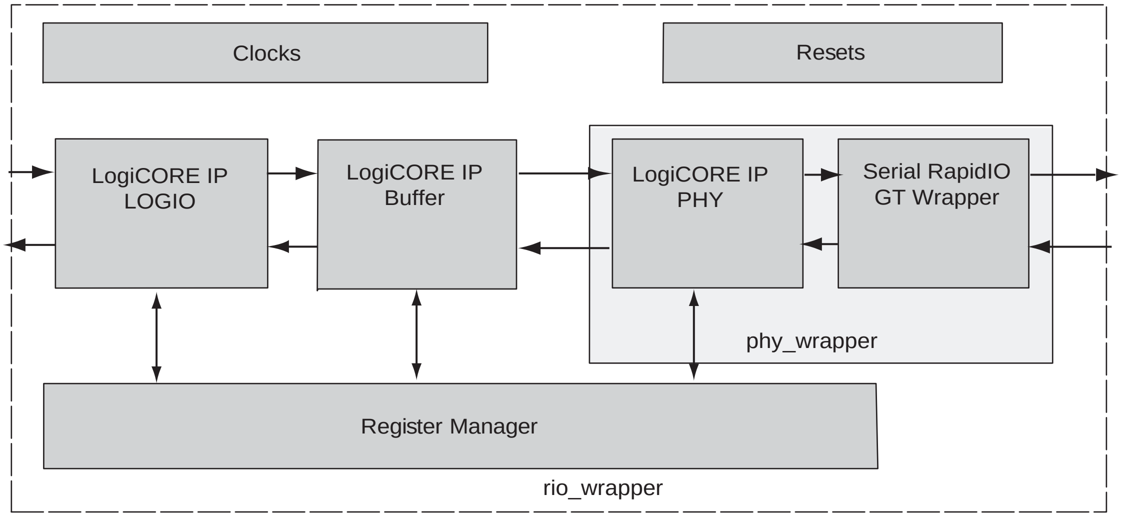

Figure 1: **Serial RapidIO Functional Overview**

Serial RapidIO System Overview

The Xilinx RapidIO Endpoint solution is delivered through a layered approach to allow for integration of specific and relevant portions of a design. The `phy_wrapper` integrates only the PHY core along with the transceivers. This is useful for those users who are interested in implementing PHY functionality only.

The `rio_wrapper` integrates the `phy_wrapper` along with other components, including the LOGIO core, Buffer core, Register Manager reference design, reference clocking module, and reset module. This has been designed for those who want to integrate a complete RapidIO Endpoint into their design.

An additional wrapper integrates the `rio_wrapper` with an example design to step you through a typical design implementation. The example design is used for testing and demonstration purposes in both simulation and hardware environments.

Logical Layer

The Serial RapidIO Logical (I/O) and Transport Interface (Logical Layer) high-level block diagram is shown in Figure 2. The Logical Layer is used in conjunction with the Serial RapidIO Physical Layer to build the Serial RapidIO Endpoint solution. The Logical Layer interfaces to the Physical Layer using the LocalLink Interface, which is a Xilinx proprietary bus interface. The LocalLink Interface consists of two unidirectional data buses with separate control signals for each direction.

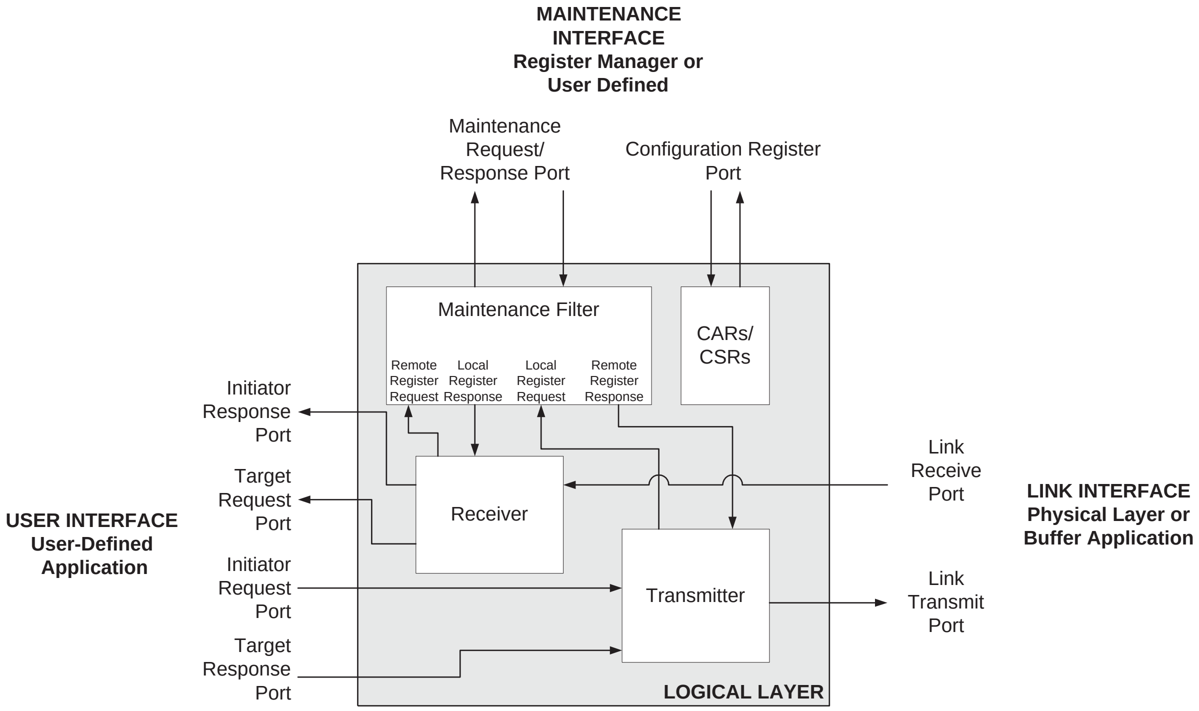

Figure 2: **RapidIO Logical (I/O) and Transport Interface Block Diagram**

The Logical and Transport interface operates at line rate. Full endpoint throughput will depend upon the buffering scheme used. The reduced internal clock rate, flexible user application interface, and combined support for many different RapidIO features provides a solution designed for use in high-performance applications.

Attaining maximum bandwidth depends on several factors, including availability of data and the ability of other devices to keep pace with your data stream. Performance for a point-to-point interface (such as RapidIO) does not depend on the volume of other traffic on a bus.

Functional Description

The Logical Layer is partitioned into several modules that control the concatenation and parsing of transmit and receive packets. It has three interfaces: User, Link, and Maintenance. The User Interface contains four ports that can be used to source or consume a packet intended for, or received from a remote endpoint. Local configuration Read and Write transactions can also be initiated from this interface to the configuration registers of the endpoint.

Transmit packets are input using either the Initiator Request, Target Response, or Maintenance Ports. They are then output by the Logical Layer interface to the Link Transmit port (except in the case of local configuration read/write accesses). Local configuration register accesses are output to the Maintenance port.

Receive packets are output to the user interface on either the Initiator Response, Target Request, or Maintenance port. Table 2 lists the various packet Ftypes supported by the Logical Layer interface.

Table 2: **Supported Ftypes by the Logical (I/O) and Transport Layer Interface**

Ftype	Transaction Type	Specification	Supported
0000	User Defined	User	Yes[1]
0001	Reserved	-	Yes[1]
0010	Atomic, Nread	Logical	Yes
0011	Reserved	-	Yes[1]
0100	Reserved	-	Yes[1]
0101	Atomic, Nwrite, Nwrite_R	Logical	Yes
0110	Swrite	Logical	Yes
0111	Reserved	-	Yes[1]
1000	Maintenance	Logical and Message Passing	Yes
1001	Reserved	-	Yes[1]
1010	Doorbell	Message Passing	Yes
1011	Message	Message Passing	Yes
1100	Reserved	-	Yes[1]
1101	Response	Logical and Message Passing	Yes
1110	Reserved	-	Yes[1]
1111	User Defined	User	Yes[1]

[1] Any unrecognized packet is sent to the User Interface. The Logical Layer interface facilitates any user-defined ftype or user-implemented Message Passing.

The Logical Layer Interface contains two ports: Receive and Transmit. It is designed to be connected with the Serial RapidIO Buffer LogiCORE IP module.

The Maintenance Interface contains two ports: Maintenance Request/Response, and Configuration Register. These ports control reads and writes to the configuration registers that reside in the Logical Layer, as well as any configuration registers that are user-defined or that belong to the Physical Layer.

The Serial RapidIO Endpoint example design provides a Register Manager reference design. The Register Manager is a typical application that interfaces to the Maintenance Request/Response Port and Configuration Register Port of the Logical Layer interface.

Logical (I/O) and Transport Interfaces

User (Logical Layer) Interface

The User Interface contains four ports that can be configured to issue a packet intended for a remote device or to consume packets issued by a remote device. It also initiates local configuration read and write accesses from these ports to the configuration registers that reside in this RapidIO Endpoint device. A sample transaction is shown in Figure 3 and described in Table 3.

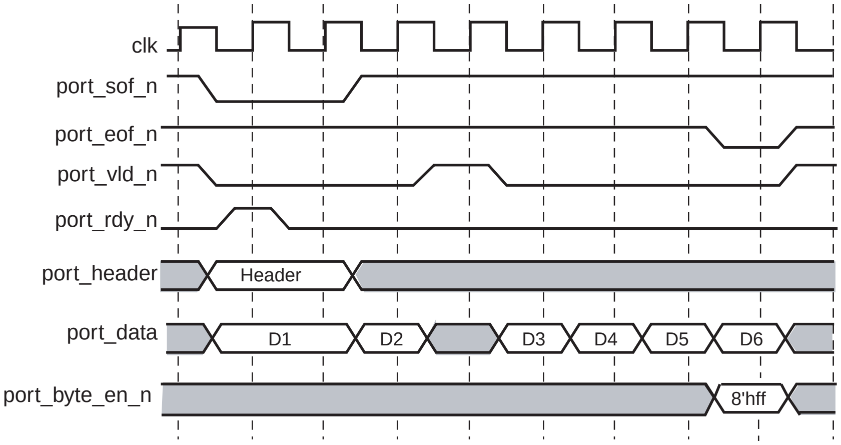

Figure 3: **User Logical Layer Interface**

Table 3: **User Interface Sample Transaction Cycles**

Cycle	Description
1	The Source side indicates a valid start of frame by asserting port_sof_n in conjunction with port_vld_n. In this example, the destination device deasserts port_rdy_n indicating a stall cycle is necessary. This deassertion invalidates this cycle.
2	The destination asserts port_rdy_n indicating it is ready for a transfer. The combination of port_rdy_n and port_vld_n assertion marks this as a valid data cycle. port_sof_n assertion in a valid cycle not only marks a new packet, it also validates the port_header information.
3	Deassertion of port_sof_n, but continued assertion of port_vld_n and port_rdy_n, mark this as a valid data transfer.
4	port_vld_n is deasserted. Indicates the Source needs a stall. Cycle is invalidated.
5	Re-assertion of port_vld_n marks valid data, and combined with the continued assertion of port_rdy_n, validates the data transfer.
6	Valid data transfer.
7	Continued data transfer.
8	Assertion of port_eof_n marks this frame as the final beat, and validates port_byte_en.
9	Deassertion of port_eof_n completes the packet transfer protocol. Deassertion of port_vld_n indicates there is no data to transfer.

Buffer

The Serial RapidIO Buffer LogiCORE IP module has been designed to provide for trade-offs between system performance and resource usage. The Transmit and Receiver buffer sizes can be configured separately, which allows you to place resources where throughput is expected to be most critical. The Buffer core also allows two flow control modes. RX Flow Control uses fewer resources at the cost of retrying packets if the link partner is full. TX Flow Control tries to only send packets when the link partner has space. This can increase throughput by reducing the number of retries at the cost of additional logic. Understanding how packet sizes, buffer sizes, and flow control work together allows you to make intelligent decisions to optimize throughput while considering resource costs.

The Buffer core handles all packet rewind scenarios from the PHY core, including packet retries and error recovery. It helps guarantee packet delivery by retaining sent packets until a proper acknowledgement has been received and verified by the PHY layer.

In compliance with the *RapidIO Interconnect v2.1* standard, the Buffer prevents deadlock scenarios. It does so by providing a *response only* signal back to the Logical Layer, stalling transmission of request packets. This frees a path for Response packets to help alleviate feedback paths from the receive buffer. The buffer also implements priority-based packet reordering and re-prioritizing of response packets. This helps to hasten response acceptance and to streamline packet transmission during peak traffic times.

Physical Layer

The Serial RapidIO Physical Layer interface provides two configuration modes: single lane (1x) and quad-lane (4x). The 1x Physical Layer can minimize the amount of logic resources needed when an application requires low data bandwidth. The 4x Physical Layer core requires more logic resources, but provides higher bandwidth and better reliability, as it can also operate in the 1x mode.

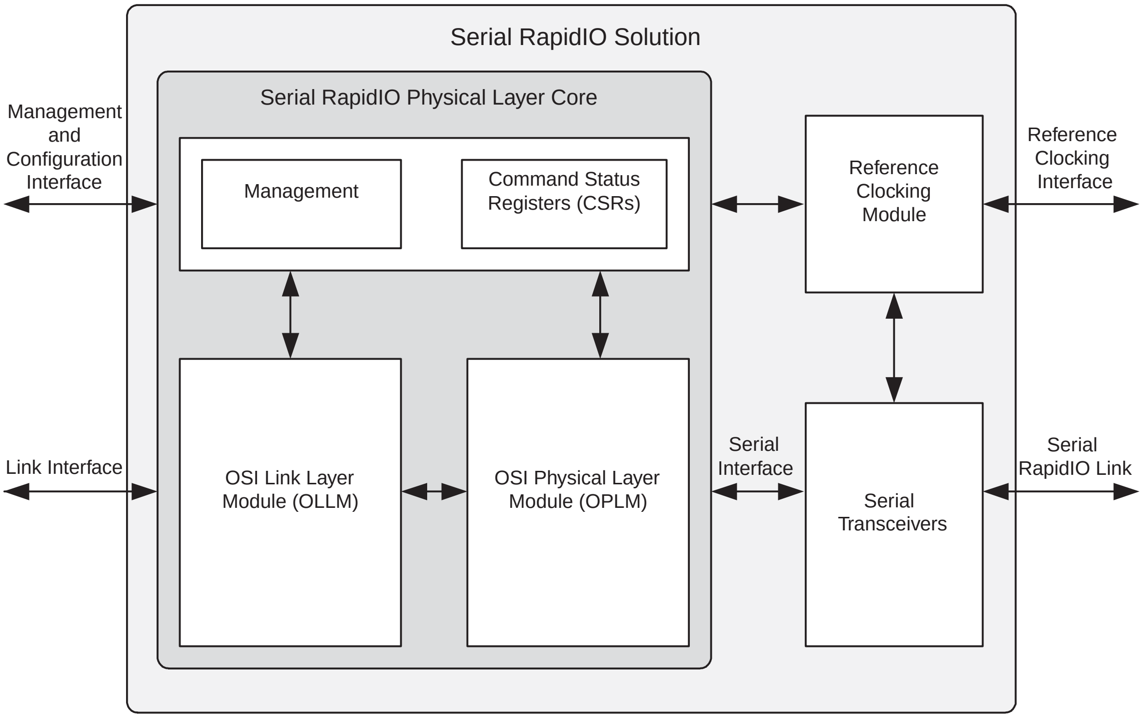
Serial RapidIO Solution
Serial RapidIO Physical Layer Core
Management and Configuration Interface
Management
Command Status Registers (CSRs)
Reference Clocking Module
Reference Clocking Interface
Link Interface
OSI Link Layer Module (OLLM)
OSI Physical Layer Module (OPLM)
Serial Interface
Serial Transceivers
Serial RapidIO Link

Figure 4: **Serial RapidIO Physical Layer**

The Virtex-6, Spartan®-6, Virtex-5, and Virtex-4 families of FPGAs enable the design of fully RapidIO compliant systems. The FPGA devices meet the required electrical and timing parameters for all four supported baud rates, 1.25, 2.5, 3.125, and 5.0 Gbps, as outlined in the Serial RapidIO AC electrical specification.

Functional Description

The Serial RapidIO Physical Layer core, transceivers, and Reference Clocking Module interface with the RapidIO link and user logic using the following interfaces.

- Serial RapidIO Interface
- Transceiver Interface
- System Interface
- Management and Configuration Interface
- Link Interface

The Serial RapidIO PHY connects to the Buffer using two local link interfaces, one for transmission and one for reception. The buffer interfaces into the Link Layer (OLLM) within the RapidIO PHY core. The OLLM is responsible for CRC generation and verification, symbol generation and decoding, packet exchange protocol handshake, and buffer management. This module is subdivided into two main modules handling the transmit and receive direction of data.

- Transmit Module

  The OLLM Transmit module generates packet headers and transmits packets from the user application interface to the OPLM block. The OLLM Transmit module also generates the early and final CRC for data packets, the CRC for control symbols, and generates and inserts control symbols for link management in to the data stream.
- Receive Module

  The OLLM Receive module detects and decodes incoming control symbols, removes packet headers, and transmits packets from the OPLM to the user application interface. The OLLM Receive module also checks intermediate and final CRC values in the data packet, CRC values in the control symbol and initiates error recovery protocol when the link enters an error condition.

As the packet and control symbols are formed, they move through the OPLM. The OPLM performs serialization and deserialization, link initialization, and training. The core OPLM implements the PCS layer logic, while the transceivers handle PMA layer functionality. The transceivers are provided outside the core for increased flexibility.

This module is subdivided into the following two modules:

- **Physical Coding Sublayer (PCS)**

  The function of the PCS block is to format and re-assemble the data packets and control symbols as they are transmitted and received from the PMA block. The PCS block ensures that the correct sequence of characters are transmitted and received to and from the PMA block in accordance with the RapidIO Serial protocol.
- **Physical Media Attach (PMA)**

  The PMA block performs 8b/10b encoding and decoding function, serialization and deserialization of data, transmit and receive clock generation, recovery clock correction logic, and transmit and receive buffering. This functionality is implemented within the Xilinx Multi-Gigabit Transceivers.

Management Interface

The Management interface provides accessibility to the Physical Layer Command and Status Registers (CSRs). The Physical Layer configuration registers provide information about core configuration and link status, as described in the *Serial RapidIO Interconnect Specification v2.1*.

Reference Clocking Module

The Reference Clocking module provides the input clocks required to operate the core. The module takes the input system clock and generates the appropriate clock to the multi-gigabit transceiver and the internal data path.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Logical Layer (DO-DI-RIO-LOG) and the Physical Layer (DO-DI-RIO-PHY) IP cores are provided under the SignOnce IP Site License. The pre-implemented netlist configurable Buffer core is delivered as part of the Physical Layer core. The Xilinx RapidIO cores can be generated using the Xilinx CORE Generator™ system. The CORE Generator system is shipped with Xilinx ISE Foundation™ Series Development software.

Simulation evaluation licenses for the cores are shipped with the CORE Generator system. To access the full functionality of the cores, including FPGA bitstream generation, full licenses must be obtained from Xilinx. For more information, please visit the Serial RapidIO Physical Layer product page, or the Logical Layer product page.

Please contact your local Xilinx sales representative for pricing of this and additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/19/08	1.1	Initial Xilinx release.
04/24/09	1.5	Updated Xilinx tools to ISE 11.1, simulator requirements, removed support for legacy Virtex-II Pro FPGA devices, added support for Virtex-6 FPGA devices.
06/24/09	1.6	Updated Xilinx tools to ISE 11.2.
09/16/09	2.0	Updated core to v5.4 and Xilinx tools to ISE v11.3.
04/19/10	3.0	Updated core to v5.5 and ISE to v12.1.
03/01/11	4.0	Updated core to v5.6 and ISE to v13.1.

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