LogiCORE IP Spartan-6 FPGA Integrated Endpoint Block v1.4 for PCI Express

DS718 September 21, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Spartan®-6 FPGA Integrated Endpoint Block for PCI Express® core is a high-bandwidth, scalable, and reliable serial interconnect building block for use with Spartan-6 FPGA devices. The Spartan-6 FPGA Integrated Endpoint Block for PCI Express (PCIe®) solution supports a 1-lane configuration that is protocol-compliant and electrically compatible with the *PCI Express Base Specification v1.1*.

PCI Express offers a serial architecture that alleviates many of the limitations of parallel bus architectures by using clock data recovery (CDR) and differential signaling. Using CDR (as opposed to source synchronous clocking) lowers pin count, enables superior frequency scalability, and makes data synchronization easier. The layered architecture of PCI Express provides for future attachment to copper, optical, or emerging physical signaling media. PCI Express technology, adopted by the PCI-SIG as the next generation PCI, is backward-compatible to the existing PCI software model.

With higher bandwidth per pin, low overhead, low latency, reduced signal integrity issues, and CDR architecture, the Integrated Endpoint Block sets the industry standard for a high-performance, cost-efficient third-generation I/O solution.

The Integrated Endpoint Block solution is compatible with industry-standard application form factors such as the *PCI Express Card Electromechanical (CEM) v1.1* and the *PCI Industrial Computer Manufacturers Group (PICMG) 3.4* specifications.

This core is defined in the following table.

Product Name	1-lane Integrated Endpoint Block
FPGA Architecture	Spartan-6
User Interface Width	32
Lane Widths Supported	x1
Link Speeds Supported	2.5 GT/s
PCIe Base Specification Compliance	v1.1

LogiCORE IP Facts			
Core Specifics			
Supported FPGA Device Families(1)	Spartan-6(2)		
Min. Device Requirements	XC6SLX25T-CSG324-2		
Resources Used	**GTP**	**LUT(3)**	**FF(3)**
	1(4)	3	0
	Block RAM	**CMPS(5) # Tx Buffers**	**CMPS**
	2-18	30(6)	512
Special Features	GTP Transceivers Spartan-6 FPGA Integrated Block for PCI Express Phased Lock Loop Block RAM		
Provided with Core			
Documentation	Product Specification, User Guide, Instantiation Template		
Design Files	Verilog and VHDL Unencrypted RTL source files for Simulation and Synthesis, Verilog and VHDL Test Bench, Verilog and VHDL Example Design		
Constraints File	User Constraints File (UCF)		
Design Tool Support			
HDL Synthesis Tool	Synplicity® Synplify®, Xilinx XST		
Implementation Tools	Xilinx ISE® v12.3		
Simulation Tools(7)	Cadence Incisive Enterprise Simulator (IES) v9.2 Synopsys VCS and VCS MX 2009.12 Mentor Graphics ModelSim v6.5c Xilinx ISim 12.1		
Support			
Provided by Xilinx, Inc. @ www.xilinx.com/support			

1. For the complete list of supported devices, see the release notes for this core.
2. Spartan-6 FPGA solutions require the latest production silicon stepping and are pending hardware validation; the LogiCORE IP warranty does not include production usage with engineering sample silicon (ES).
3. Numbers are for the default core configuration; actual LUT and FF utilization values vary based on specific configurations.
4. In Spartan-6 devices, 1-lane core uses only 1 GTP Transceiver of a GTP tile which has 2 GTP transceivers. It is possible to use the other GTP transceiver for user designs, with some limitations. See UG386, *Spartan-6 GTP Transceiver User Guide*.
5. Capability Maximum Payload Size (CMPS).
6. Supports 30 TLPs at CMPS (512 bytes payload): No restrictions.
   - Supports 29 TLPs at 256 bytes payload: No restrictions.
   - Supports 27 TLPs at 128 bytes payload or less: No restrictions.
7. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator.

Features

- High-performance, highly flexible, scalable, and reliable, general purpose I/O core
  - Compliant with the *PCI Express Base Specification v1.1*
  - Compatible with conventional PCI software model
- Incorporates Xilinx Smart-IP™ technology to guarantee critical timing
- Uses GTP transceivers for Spartan-6 LXT
  - 2.5 Gbps line speed
  - Supports 1-lane operation
  - Elastic buffers and clock compensation
  - Automatic clock data recovery
- 8b/10b encode and decode
- Supports Lane Polarity Inversion per PCI Express specification requirements
- Standardized user interface
  - Easy-to-use packet-based protocol
  - Full-duplex communication
  - Back-to-back transactions enable greater link bandwidth utilization
  - Transmit streaming, cut-through mode on TX interface for decreased latency
  - Supports flow control of data and discontinuation of an in-process transaction in transmit direction
  - Supports flow control of data in receive direction
- Supports removal of corrupted packets for error detection and recovery
- Compliant with PCI/PCI Express power management functions
- Supports a maximum transaction payload of up to 512 bytes
- Supports Multi-Vector MSI for up to 32 vectors
- Fully compliant with PCI Express transaction ordering rules

Applications

The Spartan-6 FPGA Integrated Endpoint Block for PCI Express architecture enables a broad range of computing and communications target applications, emphasizing performance, cost, scalability, feature extensibility and mission-critical reliability. Typical applications include

- Data communications networks
- Telecommunications networks
- Broadband wired and wireless applications
- Cross-connects
- Network interface cards
- Chip-to-chip and backplane interconnect
- Crossbar switches
- Wireless base stations

Functional Description

For information about the internal architecture of the Spartan-6 FPGA Endpoint block, see UG654, *Spartan-6 FPGA Integrated Endpoint Block for PCI Express User Guide*. Figure 1 illustrates the interfaces to the core.

- System (SYS) interface
- PCI Express (PCI EXP) interface
- Configuration (CFG) interface
- Transaction (TRN) interface

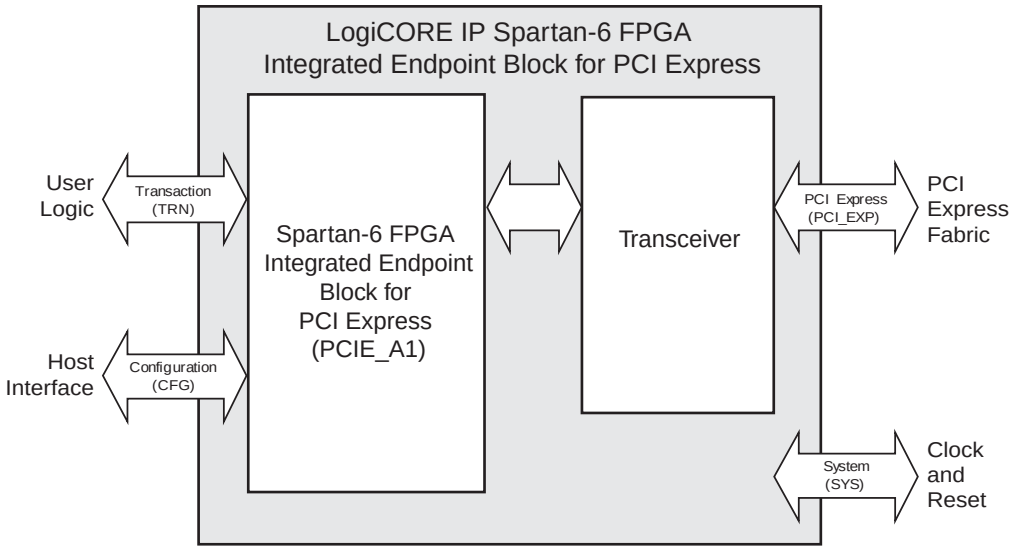

Figure 1: **Integrated Endpoint Block for PCI Express Top-level Functional Blocks and Interfaces**

Protocol Layers

The Integrated Endpoint Block follows the *PCI Express Base Specification* layering model, which consists of the Physical, Data Link, and Transaction Layers. The protocol uses packets to exchange information between layers. Packets are formed in the Transaction and Data Link Layers to carry information from the transmitting component to the receiving component. Necessary information is added to the packet being transmitted, which is required to handle the packet at specific layers.

At the receiving end, each layer of the receiving element processes the incoming packet, strips the relevant information and forwards the packet to the next layer. As a result, the received packets are transformed from their Physical Layer representation to their Data Link Layer representation and Transaction Layer representation.

The functions of the protocol layers include:

- Generating and processing of TLPs
- Flow-control management
- Initialization and power management functions
- Data protection
- Error checking and retry functions
- Physical link interface initialization

- Maintenance and status tracking
- Serialization, de-serialization and other circuitry for interface operation

Each of the protocol layers are defined in the sections that follow.

Physical Layer

The Physical Layer exchanges information with the Data Link Layer in an implementation-specific format. This layer is responsible for converting information received from the Data Link Layer into an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

Data Link Layer

The Data Link Layer acts as an intermediate stage between the Transaction Layer and the Physical Layer. Its primary responsibility is to provide a reliable mechanism for the exchange of Transaction Layer Packets (TLPs) between the two Components on a Link.

Services provided by the Data Link Layer include data exchange (TLPs), error detection and recovery, initialization services and the generation and consumption of Data Link Layer Packets (DLLPs). DLLPs are the mechanism used to transfer information between Data Link Layers of two directly connected components on the Link. DLLPs are used for conveying information such as Flow Control and TLP acknowledgments.

Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The primary function of the Transaction Layer is the assembly and disassembly of Transaction Layer Packets (TLPs). Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. TLPs are used to communicate transactions, such as read and write, as well as certain types of events. To maximize the efficiency of communication between devices, the Transaction Layer implements a pipelined, full split-transaction protocol and manages credit-based flow control of TLPs.

Configuration Management

The Configuration Management Layer supports generation and reception of System Management Messages by communicating with the other layers and the user application. This layer contains the device configuration space and other system functions. The Configuration layer implements PCI/PCI-Express power management capabilities, and facilitates exchange of power management messages, including support for PME event generation. Also implemented are user-triggered error message generation, and user-read access to the device configuration space.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Spartan-6 FPGA Integrated Block for PCI Express is included with the ISE CORE Generator™.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/09	1.0	Initial Xilinx draft.
09/16/09	2.0	Updated core to v1.2 and ISE to v11.3. Added support for VHDL.
12/02/09	2.5	Updated to support ISE v11.4.
04/19/10	3.0	Updated core to v1.3 and ISE to v12.1. Removed licensing information (a license is no longer required).
09/21/10	4.0	Updated core to v1.4 and ISE to v12.3.

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