LogiCORE IP RXAUI v4.0

Product Guide for Vivado Design Suite

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Introduction

The LogiCORE™ IP RXAUI core is a high-performance, low pin count 10 Gb/s interface intended to allow physical separation between the data-link layer and physical layer devices in a 10 Gb/s Ethernet system.

The RXAUI core implements a single-speed full-duplex 10 Gb/s Ethernet Reduced Pin eXtended Attachment Unit Interface (RXAUI) solution for Xilinx 7 series FPGAs that comply with Dune Networks specifications.

The 7 series FPGAs in combination with the RXAUI core, enable the design of RXAUI-based interconnects whether they are chip-to-chip, over backplanes, or connected to 10 Gb/s optical modules.

Features

- Designed to Dune Networks specifications
- Uses two transceivers at 6.25 Gb/s line rate to achieve 10 Gb/s data rate
- Implements DTE XGXS, PHY XGXS, and 10GBASE-X PCS in a single encrypted HDL
- *IEEE 802.3-2008* clause 45 MDIO interface (optional)
- Available under the Xilinx End User License Agreement

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq®-7000, Virtex®-7, Kintex®-7, Artix®-7
Supported User Interfaces	XGMII, MDIO
Resources	See Table 2-1 and Table 2-3.
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog/VHDL
Test Bench	Verilog/VHDL
Constraints File	XDC
Simulation Model	VHDL/Verilog
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The RXAUI standard was developed as a means to improve the 10-Gigabit Ethernet port density. The number of XAUI interfaces that could be implemented was limited by the number of available transceivers, with capacity and performance still to be utilized. RXAUI halves the number of transceivers required compared with a XAUI implementation.

RXAUI is a two-lane, 6.25 Gb/s-per-lane serial interface. It is intended to work with an existing XAUI implementation and multiplexes/demultiplexes the two physical RXAUI lanes into four logical XAUI lanes. Each RXAUI lane is a differential pair carrying current mode logic (CML) signaling, and the data on each lane is 8B/10B encoded before transmission.

In this document:

- Virtex®-7 and Kintex®-7 FPGAs GTX transceivers are abbreviated to GTX transceivers.
- Virtex-7 FPGA GTH transceiver is abbreviated to GTH transceiver.
- Artix®-7 FPGA GTP transceiver is abbreviated to GTP transceiver.

Feature Summary

The RXAUI core can be configured in the following mode for Dune Networks. This RXAUI implementation maintains 8B/10B disparity on the RXAUI physical lane. The Dune Networks RXAUI standard is fully specified in DN-DS-RXAUI-Spec v.1.0.

For the management interface, the RXAUI core can be customized with either a two-wire low-speed serial MDIO interface, or a configuration and status vector interface.

Applications

The applications of RXAUI have extended beyond 10-Gigabit Ethernet to the backplane and other general high-speed interconnect applications. A typical backplane application is shown in Figure 1-1.

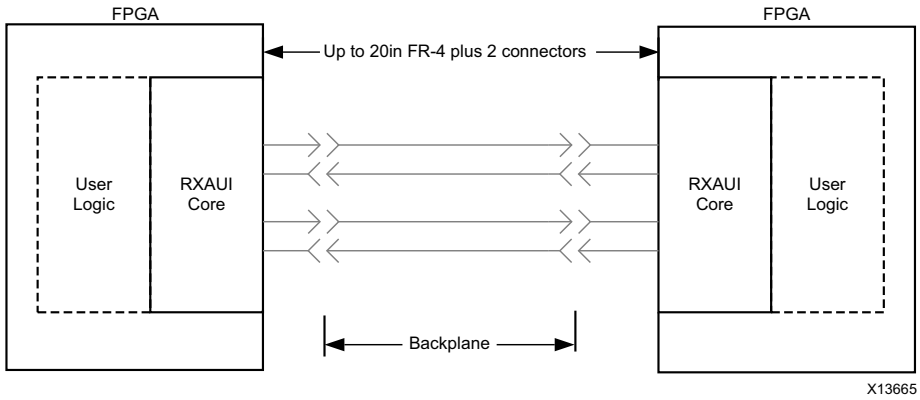

Figure 1-1: **Typical Backplane Application for RXAUI**

Functional Description

Figure 1-2 shows a block diagram of the Dune Networks RXAUI core implementation. The major functional blocks of the core include the following:

- **Transmit Idle Generation Logic** – Creates the code groups to allow synchronization and alignment at the receiver.
- **Demux Logic** – Separates the two physical RXAUI lanes into four logical XAUI lanes.
- **Synchronization State Machine (one per lane)** – Identifies byte boundaries in incoming serial data.
- **Deskew State Machine** – Deskews the four received lanes into alignment.
- **Optional MDIO Interface** – A two-wire low-speed serial interface used to manage the core.
- **Embedded Transceivers** – Provide high-speed transceivers as well as 8B/10B encode and decode, and elastic buffering in the receive datapath.

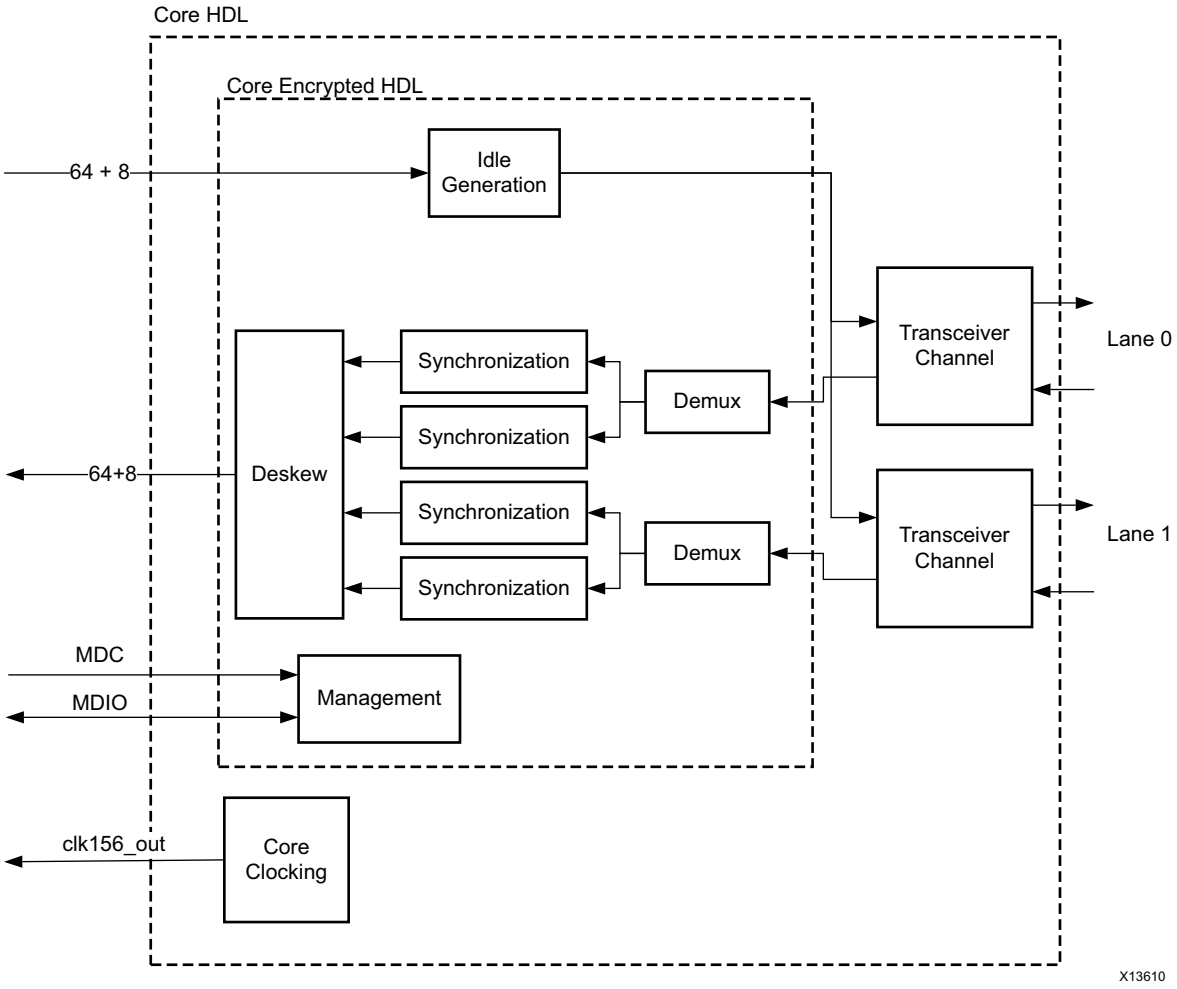

Figure 1-2: **Implementation of Dune Networks RXAUI Core**

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards

The LogiCORE™ IP RXAUI core is designed to the Dune Networks [Ref 1] specifications.

Performance

Latency

These measurements are for the core only — they do not include the latency through the transceiver. The latency through the transceiver can be obtained from the relevant user guide.

Transmit Path Latency

As measured from the input port `xgmii_txd[63:0]` of the transmitter side XGMII (until that data appears on `mgt_txdata[63:0]` on the internal transceiver interface), the latency through the core for the internal XGMII interface configuration in the transmit direction is 4 clock periods of the core input `usrclk` for Dune Networks mode.

Receive Path Latency

Measured from the transceiver output pins `RXDATA[63:0]` until the data appears on `xgmii_rxdata[63:0]` of the receiver side XGMII interface, the latency through the core in the receive direction for Dune Networks mode is equal to six to eight clock cycles of `usrclk`. The latency depends on comma alignment position and data positioning within the transceiver 4-byte interface.

Resource Utilization

Table 2-1 provides approximate utilization for the various core options on Virtex®-7 and Kintex®-7 FPGAs using the Vivado® Design Suite.

Table 2-1: **Device Utilization – Virtex-7 (GTX), Kintex-7, and Zynq®-7000 Devices**

Shared Logic	MDIO Management	LUTs	FFs
In Example Design	FALSE	779	1007
In Example Design	TRUE	919	1110
In Core	FALSE	866	1012
In Core	TRUE	1013	1120

Table 2-2 provides approximate utilization for the various core options on Virtex-7 (GTH) FPGAs using the Vivado Design Suite.

Table 2-2: **Device Utilization – Virtex-7 (GTH) FPGAs**

Shared Logic	MDIO Management	LUTs	FFs
In Example Design	FALSE	773	1002
In Example Design	TRUE	918	1115
In Core	FALSE	855	1017
In Core	TRUE	1021	1125

Table 2-3 provides approximate utilization for the various core options on Artix®-7 FPGAs using the Vivado Design Suite.

Table 2-3: **Device Utilization – Artix-7 FPGAs**

Shared Logic	MDIO Management	LUTs	FFs
In Example Design	FALSE	916	1157
In Example Design	TRUE	1080	1258
In Core	FALSE	1010	1167
In Core	TRUE	1174	1268

Port Descriptions

Client-Side Interface

The signals of the client-side interface are shown in Table 2-4. See Protocol Description for details on connecting to the client-side interface.

Table 2-4: **Client-Side Interface Ports**

Signal Name	Direction	Description
xgmii_txd[63:0]	In	Transmit data, 8 bytes wide
xgmii_txc[7:0]	In	Transmit control bits, 1-bit per transmit data byte
xgmii_rxd[63:0]	Out	Received data, 8 bytes wide
xgmii_rxc[7:0]	Out	Receive control bits, 1-bit per received data byte

Transceiver Interface

The following signals are directly connected to the transceiver instance.

Table 2-5: **Transceiver Interface Ports**

Signal Name	Direction	Description
rxaui_tx_l0_p, rxaui_tx_l0_n, rxaui_tx_l1_p, rxaui_tx_l1_n	Out	Differential complements of one another forming a differential transmit output pair. One pair for each of the 2 lanes.
rxaui_rx_l0_p, rxaui_rx_l0_n, rxaui_rx_l1_p, rxaui_rx_l1_n	In	Differential complements of one another forming a differential receiver input pair. One pair for each of the 2 lanes.
signal_detect[1:0]	In	Intended to be driven by an attached optical module; they signify that each of the two optical receivers is receiving illumination and is therefore not just putting out noise. If an optical module is not in use, this 2-wire bus should be tied to 0x3.

MDIO Ports

The RXAUI core, when generated with an MDIO interface, implements an MDIO Interface Register block. The core responds to MDIO transactions as either a 10GBASE-X PCS, a DTE XS, or a PHY XS depending on the setting of the `type_sel` port (see Table 3-3). The MDIO Interface Ports are described in Table 2-6. More information about using this interface can be found in MDIO Interface.

Table 2-6: **MDIO Management Interface Ports**

Signal Name	Direction	Description
mdc	In	Management clock
mdio_in	In	MDIO input
mdio_out	Out	MDIO output
mdio_tri	Out	MDIO 3-state. 1 disconnects the output driver from the MDIO bus.
type_sel[1:0]	In	Type select
prtad[4:0]	In	MDIO port address

Configuration and Status Signals

The Configuration and Status Signals are shown in Table 2-57. See Configuration and Status Vectors for details on these signals, including a breakdown of the configuration and status vectors.

Table 2-7: **Configuration and Status Ports**

Signal Name	Direction	Description
configuration_ vector[6:0]	In	Configuration information for the core.
status_vector[7:0]	Out	Status information from the core.

Clocking and Reset Signals and Module

Included in the example design sources are circuits for clock and reset management. For the RXAUI core these comprise the Transceiver Quad PLL and associated reset logic. Tables 2-8 to 2-12 shows the ports on the core that are associated with system clocks and resets.

Table 2-8: **Clocking and Reset Ports**

Signal Name	Direction	Description
clk156_out	Out	156.25 MHz clock derived from TXOUTCLK. Can be used for external logic. Cannot be connected to another RXAUI core.
clk156_lock	In	Indicates that clk156 is stable and ready for use.
dclk	In	Stable clock that is used in initialization logic for the transceivers and also connected to the DRPCLK port on the DRP interface of the transceiver.
reset	In	Asynchronous reset connected to the transceiver Channel PLL or Transceiver Quad PLL. This should be asserted if refclk or dclk is not valid.

Table 2-9: **GTX and GTH Clocking Ports - Shared Logic Included in Example Design**

Signal Name	Direction	Description
refclk	In	Transceiver reference clock. Must be driven from the appropriate transceiver differential clock buffer.
qplloutclk	In	Connect to the quad PLL output clock QPLLOUTCLK.
qplllock	In	Connect to the quad PLL lock output QPLLLOCK.
qplloutrefclk	In	Connect to the quad PLL output reference clock QPLLOUTREFCLK.
common_pll_reset	In	Connect to the reset to the QPLL reset.

Table 2-10: **GTP Clocking Ports - Shared Logic Included in Example Design**

Signal Name	Direction	Description
common_pll_reset	In	Connect to the reset to the GTPE2_COMMON PLL.
pll0outclk	In	Connect to the GTPE2_COMMON PLL port PLL0OUTCLK.

Table 2-10: **GTP Clocking Ports - Shared Logic Included in Example Design *(Cont'd)***

Signal Name	Direction	Description
pll0lock	In	Connect to the GTPE2_COMMON PLL lock port PLL0LOCK.
pll0outrefclk	In	Connect to the GTPE2_COMMON PLL REFCLK port PLL0OUTREFCLK.
pll1outclk	In	Connect to the GTPE2_COMMON PLL port PLL1OUTCLK.
pll1outrefclk	In	Connect to the GTPE2_COMMON PLL REFCLK port PLL1OUTREFCLK.

Table 2-11: **GTX and GTH Clocking Ports - Shared Logic Included in Core**

Signal Name	Direction	Description
refclk_p	In	Differential transceiver reference clock "p."
refclk_n	In	Differential transceiver reference clock "n."
refclk_out	Out	Reference clock output from the differential transceiver clock buffer.
qplloutclk_out	Out	Output from the quad PLL port QPLLOUTCLK.
qpllock_out	Out	Output from the quad PLL port QPLLLOCK.
qpllrefclk_out	Out	Output from the quad PLL port QPLLREFCLK.

Table 2-12: **GTP Clocking Ports - Shared Logic Included in Core**

Signal Name	Direction	Description
pll0outclk_out	Out	Output from the GTPE2_COMMON PLL port PLL0OUTCLK.
pll0lock_out	Out	Output from the GTPE2_COMMON PLL port PLL0LOCK.
pll0outrefclk_out	Out	Output from the GTPE2_COMMON PLL port PLL0OUTREFCLK.
pll1outclk_out	Out	Output from the GTPE2_COMMON PLL port PLL1OUTCLK
pll1outrefclk_out	Out	Output from the GTPE2_COMMON PLL port PLL1OUTREFCLK

Transceiver Interface

The transceiver interface is present if the "Additional Transceiver Control and Status Ports" option is selected. There are a number of ports that are directly connected to the transceivers. For a complete description of these signals, see the appropriate transceiver user guide (*7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 2] and *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 3]). Ports are prefixed with GT0 for Transceiver 0 and GT1 for Transceiver 1.

Table 2-13: **Transceiver Ports**

Signal Name	Direction
rxprbscntreset_in	In
rxprbssel_in [2:0]	In
txprbssel_in [2:0]	In
txdiffctrl_in [3:0]	In
txpostcursor_in [4:0]	In
txprecursor_in [4:0]	In (GTH & GTH)
rxdfelpmreset_in	In (GTH & GTH)
rxmonitorsel	In (GTH & GTH)
rxmonitorout	Out (GTH & GTH)
rxlpmreset_in	In (GTP)
rxlpmhfhold_in	In (GTP)
rxlpmlfhold_in	In (GTP)
rxlpmhfovrden_in	In (GTP)
rxlpmlfovrden_in	In (GTP)
rxpolarity_in	In
txpolarity_in	In
loopack_in[2:0]	In(1)
rxrate_in [2:0]	In
eyescantrigger_in	In
eyescanreset_in	In
eyescandataerror_out	Out
rxdisperr_out[3:0]	Out
rxnotintable_out[3:0]	Out
rxresetdone_out	Out
txresetdone_out	Out
drpaddr [8:0]	In
drpen	In
drpdi [15:0]	In

Table 2-13: **Transceiver Ports *(Cont'd)***

Signal Name	Direction
drpdo [15:0]	Out
drprdy	Out
drpwe	In
drp_busy	Out (GTP)

1. The Actual GT Loopback can be set by the external gt_control port input OR the XAUI Loopback bit (set by either the MDIO register or configuration vector). You should not drive both the XAUI Loopback and gt_control ports simultaneously.

Debug Interface

A debug port is provided that contains easy access to some of the important core signals.

Table 2-14: **Debug Ports**

Signal Name	Direction	Description
debug	Out	Debug Port Bit[5] = Align Status Bits[4:1] = Sync Status Bit[0] = TX Phase Align Complete

Register Space

This section describes the interfaces available for dynamically setting the configuration and obtaining the status of the RXAUI core. There are two interfaces for configuration; depending on the core customization, only one is available in a particular core instance. The interfaces are:

- MDIO Interface Registers
- Configuration and Status Vectors

In addition, there are output ports on the core signalling alignment and synchronization status. These ports are described in Alignment and Synchronization Status Ports.

MDIO Interface Registers

For a description of the MDIO Interface, see MDIO Interface.

10GBASE-X PCS/PMA Register Map

When the core is configured as a 10GBASE-X PCS/PMA, it occupies MDIO Device Addresses 1 and 3 in the MDIO register address map, as shown in Table 2-15.

Table 2-15: **10GBASE-X PCS/PMA MDIO Registers**

Register Address	Register Name
1.0	PMA/PMD Control 1
1.1	PMA/PMD Status 1
1.2,1.3	PMA/PMD Device Identifier
1.4	PMA/PMD Speed Ability
1.5, 1.6	PMA/PMD Devices in Package
1.7	10G PMA/PMD Control 2
1.8	10G PMA/PMD Status 2
1.9	Reserved
1.10	10G PMD Receive Signal OK
1.11 TO 1.13	Reserved
1.14, 1.15	PMA/PMD Package Identifier
1.16 to 1.65 535	Reserved
3.0	PCS Control 1
3.1	PCS Status 1
3.2, 3.3	PCS Device Identifier
3.4	PCS Speed Ability
3.5, 3.6	PCS Devices in Package
3.7	10G PCS Control 2
3.8	10G PCS Status 2
3.9 to 3.13	Reserved
3.14, 3.15	Package Identifier
3.16 to 3.23	Reserved
3.24	10GBASE-X PCS Status
3.25	10GBASE-X Test Control
3.26 to 3.65 535	Reserved

MDIO Register 1.0: PMA/PMD Control 1

Figure 2-1 shows the MDIO Register 1.0: PMA/PMD Control 1.

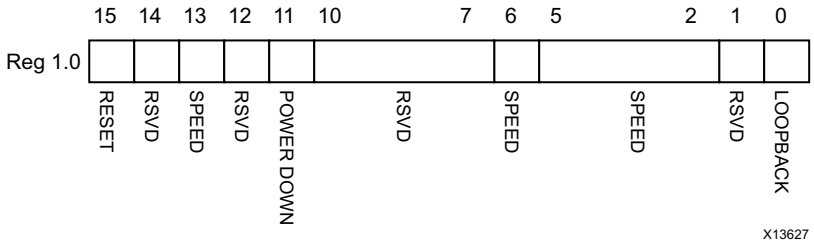

Figure 2-1: **PMA/PMD Control 1 Register**

Table 2-16 shows the PMA Control 1 register bit definitions.

Table 2-16: **PMA/PMD Control 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.0.15	Reset	0	R/W Self-clearing	0 = Normal operation 1 = Block reset The RXAUI block is reset when this bit is set to 1. It returns to 0 when the reset is complete. The soft_reset pin is connected to this bit. This can be connected to the reset of any other MMDs.
1.0.14	Reserved	0	R	The block always returns 0 for this bit and ignores writes.
1.0.13	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
1.0.12	Reserved	0	R	The block always returns 0 for this bit and ignores writes.
1.0.11	Power down	0	R/W	0 = Normal operation 1 = Power down mode When set to 1, the serial transceivers are placed in a low power state. Set to 0 to return to normal operation
1.0.10:7	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
1.0.6	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
1.0.5:2	Speed Selection	All 0s	R	The block always returns 0s for these bits and ignores writes.
1.0.1	Reserved	All 0s	R	The block always returns 0 for this bit and ignores writes
1.0.0	Loopback	0	R/W	0 = Disable loopback mode 1 = Enable loopback mode The RXAUI block loops the signal in the serial transceivers back into the receiver. Near-end PMA loopback is always used.

MDIO Register 1.1: PMA/PMD Status 1

Figure 2-2 shows the MDIO Register 1.1: PMA/PMD Status 1.

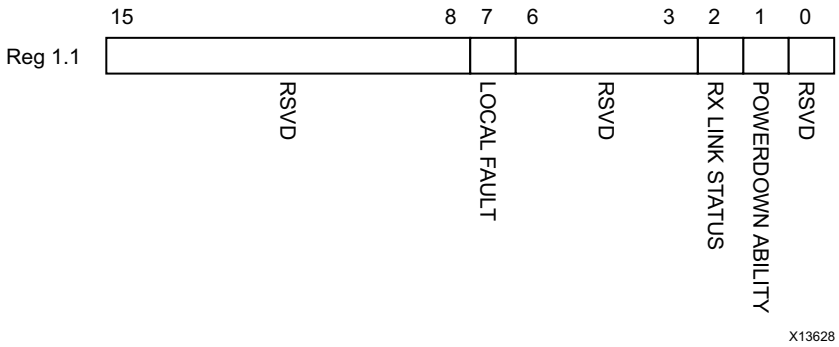

Figure 2-2: **PMA/PMD Status 1 Register**

Table 2-17 shows the PMA/PMD Status 1 register bit definitions.

Table 2-17: **PMA/PMD Status 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.1.15:8	Reserved	0	R	The block always returns 0 for this bit.
1.1.7	Local Fault	0	R	The block always returns 0 for this bit.
1.1.6:3	Reserved	0	R	The block always returns 0 for this bit.
1.1.2	Receive Link Status	1	R	The block always returns 1 for this bit.
1.1.1	Power Down Ability	1	R	The block always returns 1 for this bit.
1.1.0	Reserved	0	R	The block always returns 0 for this bit.

MDIO Registers 1.2 and 1.3: PMA/PMD Device Identifier

Figure 2-3 shows the MDIO Registers 1.2 and 1.3: PMA/PMD Device Identifier.

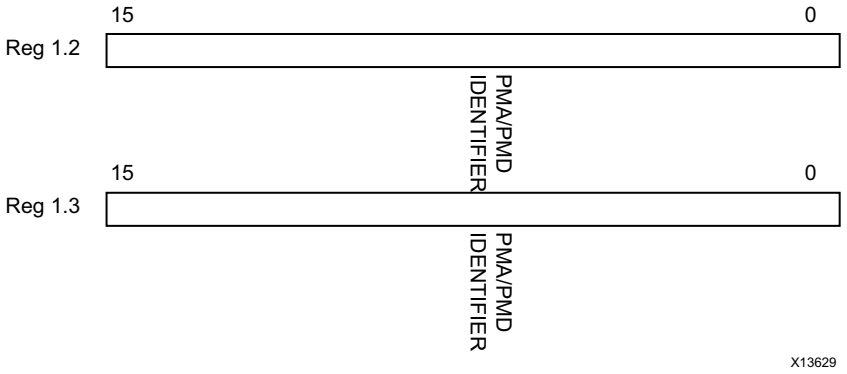

Figure 2-3: **PMA/PMD Device Identifier Registers**

Table 2-18 shows the PMA/PMD Device Identifier registers bit definitions.

Table 2-18: **PMA/PMD Device Identifier Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.2.15:0	PMA/PMD Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.
1.3.15:0	PMA/PMD Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.

MDIO Register 1.4: PMA/PMD Speed Ability

Figure 2-4 shows the MDIO Register 1.4: PMA/PMD Speed Ability.

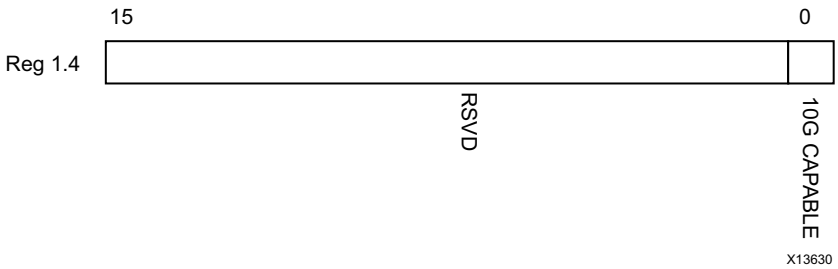

Figure 2-4: **PMA/PMD Speed Ability Register**

Table 2-19 shows the PMA/PMD Speed Ability register bit definitions.

Table 2-19: **PMA/PMD Speed Ability Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.4.15:1	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
1.4.0	10G Capable	1	R	The block always returns 1 for this bit and ignores writes.

MDIO Registers 1.5 and 1.6: PMA/PMD Devices in Package

Figure 2-5 shows the MDIO Registers 1.5 and 1.6: PMA/PMD Devices in Package.

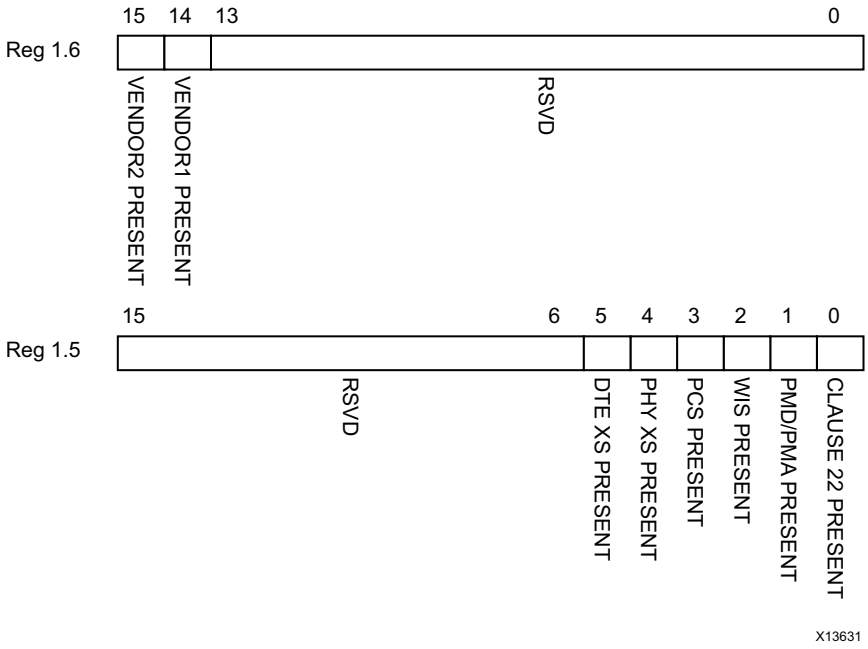

Figure 2-5: **PMA/PMD Devices in Package Registers**

Table 2-20 shows the PMA/PMD Device in Package registers bit definitions.

Table 2-20: **PMA/PMD Devices in Package Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.6.15	Vendor- specific Device 2 present	0	R	The block always returns 0 for this bit.
1.6.14	Vendor-specific Device 1 present	0	R	The block always returns 0 for this bit.
1.6.13:0	Reserved	All 0s	R	The block always returns 0 for these bits.
1.5.15:6	Reserved	All 0s	R	The block always returns 0 for these bits.
1.5.5	DTE XS present	0	R	The block always returns 0 for this bit.
1.5.4	PHY XS present	0	R	The block always returns 0 for this bit.
1.5.3	PCS present	1	R	The block always returns 1 for this bit.
1.5.2	WIS present	0	R	The block always returns 0 for this bit.
1.5.1	PMA/PMD present	1	R	The block always returns 1 for this bit.
1.5.0	Clause 22 Device present	0	R	The block always returns 0 for this bit.

MDIO Register 1.7: 10G PMA/PMD Control 2

Figure 2-6 shows the MDIO Register 1.7: 10G PMA/PMD Control 2.

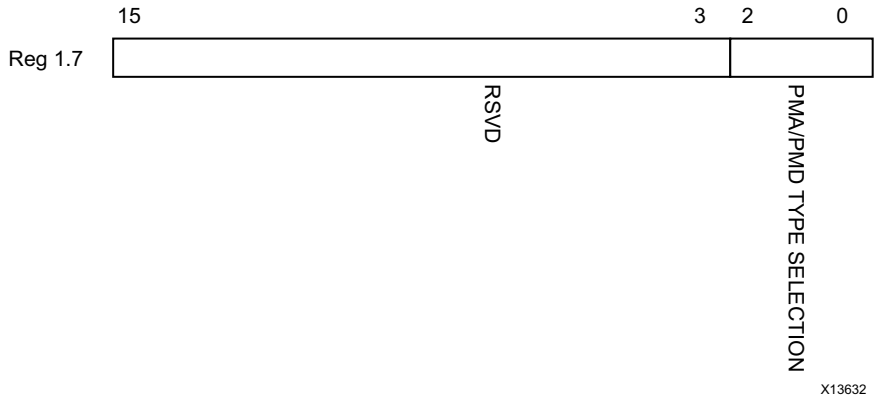

Figure 2-6: **10G PMA/PMD Control 2 Register**

Table 2-21 shows the PMA/PMD Control 2 register bit definitions.

Table 2-21: **10G PMA/PMD Control 2 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.7.15:3	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
1.7.2:0	PMA/PMD Type Selection	100	R	The block always returns 100 for these bits and ignores writes. This corresponds to the 10GBASE-X PMA/PMD.

MDIO Register 1.8: 10G PMA/PMD Status 2

Figure 2-7 shows the MDIO Register 1.8: 10G PMA/PMD Status 2.

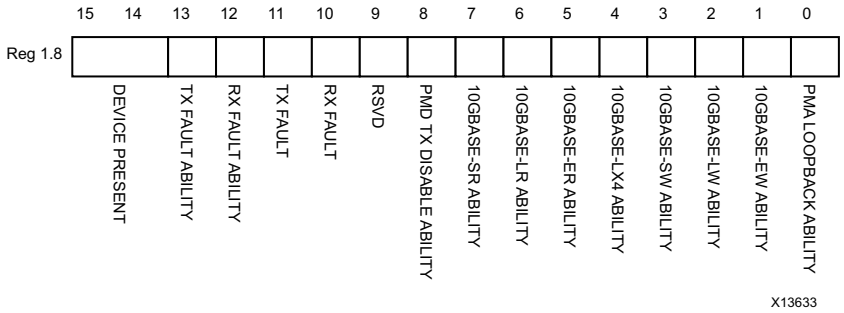

Figure 2-7: **10G PMA/PMD Status 2 Register**

Table 2-22 shows the PMA/PMD Status 2 register bit definitions.

Table 2-22: **10G PMA/PMD Status 2 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.8.15:14	Device present	10	R	The block always returns 10 for these bits.
1.8.13	Transmit Local Fault Ability	0	R	The block always returns 0 for this bit.
1.8.12	Receive Local Fault Ability	0	R	The block always returns 0 for this bit.
1.8.11	Transmit Fault	0	R	The block always returns 0 for this bit.
1.8.10	Receive Fault	0	R	The block always returns 0 for this bit.
1.8.9	Reserved	0	R	The block always returns 0 for this bit.
1.8.8	PMD Transmit Disable Ability	0	R	The block always returns 0 for this bit.
1.8.7	10GBASE-SR Ability	0	R	The block always returns 0 for this bit.
1.8.6	10GBASE-LR Ability	0	R	The block always returns 0 for this bit.
1.8.5	10GBASE-ER Ability	0	R	The block always returns 0 for this bit.
1.8.4	10GBASE-LX4 Ability	1	R	The block always returns 1 for this bit.
1.8.3	10GBASE-SW Ability	0	R	The block always returns 0 for this bit.
1.8.2	10GBASE-LW Ability	0	R	The block always returns 0 for this bit.
1.8.1	10GBASE-EW Ability	0	R	The block always returns 0 for this bit.
1.8.0	PMA Loopback Ability	1	R	The block always returns 1 for this bit.

MDIO Register 1.10: 10G PMD Signal Receive OK

Figure 2-8 shows the MDIO 1.10 Register: 10G PMD Signal Receive OK.

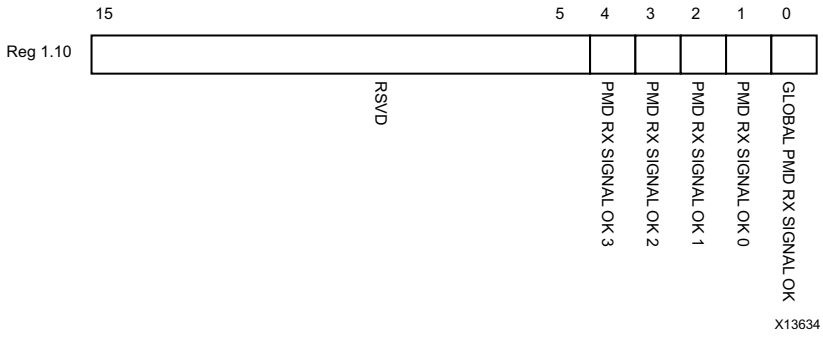

Figure 2-8: **10G PMD Signal Receive OK Register**

Table 2-23 shows the 10G PMD Signal Receive OK register bit definitions.

Table 2-23: **10G PMD Signal Receive OK Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.10.15:5	Reserved	All 0s	R	The block always returns 0s for these bits.
1.10.4	PMD Receive Signal OK 3	–	R	0 = Signal not OK on receive Lane 3 1 = Signal OK on receive Lane 3 This is the value of the SIGNAL_DETECT[1] port.
1.10.3	PMD Receive Signal OK 2	–	R	0 = Signal not OK on receive Lane 2 1 = Signal OK on receive Lane 2 This is the value of the SIGNAL_DETECT[1] port.
1.10.2	PMD Receive Signal OK 1	–	R	0 = Signal not OK on receive Lane 1 1 = Signal OK on receive Lane 1 This is the value of the SIGNAL_DETECT[0] port.
1.10.1	PMD Receive Signal OK 0	–	R	0 = Signal not OK on receive Lane 0 1 = Signal OK on receive Lane 0 This is the value of the SIGNAL_DETECT[0] port.
1.10.0	Global PMD Receive Signal OK	–	R	0 = Signal not OK on all receive lanes 1 = Signal OK on all receive lanes

MDIO Registers 1.14 and 1.15: PMA/PMD Package Identifier

Figure 2-9 shows the MDIO Registers 1.14 and 1.15: PMA/PMD Package Identifier register.

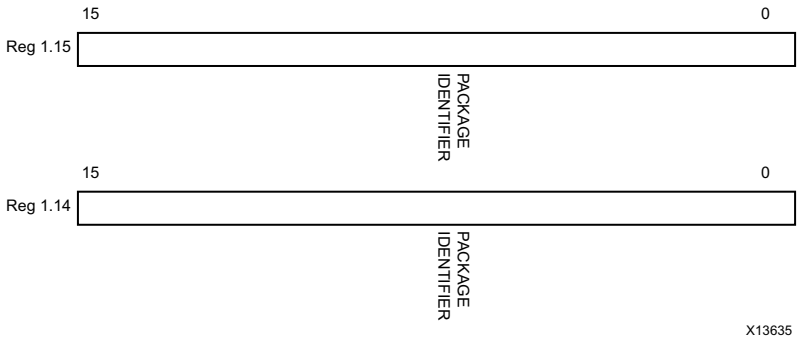

Figure 2-9: **PMA/PMD Package Identifier Registers**

Table 2-24 shows the PMA/PMD Package Identifier registers bit definitions.

Table 2-24: **PMA/PMD Package Identifier Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
1.15.15:0	PMA/PMD Package Identifier	All 0s	R	The block always returns 0 for these bits.
1.14.15:0	PMA/PMD Package Identifier	All 0s	R	The block always returns 0 for these bits.

MDIO Register 3.0: PCS Control 1

Figure 2-10 shows the MDIO Register 3.0: PCS Control 1.

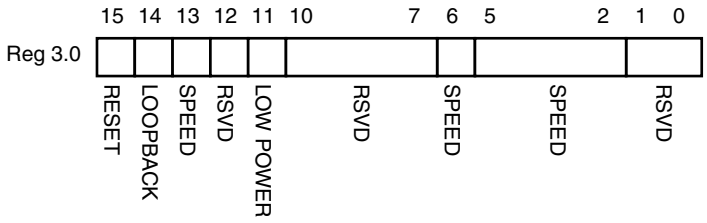

Figure 2-10: **PCS Control 1 Register**

Table 2-25 shows the PCS Control 1 register bit definitions.

Table 2-25: **PCS Control 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.0.15	Reset	0	R/W Self-clearing	0 = Normal operation 1 = Block reset The RXAUI block is reset when this bit is set to 1. It returns to 0 when the reset is complete.
3.0.14	10GBASE-R Loopback	0	R	The block always returns 0 for this bit and ignores writes.
3.0.13	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
3.0.12	Reserved	0	R	The block always returns 0 for this bit and ignores writes.
3.0.11	Power down	0	R/W	0 = Normal operation 1 = Power down mode When set to 1, the serial transceivers are placed in a low power state. Set to 0 to return to normal operation.
3.0.10:7	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
3.0.6	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
3.0.5:2	Speed Selection	All 0s	R	The block always returns 0s for these bits and ignores writes.
3.0.1:0	Reserved	All 0s	R	The block always returns 0 for this bit and ignores writes.

MDIO Register 3.1: PCS Status 1

Figure 2-11 shows the MDIO Register 3.1: PCS Status 1.

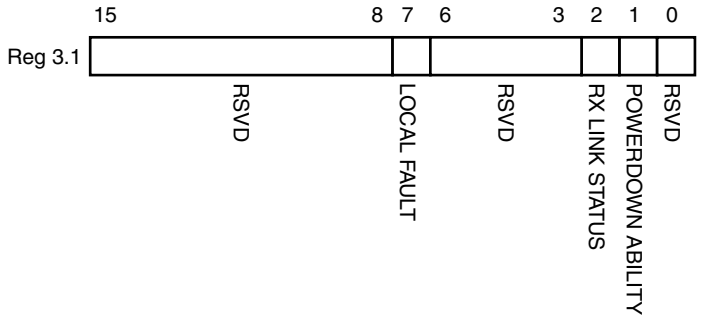

Figure 2-11: **PCS Status 1 Register**

Table 2-26 show the PCS 1 register bit definitions.

Table 2-26: **PCS Status 1 Register Bit Definition**

Bits	Name	Reset Value	Access Type	Description
3.1.15:8	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
3.1.7	Local Fault	–	R	0 = No local fault detected 1 = Local fault detected This bit is set to 1 whenever either of the bits 3.8.11 and 3.8.10 are set to 1.
3.1.6:3	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
3.1.2	PCS Receive Link Status	–	R Self-setting	0 = The PCS receive link is down 1 = The PCS receive link is up This is a latching Low version of bit 3.24.12.
3.1.1	Power Down Ability	1	R	The block always returns 1 for this bit.
3.1.0	Reserved	0	R	The block always returns 0 for this bit and ignores writes.

MDIO Registers 3.2 and 3.3: PCS Device Identifier

Figure 2-12 shows the MDIO Registers 3.2 and 3.3: PCS Device Identifier.

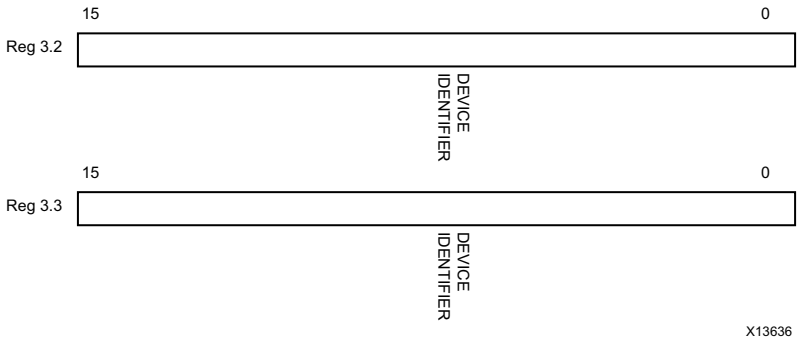

Figure 2-12: **PCS Device Identifier Registers**

Table 2-27 shows the PCS Device Identifier registers bit definitions.

Table 2-27: **PCS Device Identifier Registers Bit Definition**

Bits	Name	Reset Value	Access Type	Description
3.2.15:0	PCS Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.
3.3.15:0	PCS Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.

MDIO Register 3.4: PCS Speed Ability

Figure 2-13 shows the MDIO Register 3.4: PCS Speed Ability.

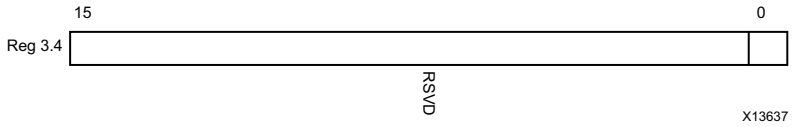

Figure 2-13: **PCS Speed Ability Register**

Table 2-28 shows the PCS Speed Ability register bit definitions.

Table 2-28: **PCS Speed Ability Register Bit Definition**

Bits	Name	Reset Value	Access Type	Description
3.4.15:1	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
3.4.0	10G Capable	1	R	The block always returns 1 for this bit and ignores writes.

MDIO Registers 3.5 and 3.6: PCS Devices in Package

Figure 2-14 shows the MDIO Registers 3.5 and 3.6: PCS Devices in Package.

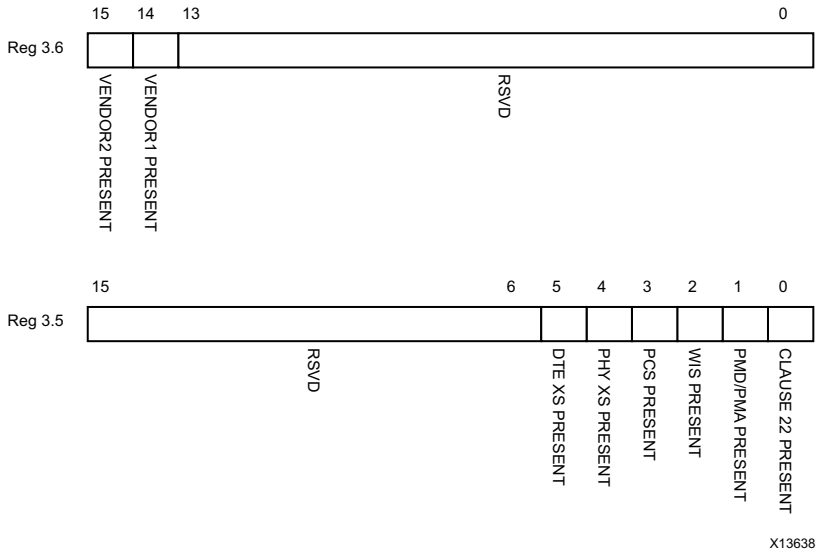

Figure 2-14: **PCS Devices in Package Registers**

Table 2-29 shows the PCS Devices in Package registers bit definitions.

Table 2-29: **PCS Devices in Package Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.6.15	Vendor-specific Device 2 present	0	R	The block always returns 0 for this bit.
3.6.14	Vendor- specific Device 1 present	0	R	The block always returns 0 for this bit.
3.6.13:0	Reserved	All 0s	R	The block always returns 0 for these bits.
3.5.15:6	Reserved	All 0s	R	The block always returns 0 for these bits.
3.5.5	PHY XS present	0	R	The block always returns 0 for this bit.
3.5.4	PHY XS present	0	R	The block always returns 0 for this bit.
3.5.3	PCS present	1	R	The block always returns 1 for this bit.
3.5.2	WIS present	0	R	The block always returns 0 for this bit.
3.5.1	PMA/PMD present	1	R	The block always returns 1 for this bit.
3.5.0	Clause 22 device present	0	R	The block always returns 0 for this bit.

MDIO Register 3.7: 10G PCS Control 2

Figure 2-15 shows the MDIO Register 3.7: 10G PCS Control 2.

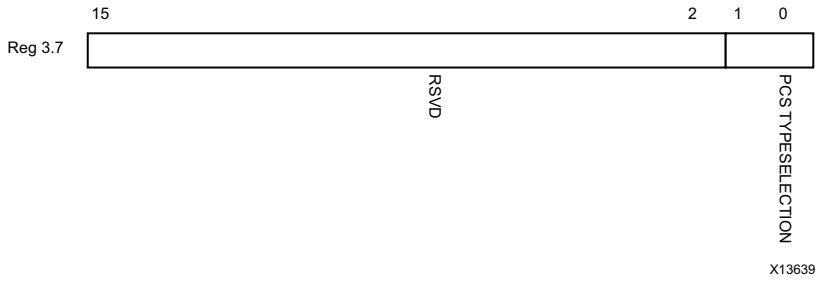

Figure 2-15: **10G PCS Control 2 Register**

Table 2-30 shows the 10 G PCS Control 2 register bit definitions.

Table 2-30: **10G PCS Control 2 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.7.15:2	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
3.7.1:0	PCS Type Selection	01	R	The block always returns 01 for these bits and ignores writes.

MDIO Register 3.8: 10G PCS Status 2

Figure 2-16 shows the MDIO Register 3.8: 10G PCS Status 2.

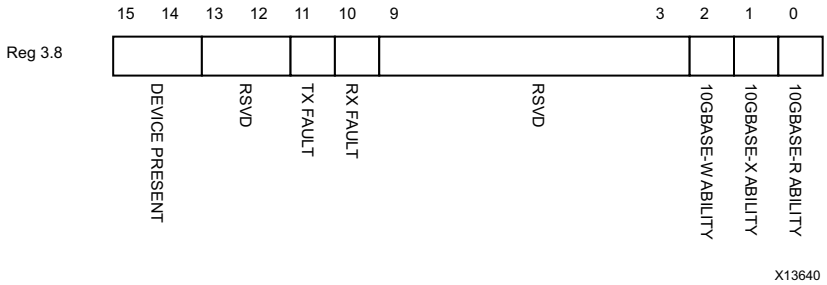

Figure 2-16: **10G PCS Status 2 Register**

Table 2-31 shows the 10G PCS Status 2 register bit definitions.

Table 2-31: **10G PCS Status 2 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.8.15:14	Device present	10	R	The block always returns 10.
3.8.13:12	Reserved	All 0s	R	The block always returns 0 for these bits.
3.8.11	Transmit local fault	–	R Latching High	0 = No fault condition on transmit path 1 = Fault condition on transmit path
3.8.10	Receive local fault	–	R Latching High	0 = No fault condition on receive path 1 = Fault condition on receive path
3.8.9:3	Reserved	All 0s	R	The block always returns 0 for these bits.
3.8.2	10GBASE-W Capable	0	R	The block always returns 0 for this bit.
3.8.1	10GBASE-X Capable	1	R	The block always returns 1 for this bit.
3.8.0	10GBASE-R Capable	0	R	The block always returns 0 for this bit.

MDIO Registers 3.14 and 3.15: PCS Package Identifier

Figure 2-17 shows the MDIO Registers 3.14 and 3.15: PCS Package Identifier.

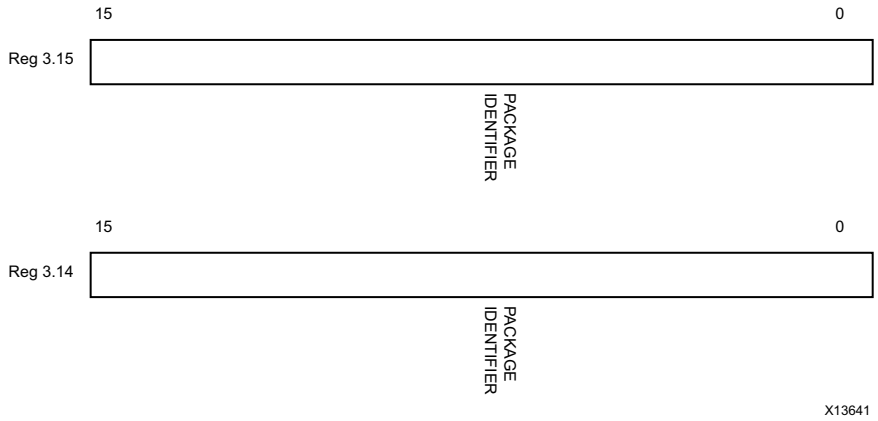

Figure 2-17: **Package Identifier Registers**

Table 2-32 shows the PCS Package Identifier registers bit definitions.

Table 2-32: **PCS Package Identifier Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.14.15:0	Package Identifier	All 0s	R	The block always returns 0 for these bits.
3.15.15:0	Package Identifier	All 0s	R	The block always returns 0 for these bits.

MDIO Register 3.24: 10GBASE-X Status

Figure 2-18 shows the MDIO Register 3.24: 10GBase-X Status.

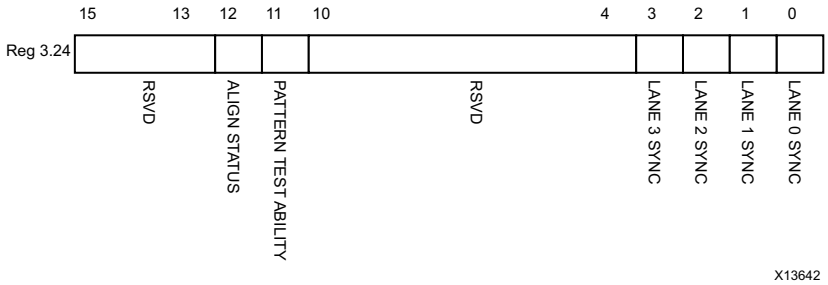

Figure 2-18: **10GBASE-X Status Register**

Table 2-33 shows the 10GBase-X Status register bit definitions.

Table 2-33: **10GBASE-X Status Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.24.15:13	Reserved	All 0s	R	The block always returns 0 for these bits.
3.24.12	10GBASE-X Lane Alignment Status	–	R	0 = 10GBASE-X receive lanes not aligned 1 = 10GBASE-X receive lanes aligned
3.24.11	Pattern Testing Ability	1	R	The block always returns 1 for this bit.
3.24.10:4	Reserved	All 0s	R	The block always returns 0 for these bits.
3.24.3	Lane 3 Sync	–	R	0 = Lane 3 is not synchronized 1 = Lane 3 is synchronized
3.24.2	Lane 2 Sync	–	R	0 =Lane 2 is not synchronized 1 =Lane 2 is synchronized
3.24.1	Lane 1 Sync	–	R	0 = Lane 1 is not synchronized 1 = Lane 1 is synchronize
3.24.0	Lane 0 Sync	–	R	0 = Lane 0 is not synchronized 1 = Lane 0 is synchronized

MDIO Register 3.25: 10GBASE-X Test Control

Figure 2-19 shows the MDIO Register 3.25: 10GBase-X Test Control.

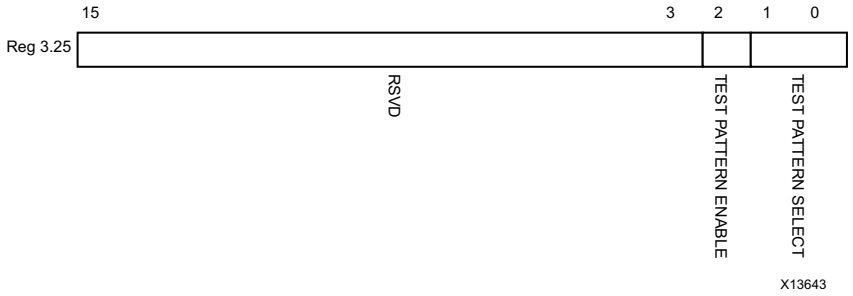

Figure 2-19: **Test Control Register**

Table 2-34 shows the 10GBase-X Test Control register bit definitions.

Table 2-34: **10GBASE-X Test Control Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
3.25.15:3	Reserved	All 0s	R	The block always returns 0 for these bits.
3.25.2	Transmit Test Pattern Enable	0	R/W	0 = Transmit test pattern disabled 1 = Transmit test pattern enable
3.25.1:0	Test Pattern Select	00	R/W	00 = High frequency test pattern 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved

DTE XS MDIO Register Map

When the core is configured as a DTE XGXS, it occupies MDIO Device Address 5 in the MDIO register address map (Table 2-35).

Table 2-35: **DTE XS MDIO Registers**

Register Address	Register Name
5.0	DTE XS Control 1
5.1	DTE XS Status 1
5.2, 5.3	DTE XS Device Identifier
5.4	DTE XS Speed Ability
5.5, 5.6	DTE XS Devices in Package
5.7	Reserved
5.8	DTE XS Status 2
5.9 to 5.13	Reserved
5.14, 5.15	DTE XS Package Identifier

Table 2-35: **DTE XS MDIO Registers *(Cont'd)***

Register Address	Register Name
5.16 to 5.23	Reserved
5.24	10G DTE XGXS Lane Status
5.25	10G DTE XGXS Test Control

MDIO Register 5.0:DTE XS Control 1

Figure 2-20 shows the MDIO Register 5.0: DTE XS Control 1.

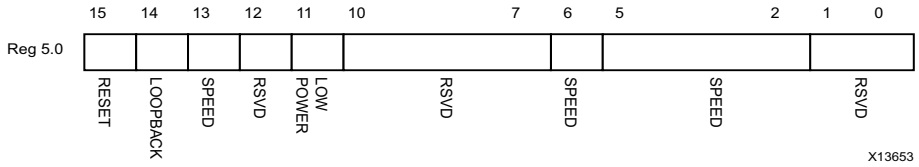

Figure 2-20: **DTE XS Control 1 Register**

Table 2-36 shows the DTE XS Control 1 register bit definitions.

Table 2-36: **DTE XS Control 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.0.15	Reset	0	R/W Self-clearing	0 = Normal operation 1 = Block reset The RXAUI block is reset when this bit is set to 1. It returns to 0 when the reset is complete.
5.0.14	Loopback	0	R/W	0 = Disable loopback mode 1 = Enable loopback mode The RXAUI block loops the signal in the serial transceivers back into the receiver.
5.0.13	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
5.0.12	Reserved	0	R	The block always returns 0 for this bit and ignores writes.
5.0.11	Power down	0	R/W	0 = Normal operation 1 = Power down mode When set to 1, the serial transceivers are placed in a low power state. Set to 0 to return to normal operation
5.0.10:7	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
5.0.6	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.

Table 2-36: **DTE XS Control 1 Register Bit Definitions *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
5.0.5:2	Speed Selection	All 0s	R	The block always returns 0s for these bits and ignores writes.
5.0.1:0	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.

MDIO Register 5.1: DTE XS Status 1

Figure 2-21 shows the MDIO Register 5.1: DTE XS Status 1.

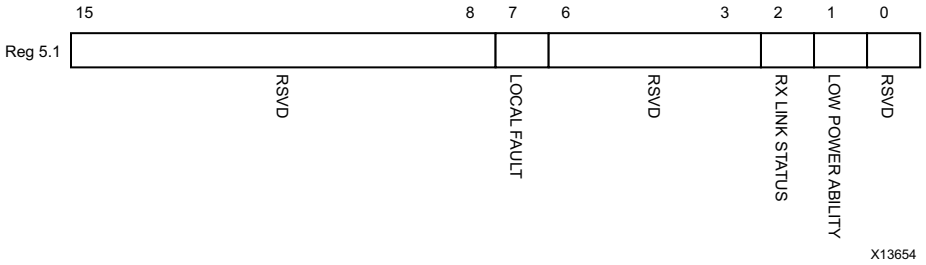

Figure 2-21: **DTE XS Status 1 Register**

Table 2-37 shows the DET XS Status 1 register bit definitions.

Table 2-37: **DTE XS Status 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.1.15:8	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
5.1.7	Local Fault	–	R	0 = No Local Fault detected 1 = Local fault detected This bit is set to 1 whenever either of the bits 5.8.11, 5.8.10 are set to 1.
5.1.6:3	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
5.1.2	DTE XS Receive Link Status	All 0s	R Self-setting	0 = The DTE XS receive link is down 1 = The DTE XS receive link is up This is a latching Low version of bit 5.24.12.
5.1.1	Power Down Ability	1	R	The block always returns 1 for this bit.
5.1.0	Reserved	0	R	The block always returns 0 for this bit and ignores writes.

MDIO Registers 5.2 and 5.3: DTE XS Device Identifier

Figure 2-22 shows the MDIO Registers 5.2 and 5.3: DTE XS Device Identifier.

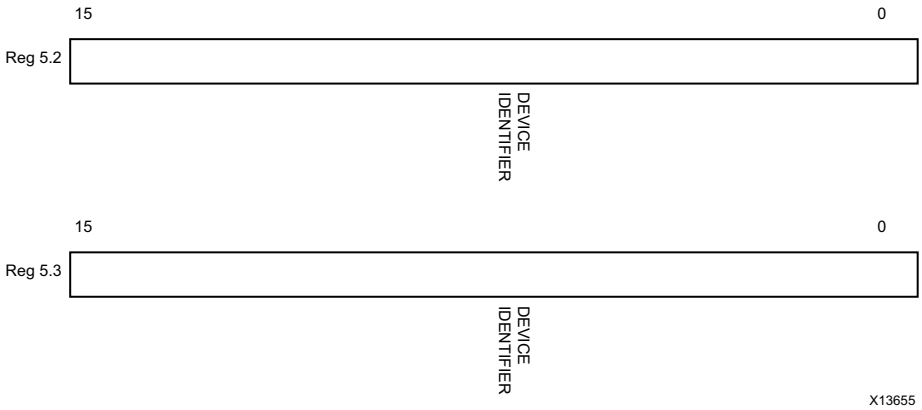

Figure 2-22: **DTE XS Device Identifier Registers**

Table 2-38 shows the DTE XS Device Identifier registers bit definitions.

Table 2-38: **DTE XS Device Identifier Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.2.15:0	DTE XS Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.
5.3.15:0	DTE XS Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.

MDIO Register 5.4: DTE XS Speed Ability

Figure 2-23 shows the MDIO Register 5.4: DTE Speed Ability.

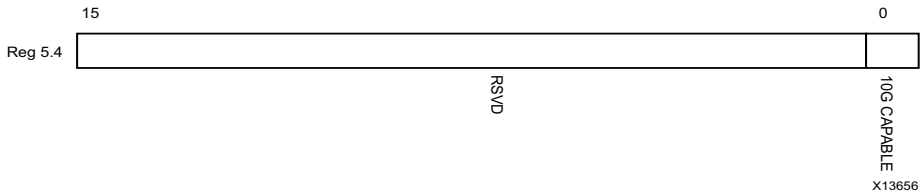

Figure 2-23: **DTE XS Speed Ability Register**

Table 2-39 shows the DTE XS Speed Ability register bit definitions.

Table 2-39: **DTE XS Speed Ability Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.4.15:1	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
5.4.0	10G Capable	1	R	The block always returns 1 for this bit and ignores writes.

MDIO Registers 5.5 and 5.6: DTE XS Devices in Package

Figure 2-24 shows the MDIO Registers 5.5 and 5.6: DTE XS Devices in Package.

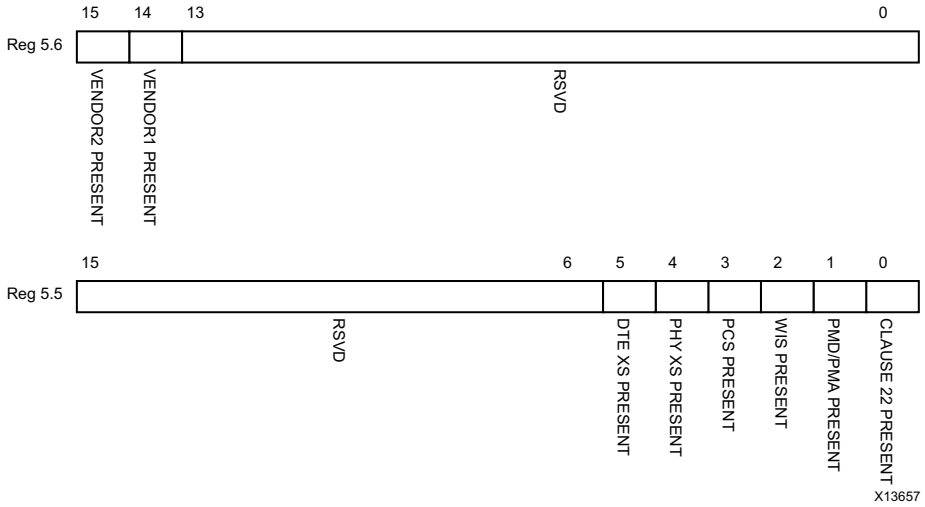

Figure 2-24: **DTE XS Devices in Package Register**

Table 2-40 shows the DTE XS Devices in Package registers bit definitions.

Table 2-40: **DTE XS Devices in Package Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.6.15	Vendor-specific Device 2 present	0	R	The block always returns 0 for this bit.
5.6.14	Vendor-specific Device 1 present	0	R	The block always returns 0 for this bit.
5.6.13:0	Reserved	All 0s	R	The block always returns 0 for these bits.
5.6.15:6	Reserved	All 0s	R	The block always returns 0 for these bits.
5.5.5	DTE XS present	1	R	The block always returns 1 for this bit.
5.5.4	PHY XS present	0	R	The block always returns 0 for this bit.
5.5.3	PCS present	0	R	The block always returns 0 for this bit.
5.5.2	WIS present	0	R	The block always returns 0 for this bit.
5.5.1	PMA/PMD present	0	R	The block always returns 0 for this bit.
5.5.0	Clause 22 Device present	0	R	The block always returns 0 for this bit.

MDIO Register 5.8: DTE XS Status 2

Figure 2-25 shows the MDIO Register 5.8: DTE XS Status 2.

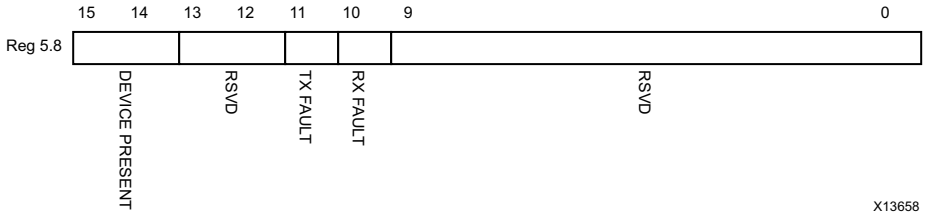

Figure 2-25: **DTE XS Status 2 Register**

Table 2-41 show the DTE XS Status 2 register bits definitions.

Table 2-41: **DTE XS Status 2 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.8.15:14	Device present	10	R	The block always returns 10.
5.8.13:12	Reserved	All 0s	R	The block always returns 0 for these bits.
5.8.11	Transmit Local Fault	–	R Latching High	0 = No fault condition on transmit path 1 = Fault condition on transmit path
5.8.10	Receive Local Fault	–	R Latching High	0 = No fault condition on receive path 1 = Fault condition on receive path
5.8.9:0	Reserved	All 0s	R	The block always returns 0 for these bits.

MDIO Registers 5.14 and 5.15: DTE XS Package Identifier

Figure 2-26 shows the MDIO Registers 5.14 and 5.15: DTE XS Package Identifier.

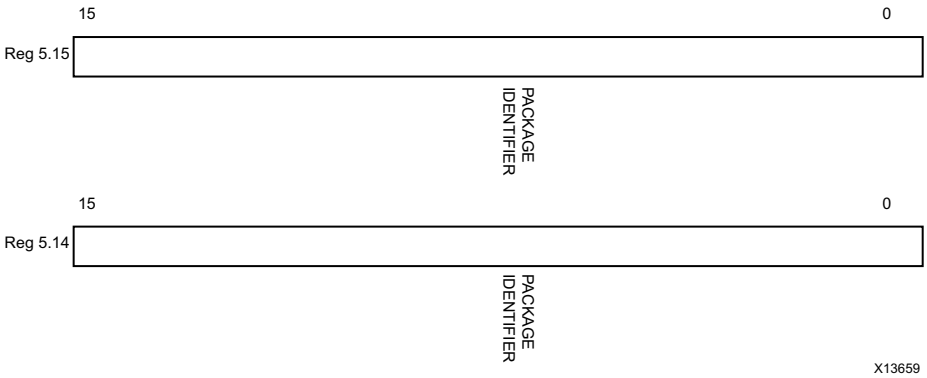

Figure 2-26: **DTE XS Package Identifier Registers**

Table 2-42 shows the DTE XS Package Identifier registers bit definitions.

Table 2-42: **DTE XS Package Identifier Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.14.15:0	DTE XS Package Identifier	All 0s	R	The block always returns 0 for these bits.
5.15.15:0	DTE XS Package Identifier	All 0s	R	The block always returns 0 for these bits.

Test Patterns

The RXAUI core is capable of sending test patterns for system debug. These patterns are defined in Annex 48A of *IEEE Std. 802.3-2008* and transmission of these patterns is controlled by the MDIO Test Control Registers.

There are three types of pattern available:

- High frequency test pattern of 1010101010.... at each device-specific transceiver output
- Low frequency test pattern of 11111000001111100000111110000 0.... at each device-specific transceiver output
- mixed frequency test pattern of 11111010110000010100111110101100000 1010... at each device-specific transceiver output.

MDIO Register 5.24: DTE XS Lane Status

Figure 2-27 shows the MDIO Register 5.24: DTE XS Lane Status.

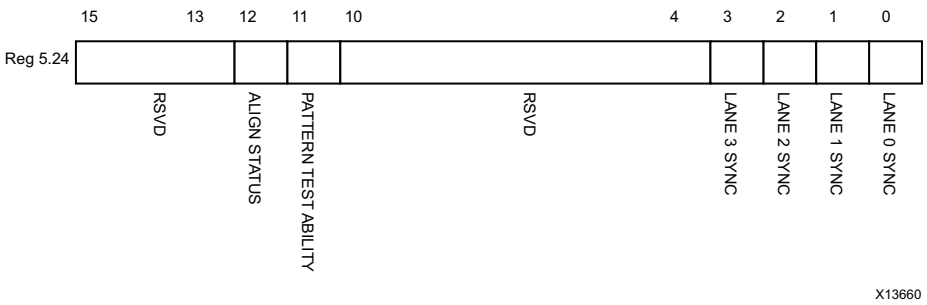

Figure 2-27: **DTE XS Lane Status Register**

Table 2-43 shows the DTE XS Lane Status register bit definitions.

Table 2-43: **DTE XS Lane Status Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.24.15:13	Reserved	All 0s	R	The block always returns 0 for these bits.
5.24.12	DTE XGXS Lane Alignment Status	–	R	0 = DTE XGXS receive lanes not aligned 1 = DTE XGXS receive lanes aligned
5.24.11	Pattern testing ability	1	R	The block always returns 1 for this bit.
5.24.10:4	Reserved	All 0s	R	The block always returns 0 for these bits.
5.24.3	Lane 3 Sync	–	R	0 = Lane 3 is not synchronized 1 = Lane 3 is synchronized
5.24.2	Lane 2 Sync	–	R	0 = Lane 2 is not synchronized 1 = Lane 2 is synchronized
5.24.1	Lane 1 Sync	–	R	0 = Lane 1 is not synchronized 1 = Lane 1 is synchronized
5.24.0	Lane 0 Sync	–	R	0 = Lane 0 is not synchronized 1 = Lane 0 is synchronized

MDIO Register 5.25: 10G DTE XGXS Test Control

Figure 2-28 shows the MDIO Register 5.25: 10G DTE XGXS Test Control.

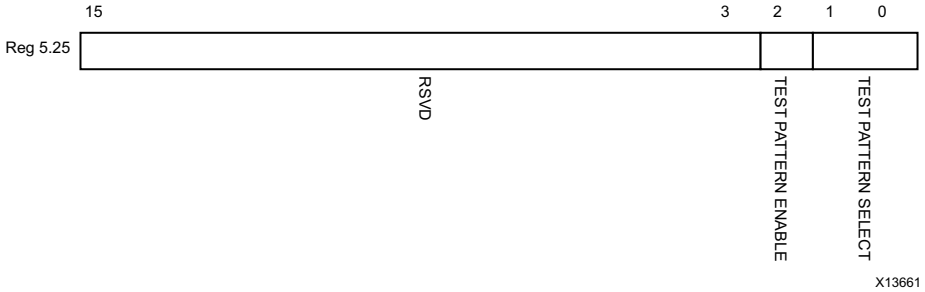

Figure 2-28: **10G DTE XGXS Test Control Register**

Table 2-44 shows the 10G DTE XGXS Test Control register bit definitions.

Table 2-44: **10G DTE XGXS Test Control Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
5.25.15:3	Reserved	All 0s	R	The block always returns 0 for these bits.
5.25.2	Transmit Test Pattern Enable	0	R/W	0 = Transmit test pattern disabled 1 = Transmit test pattern enable
5.25.1:0	Test Pattern Select	00	R/W	00 = High frequency test pattern 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved

PHY XS MDIO Register Map

When the core is configured as a PHY XGXS, it occupies MDIO Device Address 4 in the MDIO register address map (Table 2-45).

Table 2-45: **PHY XS MDIO Registers**

Register Address	Register Name
4.0	PHY XS Control 1
4.1	PHY XS Status 1
4.2, 4.3	Device Identifier
4.4	PHY XS Speed Ability
4.5, 4.6	Devices in Package
4.7	Reserved
4.8	PHY XS Status 2
4.9 to 4.13	Reserved
4.14, 4.15	Package Identifier
4.16 to 4.23	Reserved
4.24	10G PHY XGXS Lane Status
4.25	10G PHY XGXS Test Control

MDIO Register 4.0: PHY XS Control 1

Figure 2-29 shows the MDIO Register 4.0: PHY XS Control 1.

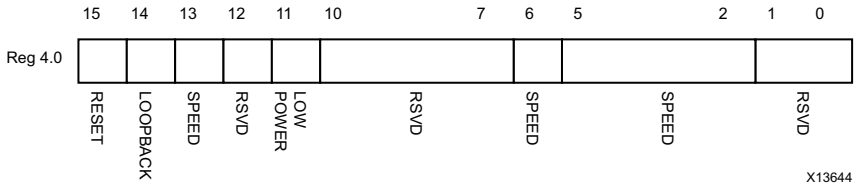

Figure 2-29: **PHY XS Control 1 Register**

Table 2-46 shows the PHY XS Control 1 register bit definitions.

Table 2-46: **PHY XS Control 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.0.15	Reset	0	R/W Self-clearing	0 = Normal operation 1 = Block reset The RXAUI block is reset when this bit is set to 1. It returns to 0 when the reset is complete.
4.0.14	Loopback	0	R/W	0 = Disable loopback mode 1 = Enable loopback mode The RXAUI block loops the signal in the serial transceivers back into the receiver.
4.0.13	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
4.0.12	Reserved	0	R	The block always returns 0 for this bit and ignores writes.
4.0.11	Power down	0	R/W	0 = Normal operation 1 = Power down mode When set to 1, the serial transceivers are placed in a low power state. Set to 0 to return to normal operation
4.0.10:7	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
4.0.6	Speed Selection	1	R	The block always returns 1 for this bit and ignores writes.
4.0.5:2	Speed Selection	All 0s	R	The block always returns 0s for these bits and ignores writes.
4.0.1:0	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.

MDIO Register 4.1: PHY XS Status 1

Figure 2-30 shows the MDIO Register 4.1: PHY XS Status 1.

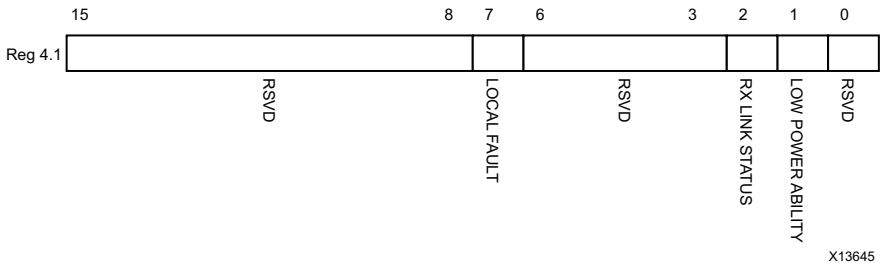

Figure 2-30: **PHY XS Status 1 Register**

Table 2-47 shows the PHY XS Status 1 register bit definitions.

Table 2-47: **PHY XS Status 1 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.1.15:8	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
4.1.7	Local Fault	–	R	0 = No Local Fault detected 1 = Local fault detected This bit is set to 1 whenever either of the bits 4.8.11 and 4.8.10 are set to 1.
4.1.6:3	Reserved	All 0s	R	The block always returns 0s for these bits and ignores writes.
4.1.2	PHY XS Receive Link Status	–	R Self-setting	0 =The PHY XS receive link is down 1 = The PHY XS receive link is up. This is a latching Low version of bit 4.24.12.
4.1.1	Power Down Ability	1	R	The block always returns 1 for this bit.
4.1.0	Reserved	0	R	The block always returns 0 for this bit and ignores writes.

MDIO Registers 4.2 and 4.3: PHY XS Device Identifier

Figure 2-31 shows the MDIO Registers 4.2 and 4.3: PHY XS Device Identifier.

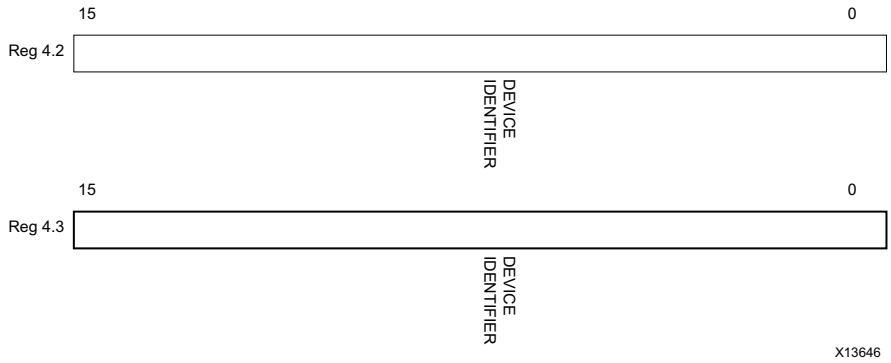

Figure 2-31: **PHY XS Device Identifier Registers**

Table 2-48 shows the PHY XS Devices Identifier registers bit definitions.

Table 2-48: **PHY XS Device Identifier Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.2.15:0	PHY XS Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.
4.3.15:0	PHY XS Identifier	All 0s	R	The block always returns 0 for these bits and ignores writes.

MDIO Register 4.4: PHY XS Speed Ability

Figure 2-32 shows the MDIO Register 4.4: PHY XS Speed Ability.

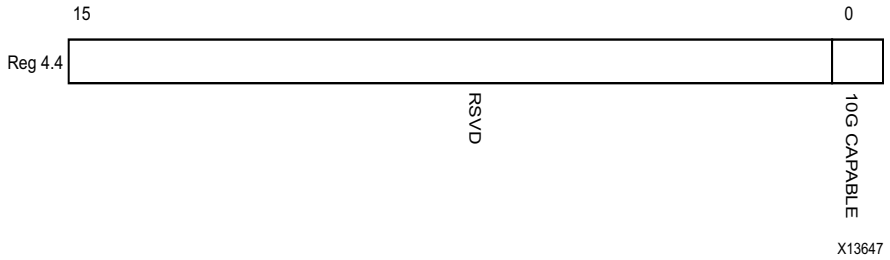

Figure 2-32: **PHY XS Speed Ability Register**

Table 2-49 shows the PHY XS Speed Ability register bit definitions.

Table 2-49: **PHY XS Speed Ability Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.4.15:1	Reserved	All 0s	R	The block always returns 0 for these bits and ignores writes.
4.4.0	10G Capable	1	R	The block always returns 1 for this bit and ignores writes.

MDIO Registers 4.5 and 4.6: PHY XS Devices in Package

Figure 2-33 shows the MDIO Registers 4.5 and 4.6: PHY XS Devices in Package.

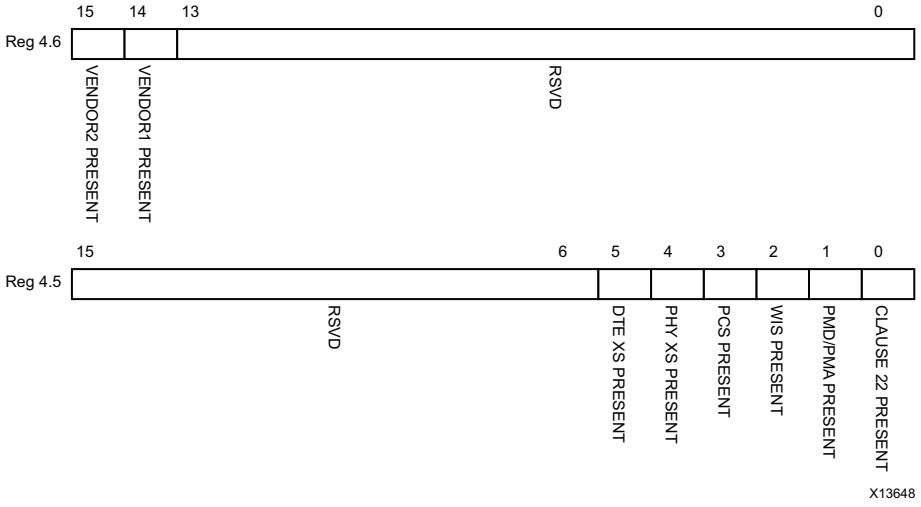

Figure 2-33: **PHY XS Devices in Package Registers**

Table 2-50 shows the PHY XS Devices in Package registers bit definitions.

Table 2-50: **PHY XS Devices in Package Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.6.15	Vendor-specific Device 2 present	0	R	The block always returns 0 for this bit.
4.6.14	Vendor-specific Device 1 present	0	R	The block always returns 0 for this bit.
4.6.13:0	Reserved	All 0s	R	The block always returns 0 for these bits.
4.5.15:6	Reserved	All 0s	R	The block always returns 0 for these bits.
4.5.5	DTE XS present	0	R	The block always returns 0 for this bit.
4.5.4	PHY XS present	1	R	The block always returns 1 for this bit.
4.5.3	PCS present	0	R	The block always returns 0 for this bit.
4.5.2	WIS present	0	R	The block always returns 0 for this bit.
4.5.1	PMA/PMD present	0	R	The block always returns 0 for this bit.
4.5.0	Clause 22 device present	0	R	The block always returns 0 for this bit.

MDIO Register 4.8: PHY XS Status 2

Figure 2-34 shows the MDIO Register 4.8: PHY XS Status 2.

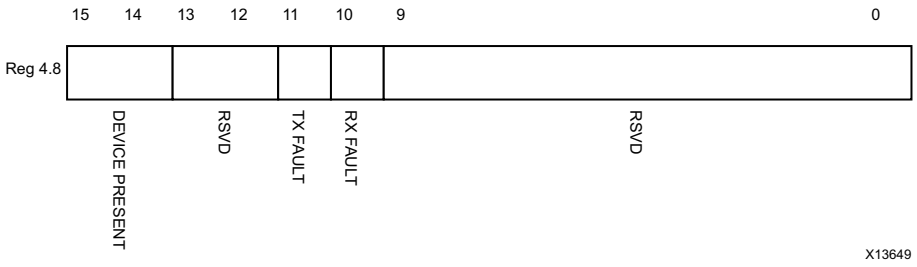

Figure 2-34: **PHY XS Status 2 Register**

Table 2-51 shows the PHY XS Status 2 register bit definitions.

Table 2-51: **PHY XS Status 2 Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.8.15:14	Device present	10	R	The block always returns 10.
4.8.13:12	Reserved	All 0s	R	The block always returns 0 for these bits.
4.8.11	Transmit local fault	–	R Latching High	0 = No fault condition on transmit path 1 = Fault condition on transmit path
4.8.10	Receive local fault	–	R Latching High	0 = No fault condition on receive path 1 = Fault condition on receive path
4.8.9:0	Reserved	All 0s	R	The block always returns 0 for these bits.

MDIO Registers 4.14 and 4.15: PHY XS Package Identifier

Figure 2-35 shows the MDIO 4.14 and 4.15 Registers: PHY XS Package Identifier.

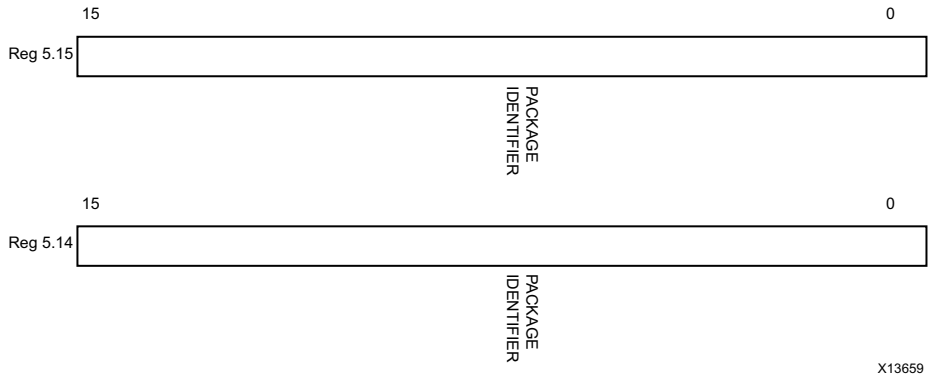

Figure 2-35: **PHY XS Package Identifier Registers**

Table 2-52 shows the Package Identifier registers bit definitions.

Table 2-52: **Package Identifier Registers Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.15.15:0	PHY XS Package Identifier	All 0s	R	The block always returns 0 for these bits.
4.14.15:0	PHY XS Package Identifier	All 0s	R	The block always returns 0 for these bits.

MDIO Register 4.24: 10G PHY XGXS Lane Status

Figure 2-36 shows the MDIO Register 4.24: 10G XGXS Lane Status.

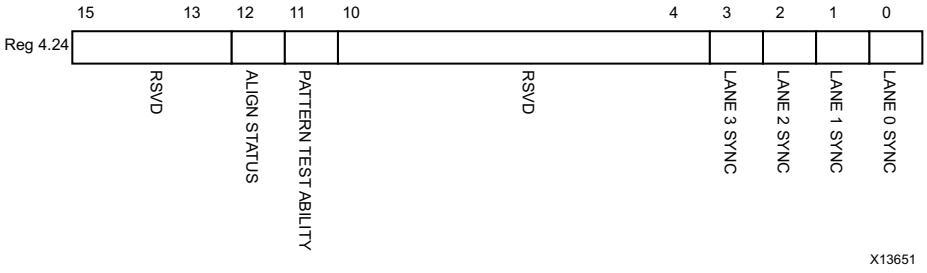

Figure 2-36: **10G PHY XGXS Lane Status Register**

Table 2-53 shows the 10G PHY XGXS Lane register bit definitions.

Table 2-53: **10G PHY XGXS Lane Status Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.24.15:13	Reserved	All 0s	R	The block always returns 0 for these bits.
4.24.12	PHY XGXS Lane Alignment Status	–	R	0 = PHY XGXS receive lanes not aligned 1 = PHY XGXS receive lanes aligned
4.24.11	Pattern Testing Ability	1	R	The block always returns 1 for this bit.
4.24.10:4	Reserved	All 0s	R	The block always returns 0 for these bits.
4.24.3	Lane 3 Sync	–	R	0 = Lane 3 is not synchronized 1 = Lane 3 is synchronized
4.24.2	Lane 2 Sync	–	R	0 = Lane 2 is not synchronized 1 = Lane 2 is synchronized
4.24.1	Lane 1 Sync	–	R	0 = Lane 1 is not synchronized 1 = Lane 1 is synchronized
4.24.0	Lane 0 Sync	–	R	0 = Lane 0 is not synchronized 1 = Lane 0 is synchronized

MDIO Register 4.25: 10G PHY XGXS Test Control

Figure 2-37 shows the MDIO Register 4.25: 10G XGXS Test Control.

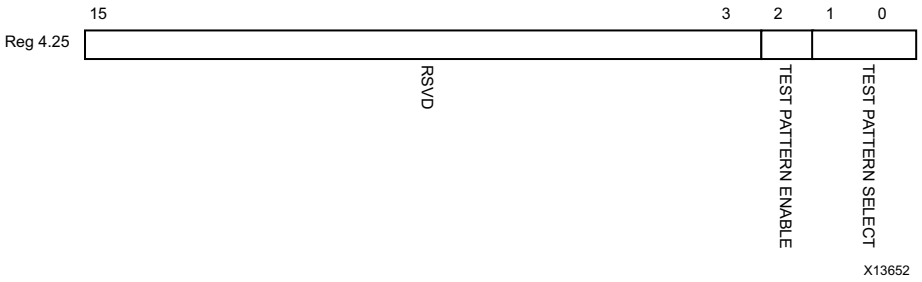

Figure 2-37: **10G PHY XGXS Test Control Register**

Table 2-54 shows the 10G PHY XGXS Test Control register bit definitions.

Table 2-54: **10G PHY XGXS Test Control Register Bit Definitions**

Bits	Name	Reset Value	Access Type	Description
4.25.15:3	Reserved	All 0s	R	The block always returns 0 for these bits.
4.25.2	Transmit Test Pattern Enable	0	R/W	0 = Transmit test pattern disabled 1 = Transmit test pattern enable
4.25.1:0	Test Pattern Select	00	R/W	00 = High frequency test pattern 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved

Configuration and Status Vectors

If the RXAUI core is generated without an MDIO interface, the key configuration and status information is carried on simple bit vectors, which are:

- configuration_vector[6:0]
- status_vector[7:0]

Table 2-55 shows the Configuration Vector bit definitions.

Table 2-55: **Configuration Vector Bit Definitions**

Bits	Name	Description
6:5	Test Select[1:0]	Selects the test pattern. See bits 5.25.1:0 in Table 2-44, page 37.
4	Test Enable	Enables transmit test pattern generation. See bit 5.25.2 in Table 2-44, page 37.
3	Reset RX Link Status	Sets the RX Link Status bit (status_vector[7]). See Table 2-56. This bit should be driven by a register on the same clock domain as the RXAUI core.
2	Reset Local Fault	Clears both TX Local Fault and RX Local Fault bits (status_vector[0] and status_vector[1]). See Table 2-56. This bit should be driven by a register on the same clock domain as the RXAUI core.
1	Power Down	Sets the device-specific transceivers into power down mode. See bit 5.0.11 in Table 2-36, page 31.
0	Loopback	Sets serial loopback in the device-specific transceivers. See bit 5.0.14 in Table 2-36, page 31.

Table 2-56 shows the Status Vector bit definitions.

Table 2-56: **Status Vector Bit Definitions**

Bits	Name	Description
7	RX Link Status	1 if the Receiver link is up, otherwise 0. See bit 5.1.2 in Table 2-37, page 32. Latches Low. Cleared by rising edge on configuration_vector[3].
6	Alignment	1 if the RXAUI receiver is aligned over all four logical XAUI lanes, otherwise 0. See bit 5.24.12 in Table 2-42, page 36. This is also used to generate the align_status signal described in Table 2-57.
5:2	Synchronization	Each bit is 1 if the corresponding RXAUI lane is synchronized on receive, otherwise 0. See bits 5.24.3:0 in Table 2-42, page 36. These four bits are also used to generate the sync_status[3:0] signal described in Table 2-57.
1	RX Local Fault	1 if there is a fault in the receive path, otherwise 0. See bit 5.8.10 in Table 2-41, page 35. Latches High. Cleared by rising edge on configuration_vector[2].
0	TX Local Fault	1 if there is a fault in the transmit path, otherwise 0. See bit 5.8.11 in Table 2-41, page 35. Latches High. Cleared by rising edge on configuration_vector[2].

Bits[1:0] of the status_vector port, the Local Fault bits, are latching-high and cleared low by Bit[2] of the configuration_vector port. Figure 2-38 shows how the status bits are cleared.

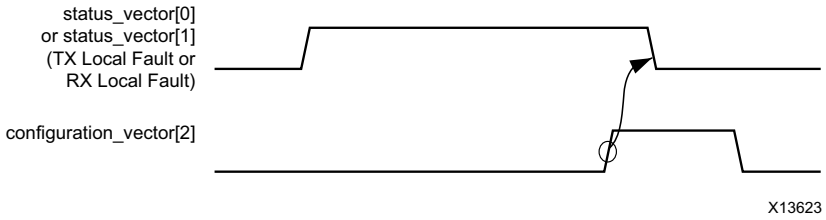

Figure 2-38: **Clearing the Local Fault Status Bits**

Bit[7] of the status_vector port, the RX Link Status bit, is latching-low and set high by Bit[3] of the configuration vector. Figure 2-39 shows how the status bit is set.

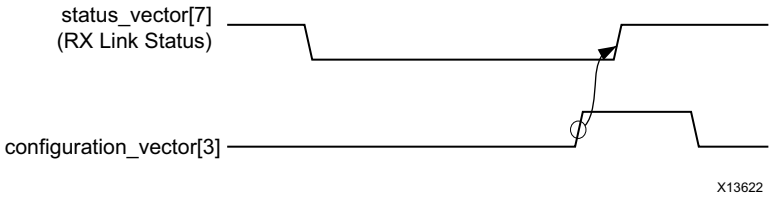

Figure 2-39: **Setting the RX Link Status Bit**

Alignment and Synchronization Status Ports

In addition to the configuration and status interfaces described in the previous section, there is some information on the debug output port signalling the alignment and synchronization status of the receiver (Table 2-57).

Table 2-57: **Alignment Status and Synchronization Status Ports**

Port Name	Description
debug[5]	1 when the RXAUI receiver is aligned across all four XAUI logical lanes, 0 otherwise.
debug[4:1]	Each pin is 1 when the respective XAUI logical lane receiver is synchronized to byte boundaries, 0 otherwise.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

This section describes the steps required to turn a RXAUI core into a fully-functioning design with user-application logic.

IMPORTANT: *Not all implementations require all of the design steps listed in this chapter. Follow the logic design guidelines in this manual carefully.*

Use the Example Design as a Starting Point

The RXAUI core has an example design that can be implemented in an FPGA and simulated. This design can be used as a starting point for your own design or can be used to sanity-check your application in the event of difficulty.

See Chapter 8, Detailed Example Design for information about using and customizing the example designs for the RXAUI core.

Know the Degree of Difficulty

RXAUI designs are challenging to implement in any technology, and the degree of difficulty is further influenced by:

- Maximum system clock frequency
- Targeted device architecture
- Nature of your application

All RXAUI implementations need careful attention to system performance requirements. Pipelining, logic mapping, placement constraints, and logic duplication are all methods that help boost system performance.

Keep It Registered

To simplify timing and increase system performance in an FPGA design, keep all inputs and outputs registered between your application and the core. This means that all inputs and outputs from your application should come from, or connect to a flip-flop. While registering signals might not be possible for all paths, it simplifies timing analysis and makes it easier for the Xilinx tools to place and route the design.

Recognize Timing Critical Signals

The XDC provided with the example design for the core identifies the critical signals and the timing constraints that should be applied. See Chapter 5, Constraining the Core for further information.

Use Supported Design Flows

The core HDL is added to the open Vivado® project. The core is then synthesized along with the rest of the project as part of project synthesis.

Make Only Allowed Modifications

The RXAUI core is not user-modifiable. Do not make modifications as they can have adverse effects on system timing and protocol compliance. Supported user configurations of the RXAUI core can only be made by selecting the options from within the Vivado Design Suite tool when the core is generated. See Chapter 4, Customizing and Generating the Core.

Shared Logic

Shared Logic provides a flexible architecture that works both as a stand-alone core and as part of a larger design with one of more core instances. This minimizes the amount of HDL modifications required, but at the same time retains the flexibility to address for uses of the core.

There is a level of hierarchy called <component_name>_support. Figure 3-1 and Figure 3-2 show two hierarchies where the shared logic is either contained in the core or in the example design. In these figures, <component_name> is the name of the generated core. The difference between the two hierarchies is the boundary of the core. it is controlled using the Shared Logic option in the RXAUI customization GUI.

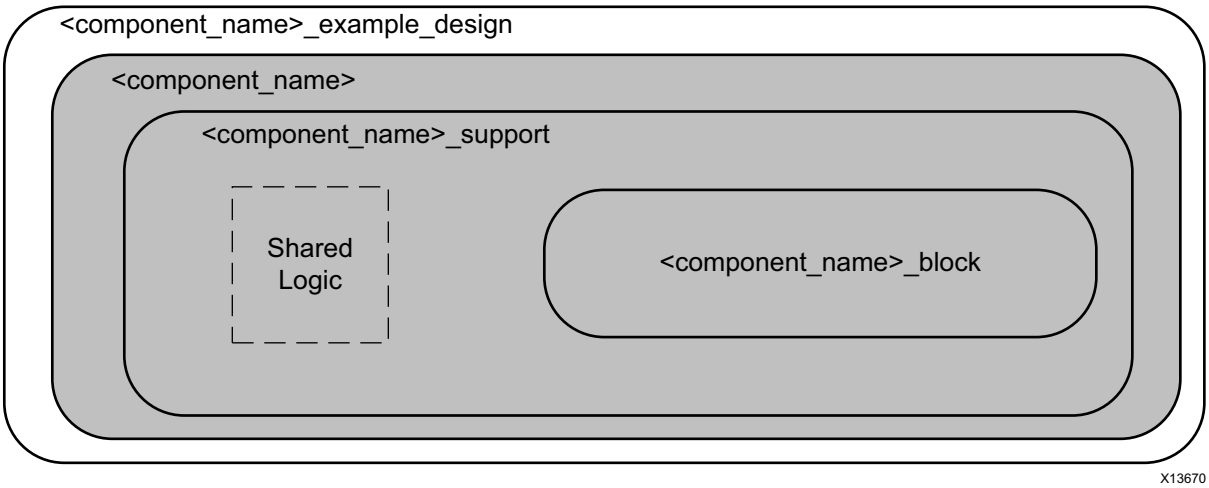

Figure 3-1: **Shared Logic Included in Core**

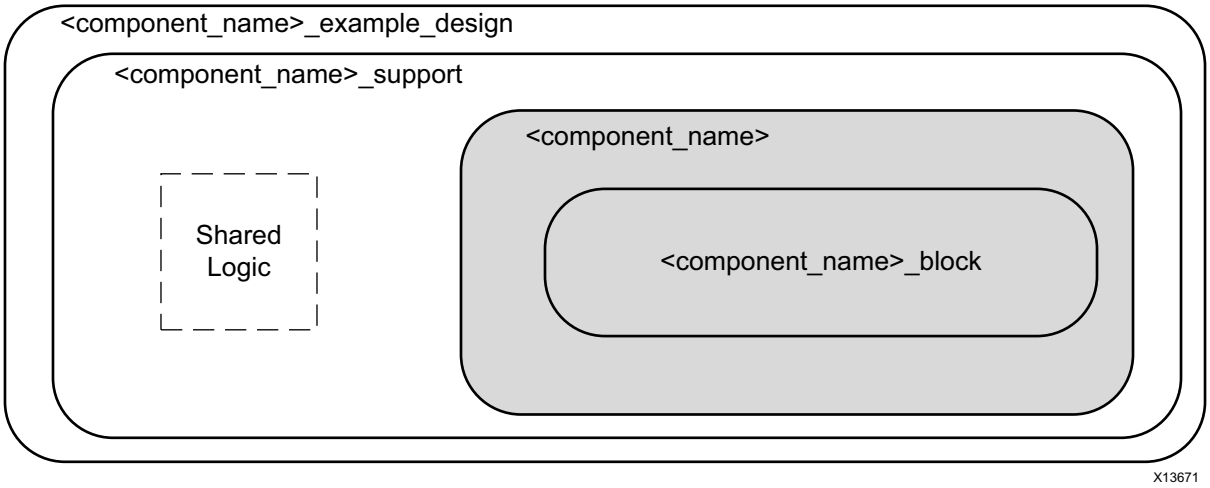

Figure 3-2: **Shared Logic Included in Example Design**

The shared logic comprises IBUFDS_GT, and the GT quad PLL with associated reset logic.

Shared Logic in Core

Select this option if:

- You do not require direct control over the Transceiver Quad PLL and Transceiver differential clock buffer.
- You want to manage multiple customizations of the core for multi-core designs.
- This is the first RXAUI core in a multi-core system.

These components are included in the core, and their output ports are also provided as core outputs.

Shared Logic in Example Design

Select this option if either:

- This is the second RXAUI core in a multi-core design
- You only want to manage one customization of the RXAUI core in your design
- You want direct access to the Transceiver quad PLL and differential reference clock buffer.

To fully utilize a transceiver quad, customize one RXAUI core with shared logic in the core, and one with shared logic in the example design. You can connect the quad PLL outputs from the first RXAUI core to the second core.

If you want fine control - you can select 'Include shared logic in example design' and base your own logic on the shared logic produced in the example design.

Clocking

The clocking schemes in this section are illustrative only and might require customization for a specific application. See Table 2-8 for information on the clock ports.

The transceiver common PLL can be included as part of the core if the **Include Shared Logic in Core** GUI option is selected. If this option is deselected, it appears in the “support” layer in the example design for reference.

Reference Clock

The transceivers use a reference clock of 156.25 MHz to operate at a line rate of 6.25 Gb/s.

Transceiver Placement

Common to all schemes shown is that a single IBUFDS_GTE2 (7 series FPGAs) is used to feed the reference clocks for all transceivers. In addition, timing requirements are met if both transceivers are placed next to each other.

For details about transceiver clock distribution, see the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 2] and the *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 3].

Dune Networks RXAUI (7 Series FPGAs)

The clocking scheme for 7 series GTX transceivers with Shared Logic included in the core is shown in Figure 3-3.

The transceiver primitives require a 156.25 MHz clock. The 156.25 MHz clock is used as the clock for the encrypted HDL part of the RXAUI core and is typically also used for your logic.

A dedicated clock is used by the transceivers; this is connected to the `dclk` port on the core. The example design uses a 50 MHz clock. Choosing a different frequency might allow sharing of clock resources. See the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 2] and the *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 3] for details about this clock.

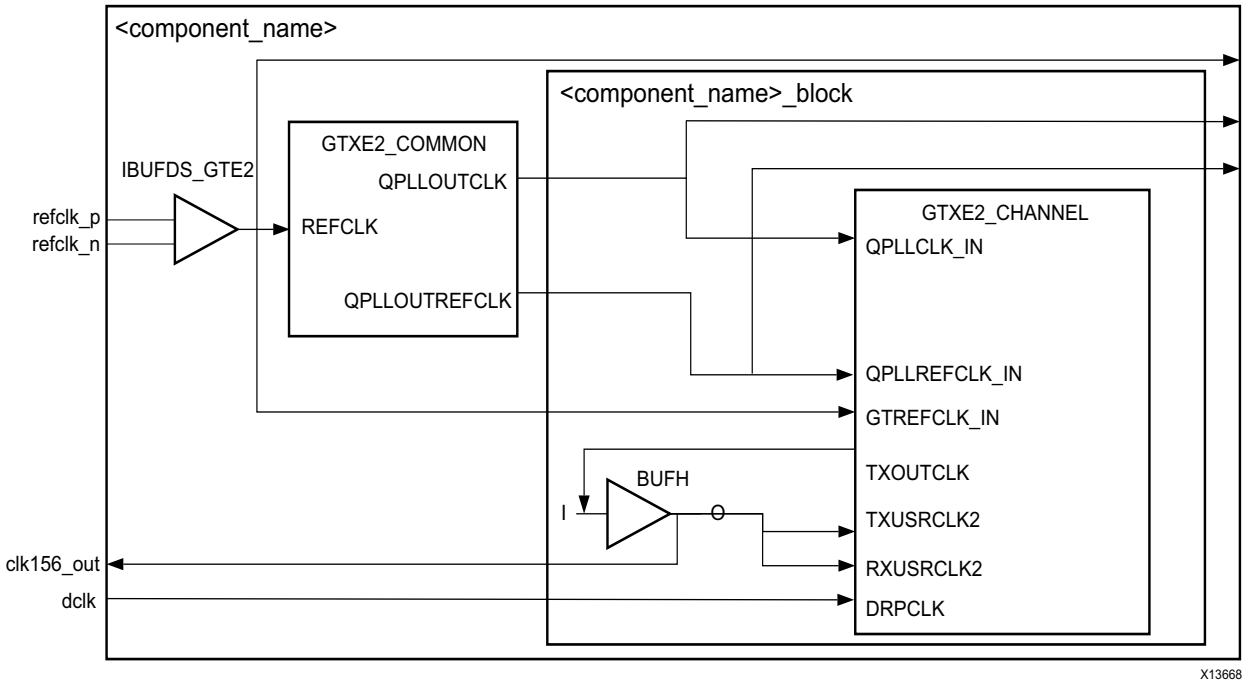

Figure 3-3: **Clock Scheme for Dune Networks RXAUI - GTX Transceivers**

Similarly, Figure 3-4 shows the clocking scheme for 7 series GTH transceivers with Shared Logic included in the core.

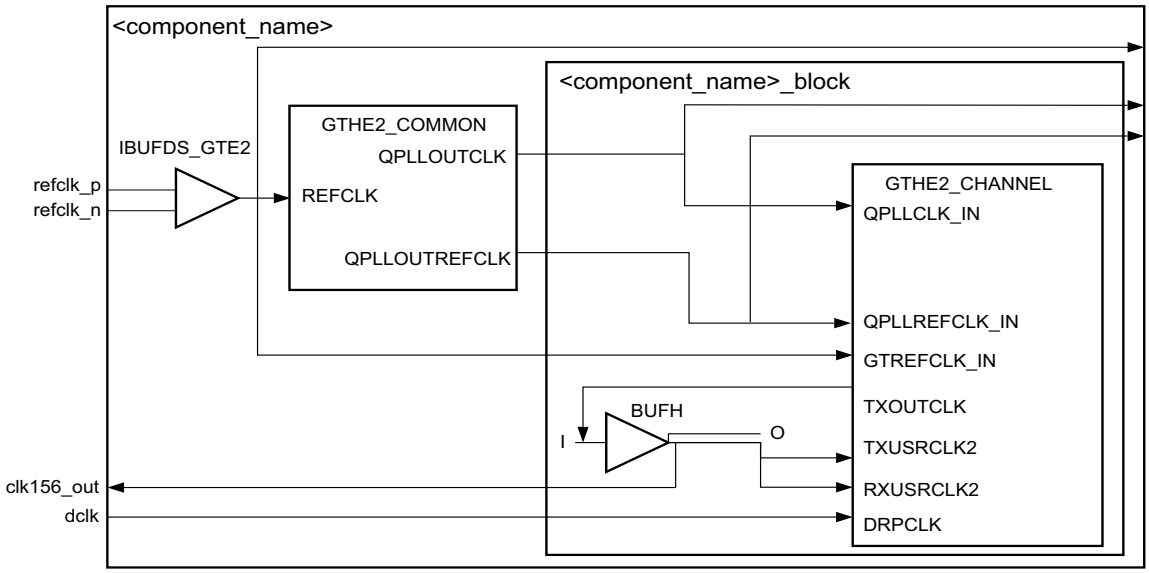

Figure 3-4: **Clock Scheme for Dune Networks RXAUI – GTH Transceivers**

Figure 3-5 shows the clocking scheme for 7 series GTP transceivers with Shared Logic included in the core.

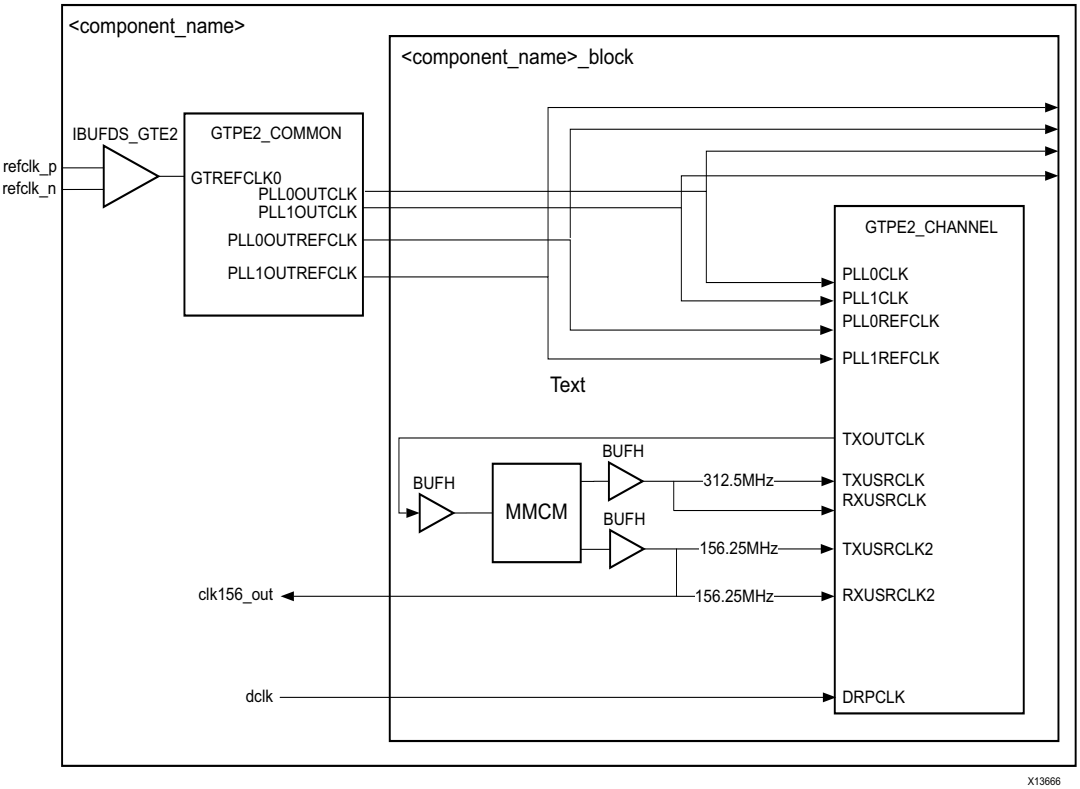

Figure 3-5: **Clock Scheme for Dune Networks RXAUI – GTP Transceivers**

Figure 3-6 shows the clocking scheme for 7 series GTX transceivers with Shared Logic included in the example design.

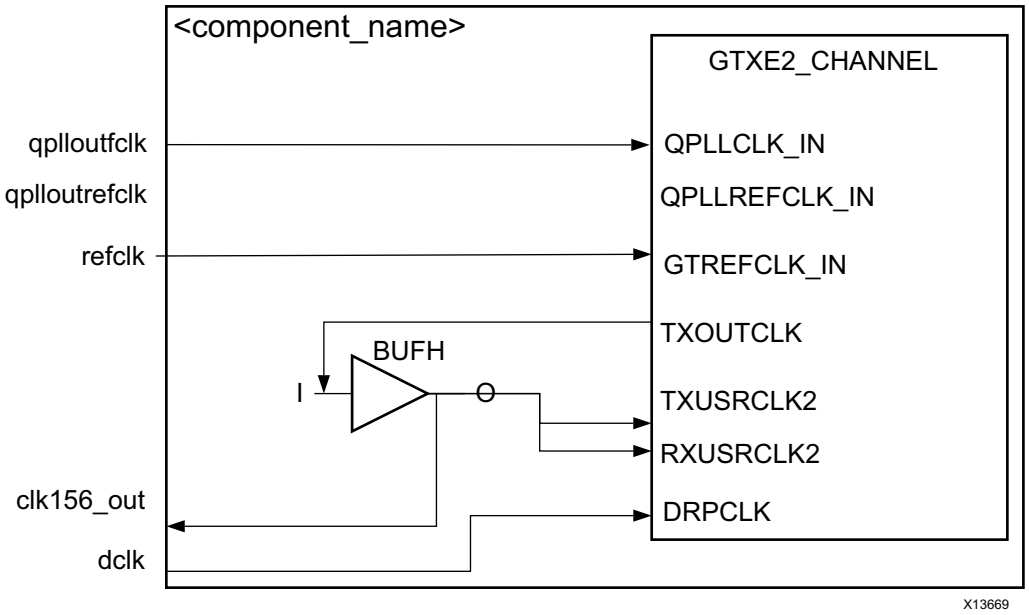

Figure 3-6: **Clock Scheme for Dune Networks RXAUI - GTX Transceivers**

Figure 3-7 shows the clocking scheme for 7 series GTP transceivers with Shared Logic included in the example design.

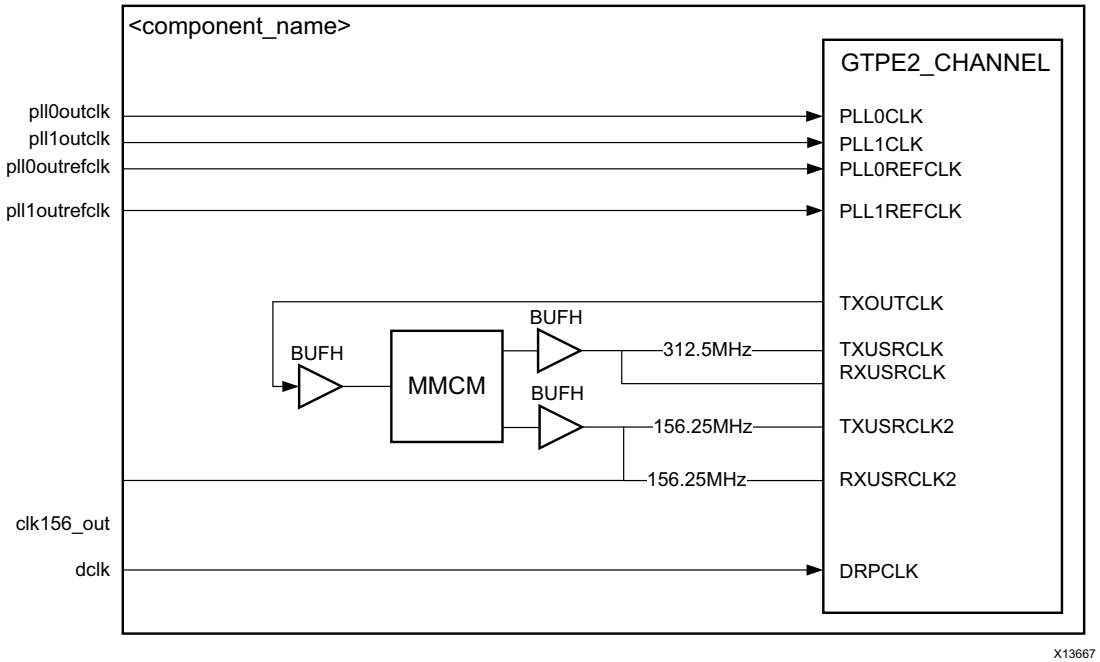

Figure 3-7: **Clock Scheme for Dune Networks RXAUI - GTP Transceivers**

Figure 3-8 shows the clocking scheme for 7 series GTH transceivers with Shared Logic included in the example design.

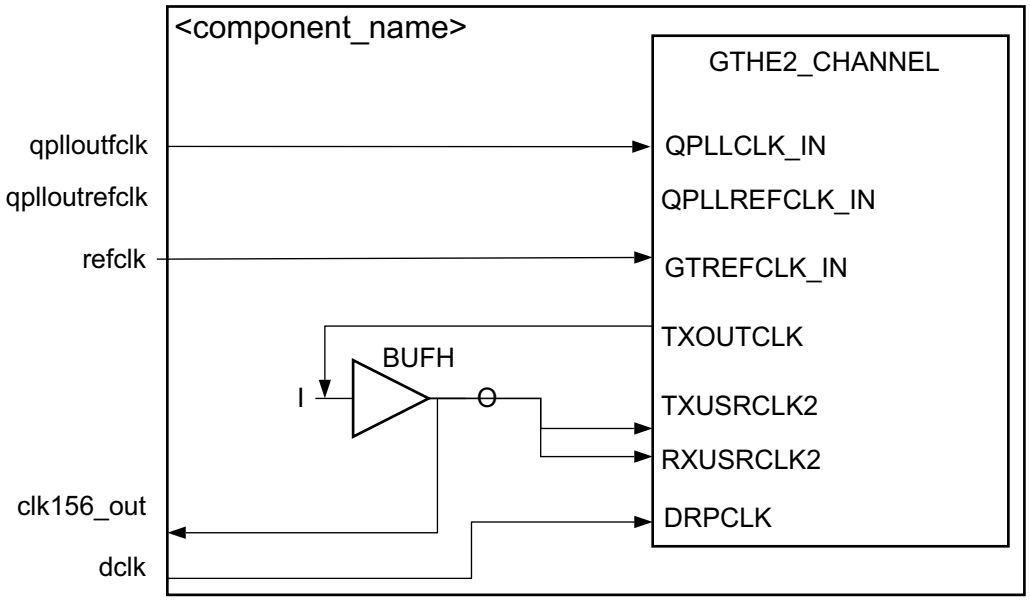

Figure 3-8: **Clock Scheme for Dune Networks RXAUI - GTH Transceivers**

Changing the clk156 Clock Buffer

The default clock buffer on TXOUTCLK is a BUFH. If you require a different clock buffer, for example a BUFG, unlink the IP and alter the HDL. The clock buffer is instanced in the `<core name>_cl_clocking.v[hd]` file.

For information about unlinking IP see the *Vivado Design Suite User Guide, Designing with IP* (UG896) [Ref 5].

Resets

See Table 2-8 for information on the reset ports. The asynchronous reset is internally synchronized to reset registers within the RXAUI core.

Design Considerations

This section describes considerations that can apply in particular design cases.

Multiple Core Instances

There are several ways to instance 2 RXAUI cores:

1. The simplest way if all transceivers are to be located in the same QUAD is to customize one RXAUI core with shared logic in the core, and the other with shared logic in the example design. The common PLL ports can then be directly connected between the two cores allowing the transceiver common PLL to be shared between the two cores.
2. For finer grained control, customize the core with shared logic in the example design. You then have to implement the common PLL in your own design, and connect it to the cores.

Due to the transceiver phase alignment procedure, `clk156` must be generated from the transceiver `txoutclk` port and is not shareable with another core instance. See the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 2] and the *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 3] for details on sharing the reference clock and any limitations.

Figure 3-9 shows two RXAUI cores, showing the ports that are connected. RXAUI_1 core has the Shared Logic included in the core and RXAUI_0 has the Shared Logic included in the example design.

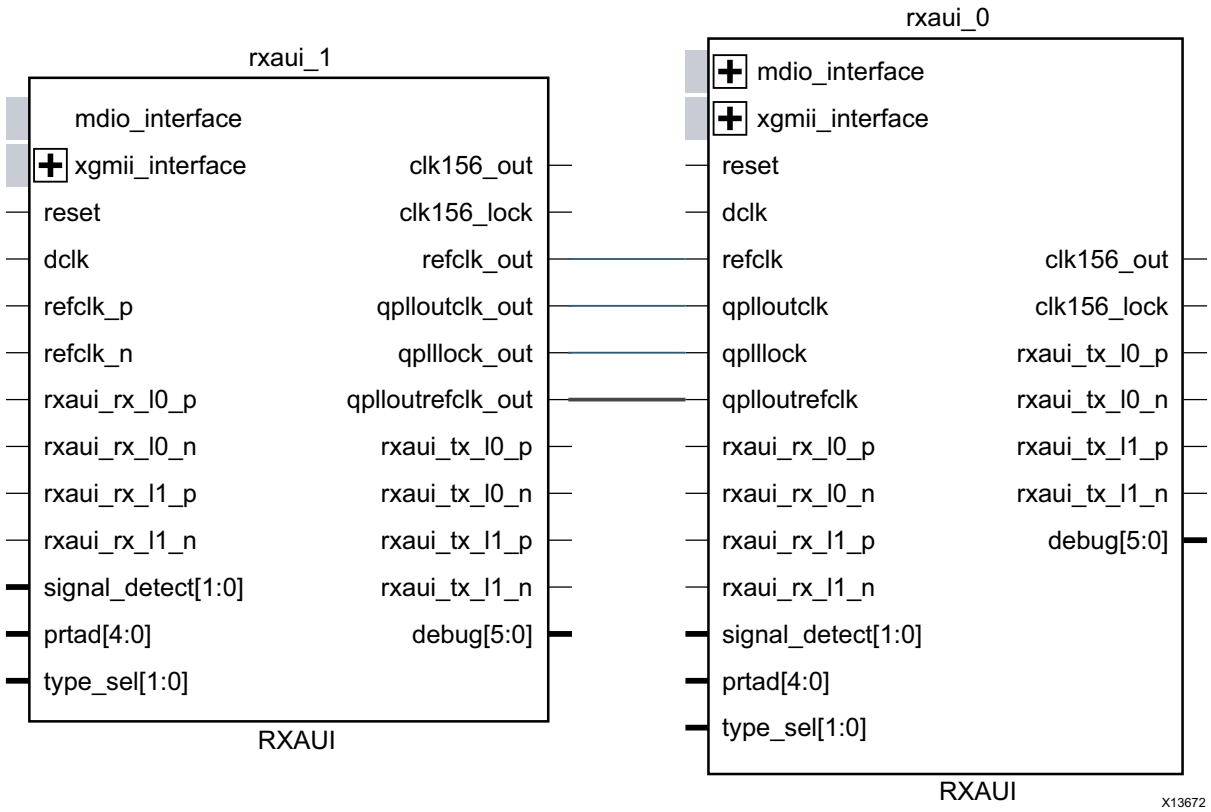

Figure 3-9: **RXAUI Cores Showing the Two Possible Shared Logic Configurations**

Receiver Termination

See the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 2] and the *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 3].

Protocol Description

Data Interface: Internal Interfaces

Internal 64-bit SDR Client-side Interface

The 64-bit single-data rate (SDR) client-side interface is based upon the 32-bit XGMII-like interface. The bus is demultiplexed from 32- bits wide to 64-bits wide on a single rising clock edge. This demultiplexing is done by extending the bus upwards so that there are now eight lanes of data numbered 0-7; the lanes are organized such that data appearing on lanes 4–7 is transmitted or received *later* in time than that in lanes 0–3.

The mapping of lanes to data bits is shown in Table 3-1. The lane number is also the index of the control bit for that particular lane; for example, `XGMII_TXC[2]` and `XGMII_TXD[23:16]` are the control and data bits respectively for lane 2.

Table 3-1: **XGMII_TXD, XGMII_RXD Lanes for Internal 64-bit Client-Side Interface**

Lane	XGMII_TXD, XGMII_RXD Bits
0	7:0
1	15:8
2	23:16
3	31:24
4	39:32
5	47:40
6	55:48
7	63:56

Definitions of Control Characters

Reference is regularly made to certain XGMII control characters signifying Start, Terminate, Error and others. These control characters all have in common that the control line for that lane is 1 for the character and a certain data byte value. The relevant characters are defined in the *IEEE Std. 802.3-2008* and are reproduced in Table 3-2 for reference.

Table 3-2: **Partial list of XGMII Characters**

Data (Hex)	Control	Name, Abbreviation
00 to FF	0	Data (D)
07	1	Idle (I)
FB	1	Start (S)
FD	1	Terminate (T)
FE	1	Error (E)

Interfacing to the Transmit Client Interface

Internal 64-bit Client-Side Interface

The timing of a data frame transmission using the internal 64-bit client-side interface is shown in Figure 3-10. The beginning of the data frame is shown by the presence of the Start character (the /S/ codegroup in lane 4 of Figure 3-10) followed by data characters in lanes 5, 6, and 7. Alternatively the start of the data frame can be marked by the occurrence of a Start character in lane 0, with the data characters in lanes 1 to 7.

When the frame is complete, it is completed by a Terminate character (the T in lane 1 of Figure 3-10). The Terminate character can occur in any lane; the remaining lanes are padded by XGMII idle characters.

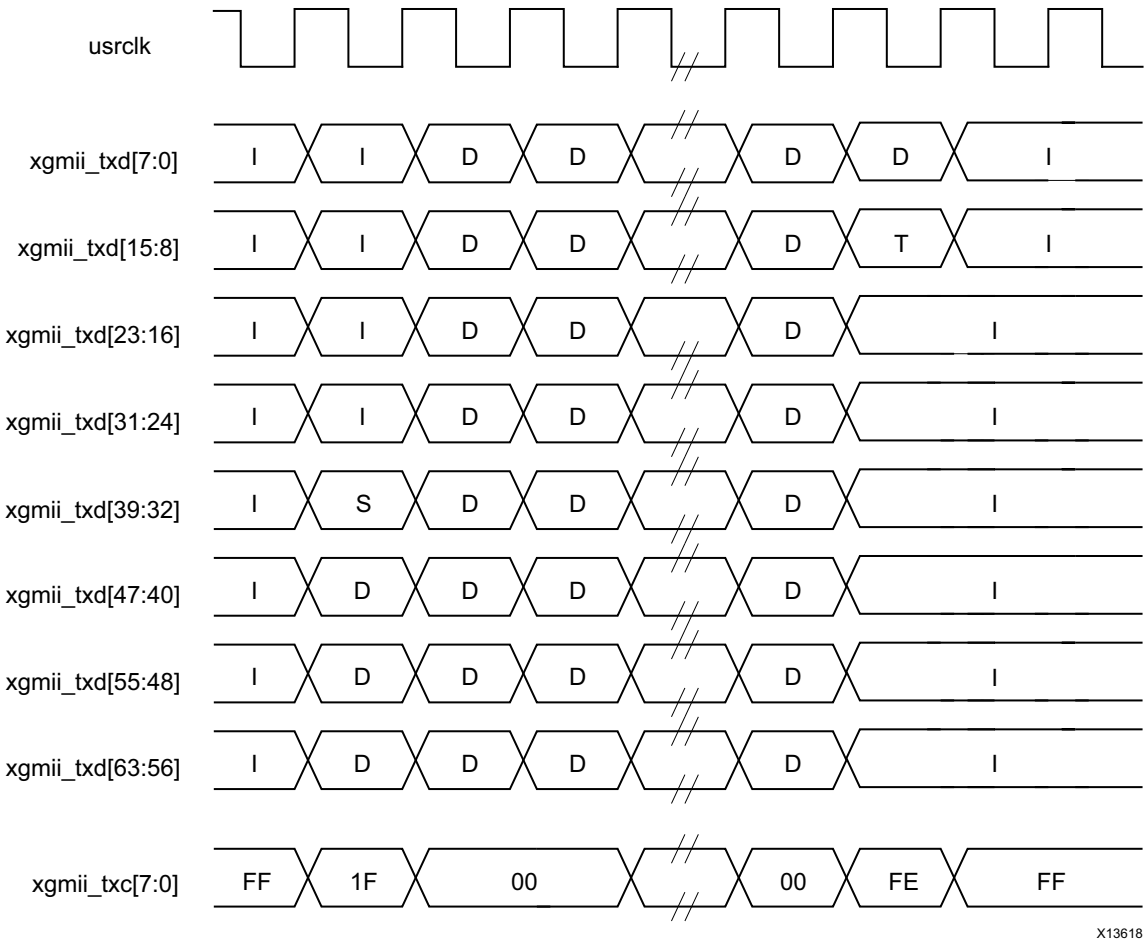

Figure 3-10: **Normal Frame Transmission Across the Internal 64-bit Client-Side I/F**

Figure 3-11 depicts a similar frame to that in Figure 3-10, with the exception that this frame is propagating an error. The error code is denoted by the letter E, with the relevant control bits set.

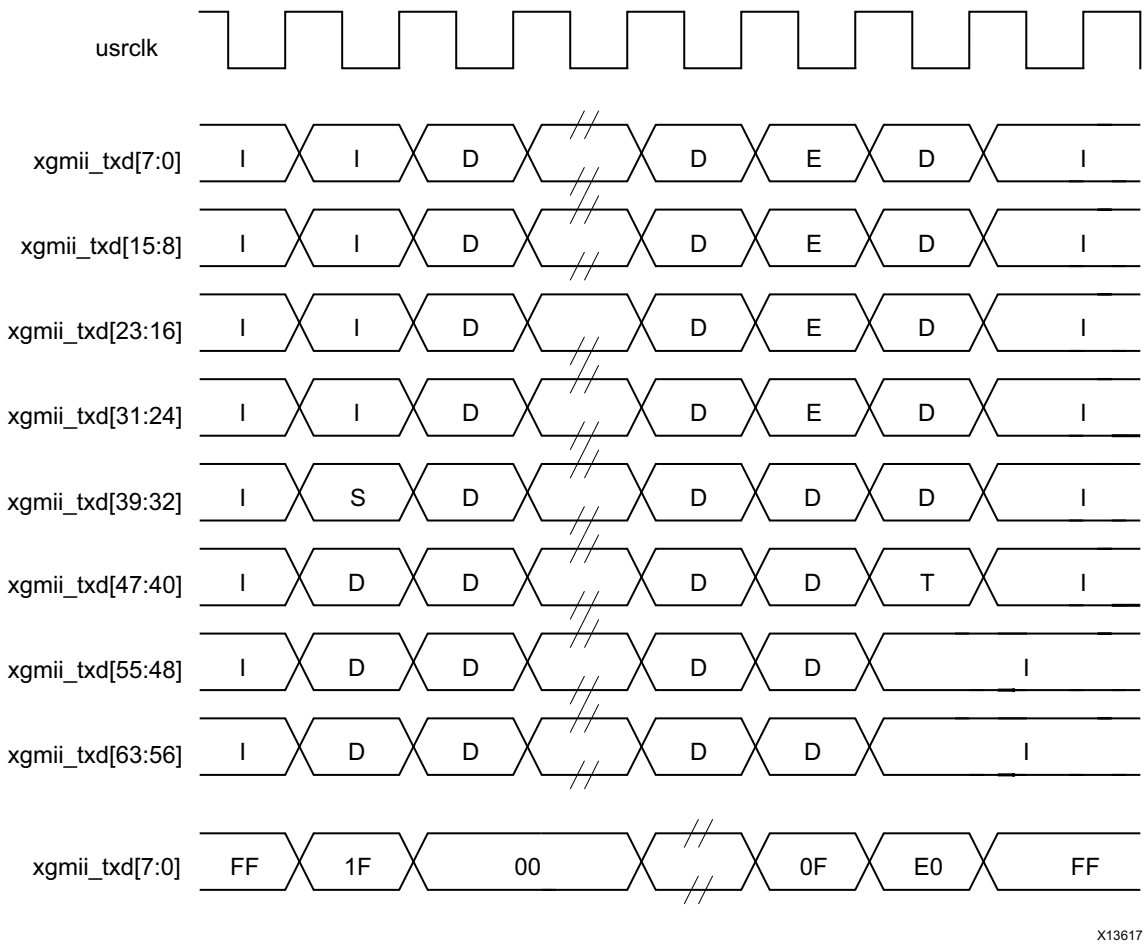

Figure 3-11: **Frame Transmission with Error Across Internal 64-bit Client-Side I/F**

Interfacing to the Receive Client Interface

Internal 64-bit Client-Side Interface

The timing of a normal inbound frame transfer is shown in Figure 3-12. As in the transmit case, the frame is delimited by a Start character (S) and by a Terminate character (T). The Start character in this implementation can occur in either lane 0 or in lane 4. The Terminate character, T, can occur in any lane.

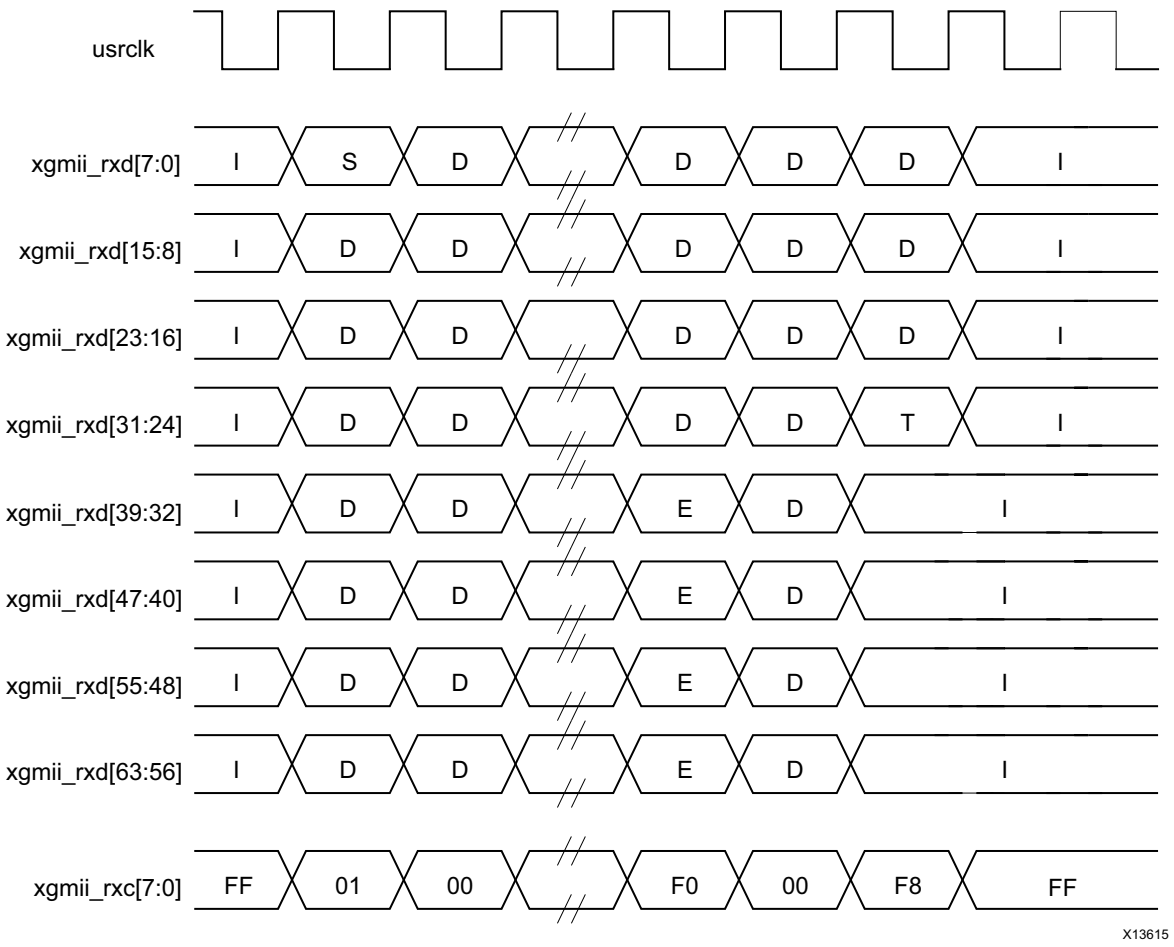

Figure 3-12: **Frame Reception Across the Internal 64-bit Client Interface**

Figure 3-13 shows an inbound frame of data propagating an error. In this instance, the error is propagated in lanes 4 to 7, shown by the letter E.

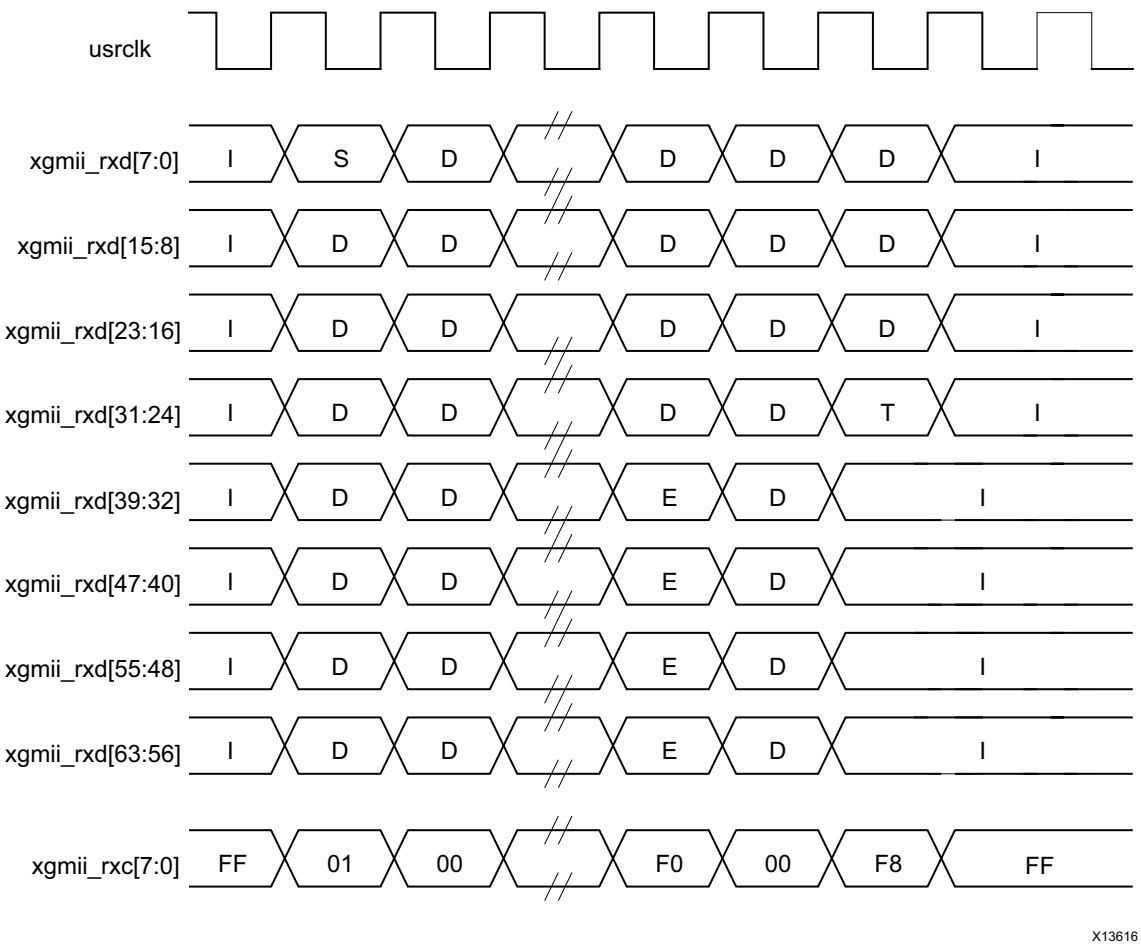

Figure 3-13: **Frame Reception with Error Across the Internal 64-bit Client Interface**

MDIO Interface

The Management Data Input/Output (MDIO) interface is a simple, low-speed 2-wire interface for management of the RXAUI core consisting of a clock signal and a bidirectional data signal. It is defined in clause 45 of I*EEE Standard 802.3-2008*.

An MDIO bus in a system consists of a single Station Management (STA) master management entity and several MDIO Managed Device (MMD) slave entities. Figure 3-14 illustrates a typical system. All transactions are initiated by the STA entity. The RXAUI core implements an MMD.

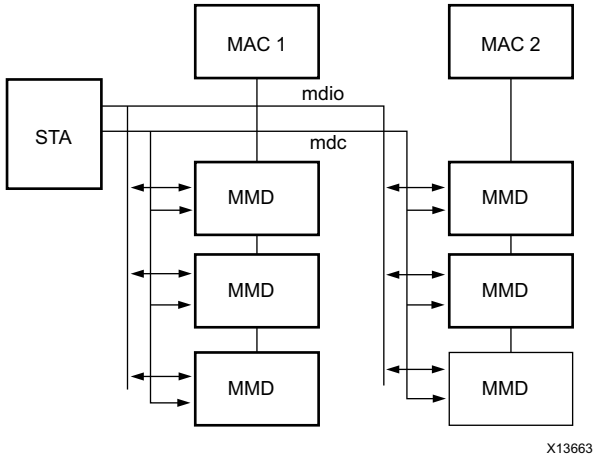

Figure 3-14: **A Typical MDIO-Managed System**

If implemented, the MDIO interface is implemented as four unidirectional signals. These can be used to drive a 3-state buffer either in the FPGA SelectIO™ interface buffer or in a separate device.

The `type_sel` port is registered into the core at FPGA configuration and core hard reset; changes after that time are ignored by the core. Table 3-3 shows the mapping of the `type_sel` setting to the implemented register map.

Table 3-3: **Mapping of type_sel Port Settings to MDIO Register Type**

type_sel setting	MDIO Register	Description
00 or 01	10GBASE-X PCS/PMA	When driving a 10GBASE-X PHY
10	DTE XGXS	When connected to a 10GMAC through XGMII
11	PHY XGXS	When connected to a PHY through XGMII

The `prtad[4:0]` port sets the port address of the core instance. Multiple instances of the same core can be supported on the same MDIO bus by setting the `prtad[4:0]` to a unique value for each instance; the RXAUI core ignores transactions with the PRTAD field set to a value other than that on its `prtad[4:0]` port.

MDIO Transactions

The MDIO interface should be driven from a STA master according to the protocol defined in *IEEE Std. 802.3-2008*. An outline of each transaction type is described in the following sections. In these sections, these abbreviations apply:

- PRE: preamble
- ST: start
- OP: operation code
- PRTAD: port address

- DEVAD: device address
- TA: turnaround

Set Address Transaction

Figure 3-15 shows an Address transaction defined by OP = 00. Set Address is used to set the internal 16-bit address register of the RXAUI core for subsequent data transactions (called the current address in the following sections).

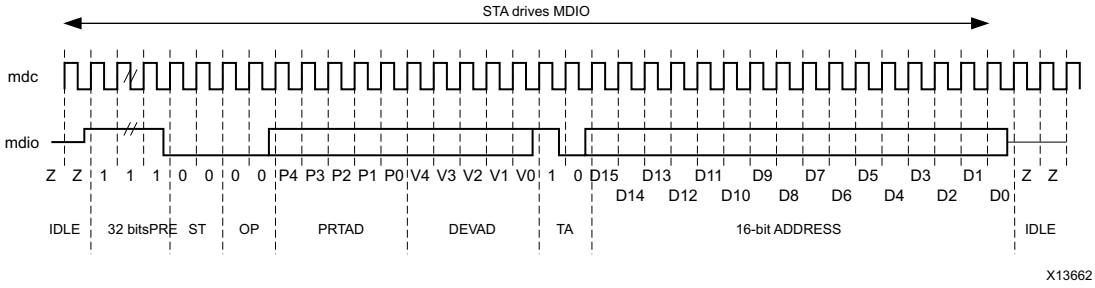

Figure 3-15: **MDIO Set Address Transaction**

Write Transaction

Figure 3-16 shows a Write transaction defined by OP = 01. The RXAUI core takes the 16-bit word in the data field and writes it to the register at the current address.

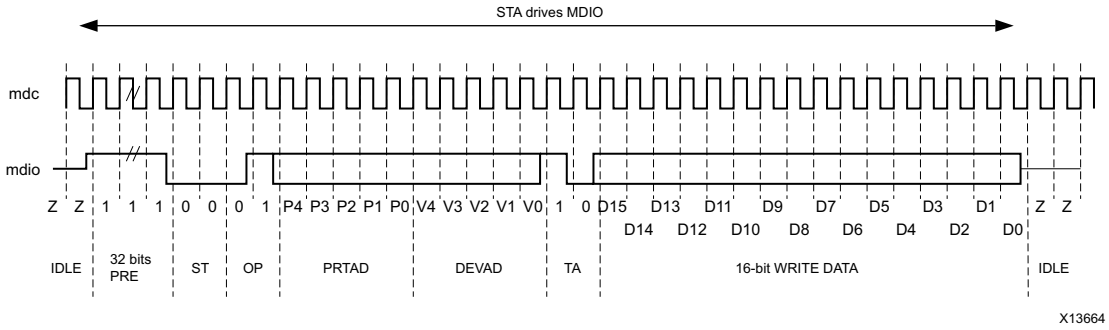

Figure 3-16: **MDIO Write Transaction**

Read Transaction

Figure 3-17 shows a Read transaction defined by OP = 11. The RXAUI core returns the 16-bit word from the register at the current address.

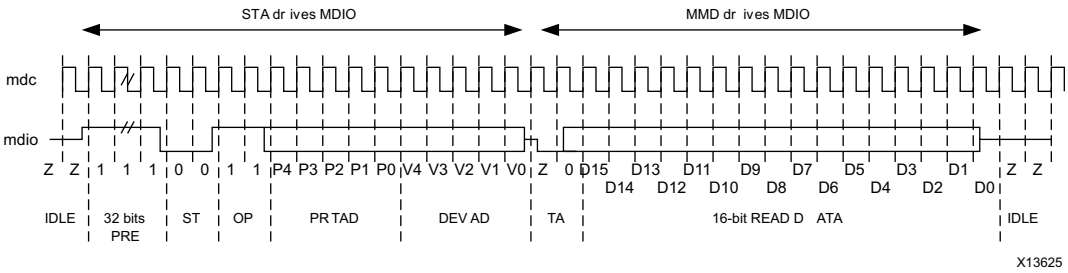

Figure 3-17: **MDIO Read Transaction**

Post-Read-increment-address Transaction

Figure 3-18 shows a Post-read-increment-address transaction, defined by OP = 10. The RXAUI core returns the 16-bit word from the register at the current address then increments the current address. This allows sequential reading or writing by a STA master of a block of register addresses.

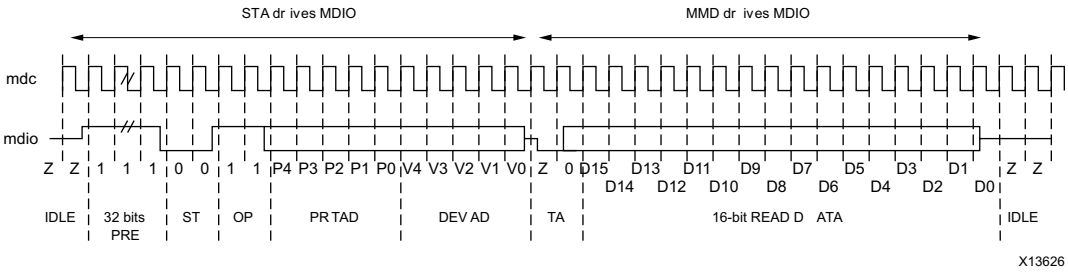

Figure 3-18: **MDIO Read-and-increment Transaction**

For detail on the MDIO registers, see MDIO Interface Registers.

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado® Design Suite environment.

If you are customizing the generating the core in the Vivado IP Integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4] for detailed information.

Vivado Integrated Design Environment

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click on the selected IP or select the Customize IP command from the toolbar or popup menu.

For details, see the sections, "Working with IP" and "Customizing IP for the Design" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5] and the "Working with the Vivado IDE" section in the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 6].

Note: Figures in this chapter are illustrations of the RXAUI core GUI in the Vivado Integrated Design Environment (IDE). This layout might vary from the current version.

Figure 4-1 displays the main screen for customizing the RXAUI core.

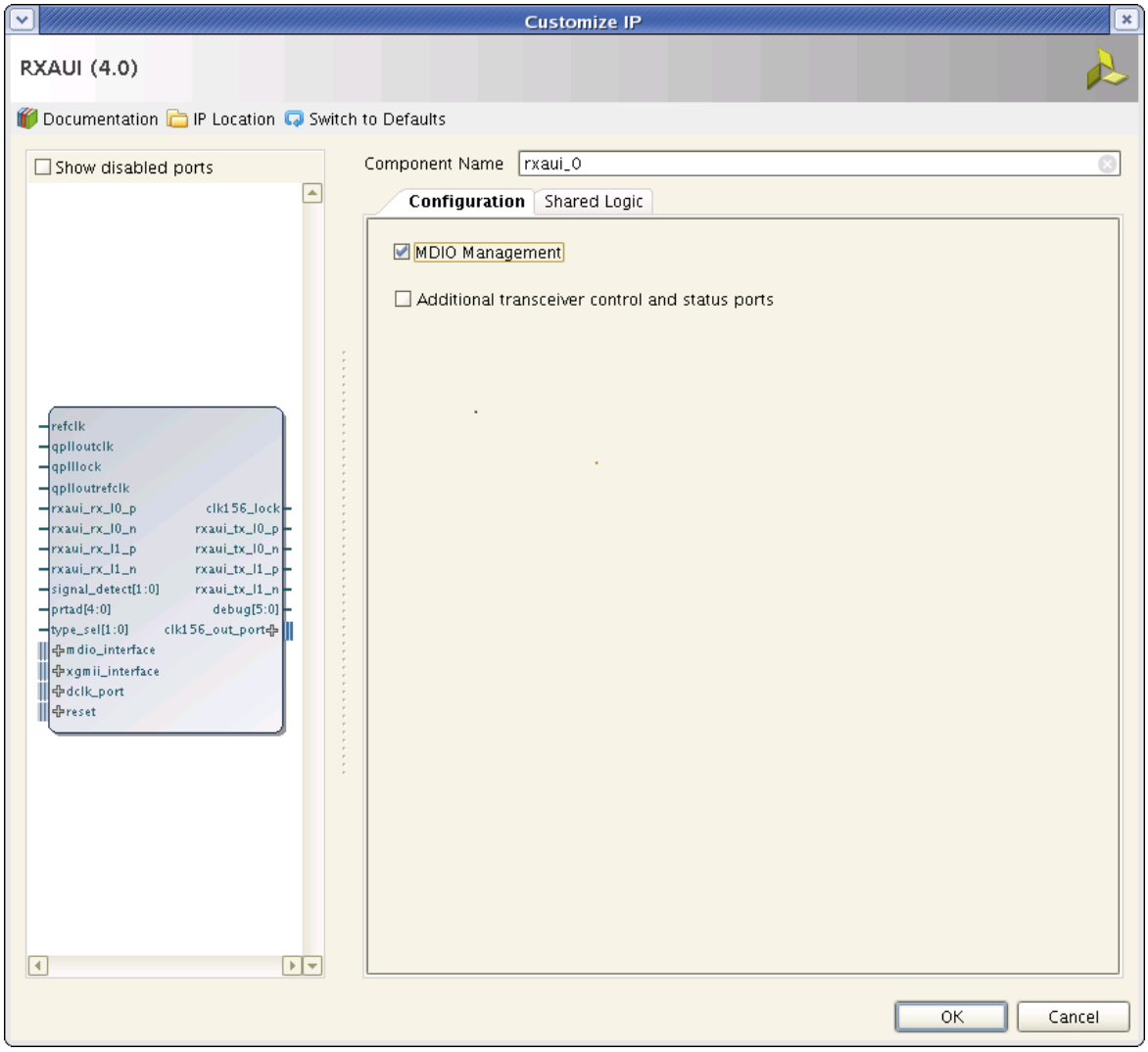

Figure 4-1: **RXAUI Main Screen**

For general help with starting and using the Vivado GUI, see the documentation supplied with the Vivado Design Suite.

Component Name

The component name is used as the base name of the output files generated for the core. Names must begin with a letter and must be composed from the following characters: a through z, 0 through 9 and "_" (underscore).

MDIO Management

Select this option to implement the MDIO interface for managing the core. Deselect the option to remove the MDIO interface and expose a simple bit vector to manage the core.

The default is to implement the MDIO interface.

Additional Transceiver Control and Status Ports

Select if GT control and status ports such as DRP, PRBS, RX Equalizer and TX Driver are required.

Shared Logic

Select whether the Transceiver Quad PLL and differential reference clock buffer is included in the core itself or in the example design (see Shared Logic for more information).

Output Generation

For details, see "Generating IP Output Products" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5]

Constraining the Core

This chapter describes how to constrain a design containing the RXAUI core. An XDC file is applied to the core instance. This XDC is available through the **IP Sources** view under **Synthesis**. No modification is required to this file.

There are some additional constraints required that are design specific such as transceiver location constraints. These are detailed in this chapter and an example of such constraints can be found in the example design. See Chapter 8, Detailed Example Design, for a complete description of the Vivado Design Suite output files.

CAUTION! *Not all constraints are relevant to specific implementations of the core; consult the XDC created with the core instance to see exactly what constraints are relevant.*

Required Constraints

This section defines the additional constraint requirements for the core. Constraints are provided with an XDC file. An XDC is provided with the HDL example design to give a starting point for constraints for your design. The following constraints are required.

Clock Frequencies

DCLK should be specified:

```
create_clock -name dclk -period 20.000 [get_ports dclk]
```

This constraint defines the frequency of DCLK that is supplied to the transceivers. The example design uses a nominal 50 MHz clock.

Clock Management

The Dune Networks RXAUI core has two clock domains:

- The `clk156` domain derived from the TXOUTCLK output of the transceiver.
- The core XDC applies a `create_clock` that propagates to the clk156_out output port.
- The `dclk` domain. This must be constrained outside of the core as described in Clock Frequencies.

Transceiver Placement

To constrain the placement of the transceivers using X0Y0 terminology the following constraints should be used.

Shared Logic in Example Design

7 Series GTH Transceivers

```
set_property LOC GTHE2_CHANNEL_X0Y0 [get_cells rxaui_support_i/rxaui_i/*/
gt0_wrapper_i/gthe2_i]
set_property LOC GTHE2_CHANNEL_X0Y1 [get_cells rxaui_support_i/rxaui_i/*/
gt1_wrapper_i/gthe2_i]
```

7 Series GTX Transceivers

```
set_property LOC GTXE2_CHANNEL_X0Y0 [get_cells rxaui_support_i/rxaui_i/*/
gt0_wrapper_i/gtxe2_i]
set_property LOC GTXE2_CHANNEL_X0Y1 [get_cells rxaui_support_i/rxaui_i/*/
gt1_wrapper_i/gtxe2_i]
```

7 Series GTP Transceivers

```
set_property LOC GTPE2_CHANNEL_X0Y0 [get_cells rxaui_support_i/rxaui_i/*/
gt0_wrapper_i/gtpe2_i]
set_property LOC GTPE2_CHANNEL_X1Y0 [get_cells rxaui_support_i/rxaui_i/*/
gt1_wrapper_i/gtpe2_i]
```

Shared Logic in Core

7 Series GTH Transceivers

```
set_property LOC GTHE2_CHANNEL_X0Y0 [get_cells rxaui_i/rxaui_block_i/*/
gt0_wrapper_i/gthe2_i]
set_property LOC GTHE2_CHANNEL_X0Y1 [get_cells rxaui_i/rxaui_block_i/*/
gt1_wrapper_i/gthe2_i]
```

7 Series GTX Transceivers

```
set_property LOC GTXE2_CHANNEL_X0Y0 [get_cells rxaui_i/rxaui_block_i/*/
gt0_wrapper_i/gtxe2_i]
set_property LOC GTXE2_CHANNEL_X0Y1 [get_cells rxaui_i/rxaui_block_i/*/
gt1_wrapper_i/gtxe2_i]
```

7 Series GTP Transceivers

```
set_property LOC GTPE2_CHANNEL_X0Y0 [get_cells rxaui_i/rxaui_block_i/*/
gt0_wrapper_i/gtpe2_i]
set_property LOC GTPE2_CHANNEL_X1Y0 [get_cells rxaui_i/rxaui_block_i/*/
gt1_wrapper_i/gtpe2_i]
```

Simulation

Simulation of the RXAUI solution at the core level is not supported without the addition of a test bench (not supplied). Simulation of the example design is supported.

For comprehensive information about Vivado simulation components, as well as information about using supported third party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 7].

Synthesis and Implementation

The RXAUI solution this is a mix of both encrypted and unencrypted source. Only the unencrypted sources are visible and optionally editable by using the Unlink IP Vivado option.

For details about synthesis and implementation, see “Synthesizing IP” and “Implementing IP” in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5].

Detailed Example Design

This chapter provides information about the example design, including a description of the files and the directory structure generated by the Xilinx Vivado® Design Suite, the purpose and contents of the provided scripts, the contents of the example HDL wrappers, and the operation of the demonstration test bench.

Example Design

Figure 8-1 illustrates the clock and reset enabled configuration of the example design.

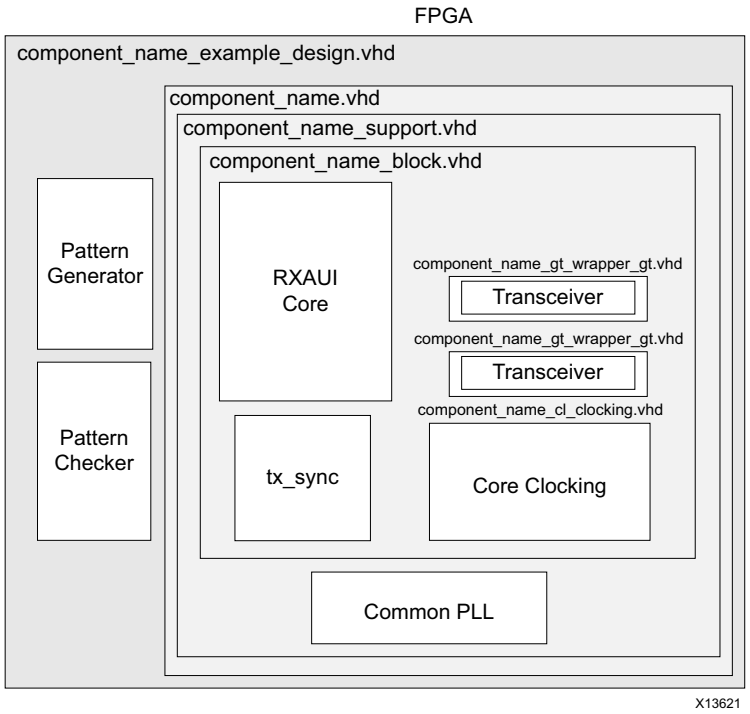

Figure 8-1: **RXAUI Example Design (Shared Logic in Core) and Test Bench – Clock and Reset Enabled**

The RXAUI example design consists of the following:

- Clock buffers for `DCLK`
- Simple XGMII pattern generator and checker
- An instance of the core (Shared Logic included in the core) or the support level module which contains the core, common PLL, and shared reset module

The RXAUI Design Example has been tested with Xilinx Vivado® Design Suite and Mentor Graphics Questa® SIM (the versions of these tools are available in the Xilinx Design Tools: Release Notes Guide.

Test Bench

The example design demonstration test bench is a simple VHDL or Verilog program to exercise the example design and the core itself. It simulates an instance of the example design that is externally looped back. It generates all the required clocks and resets and waits for successful pattern checking to complete. If it fails to detect successful pattern checking within the time limit defined in the test bench, it produces an error.

Verification, Compliance, and Interoperability

The RXAUI core has been verified using both simulation and hardware testing.

Simulation

A highly parameterizable transaction-based simulation test suite has been used to verify the core. Tests included:

- Register access over MDIO
- Loss and re-gain of synchronization
- Loss and re-gain of alignment
- Frame transmission
- Frame reception
- Clock compensation
- Recovery from error conditions

Hardware Testing

The core has been used in several hardware test platforms within Xilinx. In particular, the core has been used in a test platform design with the Xilinx 10-Gigabit Ethernet MAC core. This design comprises the MAC, RXAUI, a ping loopback FIFO, and a test pattern generator all under embedded MicroBlaze™ processor control. This design has been used for interoperability testing at Dune Networks.

Migrating and Upgrading

This appendix contains information about migrating a design from ISE® to the Vivado® Design Suite, and for upgrading to a more recent version of the IP core. For customers upgrading in the Vivado Design Suite, important details (where applicable) about any port changes and other impact to user logic are included.

Migrating to the Vivado Design Suite

For information on migrating from Xilinx ISE® Design Suite tools to the Vivado® Design Suite, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 8].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when you upgrade from RXAUI v3.0 to RXAUI v4.0 in the Vivado Design Suite.

"Include common clocking and resets" is now mapped to "Include shared logic in core". If this option was previously off this now maps to "Include shared logic in example design".

Parameter Changes

The WRAPPER_SIM_GTRESET_SPEEDUP parameter has been removed.

Port Changes

Table B-1 shows the ports that have been added, removed, or re-named between RXAUI v3.0 and RXAUI v4.0.

Table B-1: **Port Changes**

Added	Removed	Notes
clk156_out (output)	clk156 (input)	clk156_out is a clock output that replaces the txoutclk and clk156 pins. It is driven by a BUFH. As before, this clock is not shared with another RXAUI core instance. Remove any clock buffer you had instanced previously in your design.
	txoutclk (output)	
	reset156 (input)	The core now generates its synchronous reset internally.
	mmcm_lock (input)	
	clk312 (input) (GTP only)	The MMCM is located inside the core.
	gt_control (input vector)	Replaced by individual transceiver control pins.
clk156_lock	txlock	txlock output re-named as clk156_lock
debug		This output vector has been resized to 6 bits wide. These bits map to the old debug vector [5:0]. Individual transceiver ports have replaced the removed bits.
refclkout (output)		GTX/GTH: When "Shared logic in core" is selected, refclkout is a new output port than can be connected to the refclk input port of another core.

DRP Ports

Table B-2 shows the re-naming of DRP ports between versions 3.0 and 4.0.

Table B-2: **DRP Port Name Changes**

3.0	4.0
3.0 drp0_addr	gt0_drpaddr
drp0_en	gt0_drpen
drp0_i	gt0_drpdi
drp0_o	gt0_drpdo
drp0_rdy	gt0_drprdy
drp0_we	gt0_drpwe
drp0_busy	gt0_drp_busy (GTP only)
drp1_addr	gt1_drpaddr
drp1_en	gt1_drpen
drp1_i	gt1_drpdi
drp1_o	gt1_drpdo
drp1_rdy	gt1_drprdy
drp1_we	gt1_drpwe
drp1_busy	gt1_drp_busy (GTP only)

QPLL Ports

Table B-3 and Table B-4 shows the re-naming of QPLL ports (GTX/GTH only) between versions 3.0 and 4.0.

Table B-3: **QPLL Port Name Changes (Shared Logic in Core)**

3.0	4.0
common_pll_clk	qplloutclk_out
common_pll_lock	qplllock_out
common_pll_refclk	qplloutrefclk_out

Table B-4: **QPLL Port Name Changes (Shared Logic in Example Design)**

3.0	4.0
common_pll_clk	qplloutclk
common_pll_lock	qplllock
common_pll_refclk	qplloutrefclk

GTP Ports

Table B-5 and Table B-6 shows the re-naming of GTP ports between versions 3.0 and 4.0.

Table B-5: **GTPE2_COMMON Port Name Changes (Shared Logic in Core)**

3.0	4.0
common_pll0_clk	pll0outclk_out
common_pll0_lock	pll0lock_out
common_pll0_refclk	pll0outrefclk_out
common_pll1_clk	pll1outclk_out
common_pll1_refclk	pll1outrefclk_out

Table B-6: **GTPE2_COMMON Ports (Shared Logic in Example Design)**

3.0	4.0
common_pll0_clk	pll0outclk
common_pll0_lock	pll0lock
common_pll0_refclk	pll0refclk
common_pll1_clk	pll1outclk
common_pll1_refclk	pll1outrefclk

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the RXAUI, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for opening a Technical Support WebCase.

Documentation

This product guide is the main document associated with the RXAUI. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

The Solution Center specific to the RXAUI core is listed below.

- Xilinx Ethernet IP Solution Center

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product.

Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the RXAUI

AR: 54249

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Additional Resources.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Login to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address RXAUI design issues. It is important to know which tools are useful for debugging various situations.

Link Analyzers

Link Analyzers can be used to generate and analyzer traffic for hardware debug and testing. Common link analyzers include:

- SMARTBITS
- IXIA

Vivado Lab Tools

Vivado® inserts logic analyzer and virtual I/O cores directly into your design. Vivado lab tools allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature represents the functionality in the Vivado IDE that is used for logic debugging and validation of a design running in Xilinx devices in hardware.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

The RXAUI core has useful signals that have the `MARK_DEBUG` attribute applied to them. This shows up as debug nets within Vivado.

See *Vivado Design Suite User Guide, Programming and Debugging* (UG908) [Ref 9].

Simulation Debug

The simulation debug flow for Questa® SIM is illustrated in Figure C-1. A similar approach can be used with other simulators.

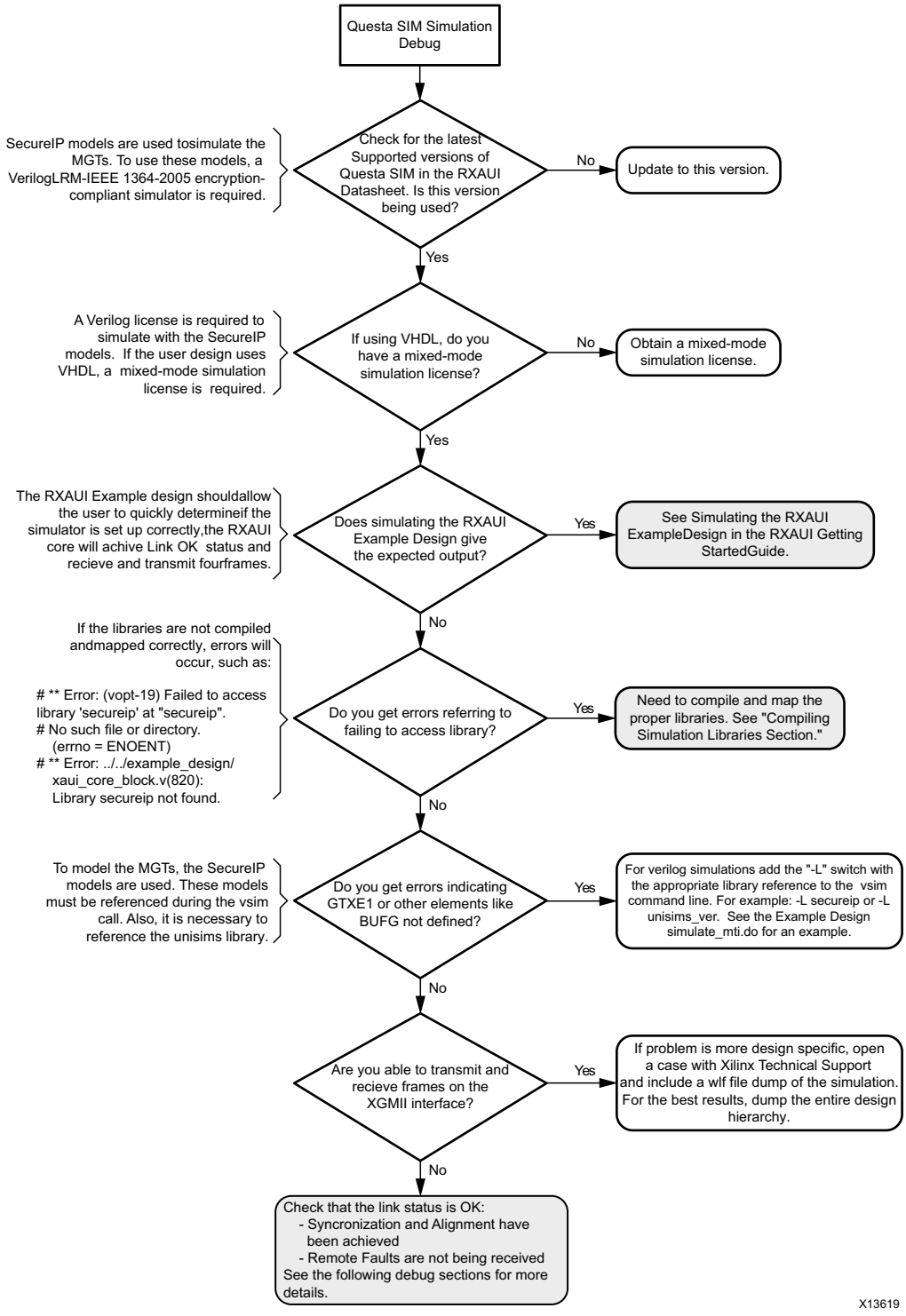

Figure C-1: **Questa SIM Debug Flow Diagram**

Compiling Simulation Libraries

To run simulation with third-party simulators, it is necessary to compile the Xilinx Simulation Libraries. For full details on how to perform this, see Appendix B of the *Vivado Design Suite User Guide, Logic Simulation* (UG900) [Ref 7].

If the debug suggestions listed previously do not resolve the issue, open a support case. See Contacting Technical Support for information on how to do this.

To discuss possible solutions, use the Xilinx User Community: forums.xilinx.com/xlnx/

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado Analyzer tool is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the Vivado Analyzer tool for debugging the specific problems. Many of these common issues can also be applied to debugging design simulations.

General Checks

Ensure that all the timing constraints for the core were met during Place and Route.

- Does it work in timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue.
- Ensure that all clock sources are clean. If using DCMs in the design, ensure that all DCMs have obtained lock by monitoring the LOCKED port.

Monitoring the RXAUI Core with Vivado Lab Tools

- The RXAUI core has the `MARK_DEBUG` attribute applied to the signal for debugging and checking the status of the RXAUI core and transceivers for easy access to adding these to the Vivado logic analyzer.
- A debug port is also provided so it can connect to external logic for debug (for example, processor monitoring). This port contains transceiver and core debug information.
- XGMII signals and signals between RXAUI core and the transceiver can be added to monitor data transmitted and received. See Table 2-4, page 10 and Table 2-8, page 11 for a list of signal names.
- Status signals added to check status of link: `STATUS_VECTOR[7:0]`, `ALIGN_STATUS`, `SYNC_STATUS`, and Debug port Bits[5:0].

- To interpret control codes in on the XGMII interface or the interface to the transceiver, see Table C-1 and Table C-2.
- An Idle (0x07) on the XGMII interface is encoded to be a randomized sequence of /K/ (Sync), /R/ (Skip), /A/(Align) codes on the RXAUI interface. For details on this encoding, see the IEEE 802.3-2008 specification (section 48.2.4.2) for more details.

Table C-1: **XGMII Control Codes**

TXC	TXD	Description
0	0x00 through 0xFF	Normal data transmission
1	0x07	Idle
1	0x9C	Sequence
1	0xFB	Start
1	0xFD	Terminate
1	0xFE	Error

Table C-2: **RXAUI Control Codes**

Codegroup	8-bit Value	Description
Dxx.y	**0xXX**	Normal data transmission
K28.5	0xBC	/K/ (Sync)
K28.0	0x1C	/R/ (Skip)
K28.3	0x7C	/A/ (Align)
K28.4	0x9C	/Q/ (Sequence)
K27.7	0xFB	/S/ (Start)
K29.7	0xFD	/T/ (Terminate)
K30.7	0xFE	/E/ (Error)

Issues with Data Reception or Transmission

Issues with data reception or transmission can be caused by a wide range of factors. Following is a flow diagram of steps to debug the issue. Each of the steps are discussed in more detail in the following sections.

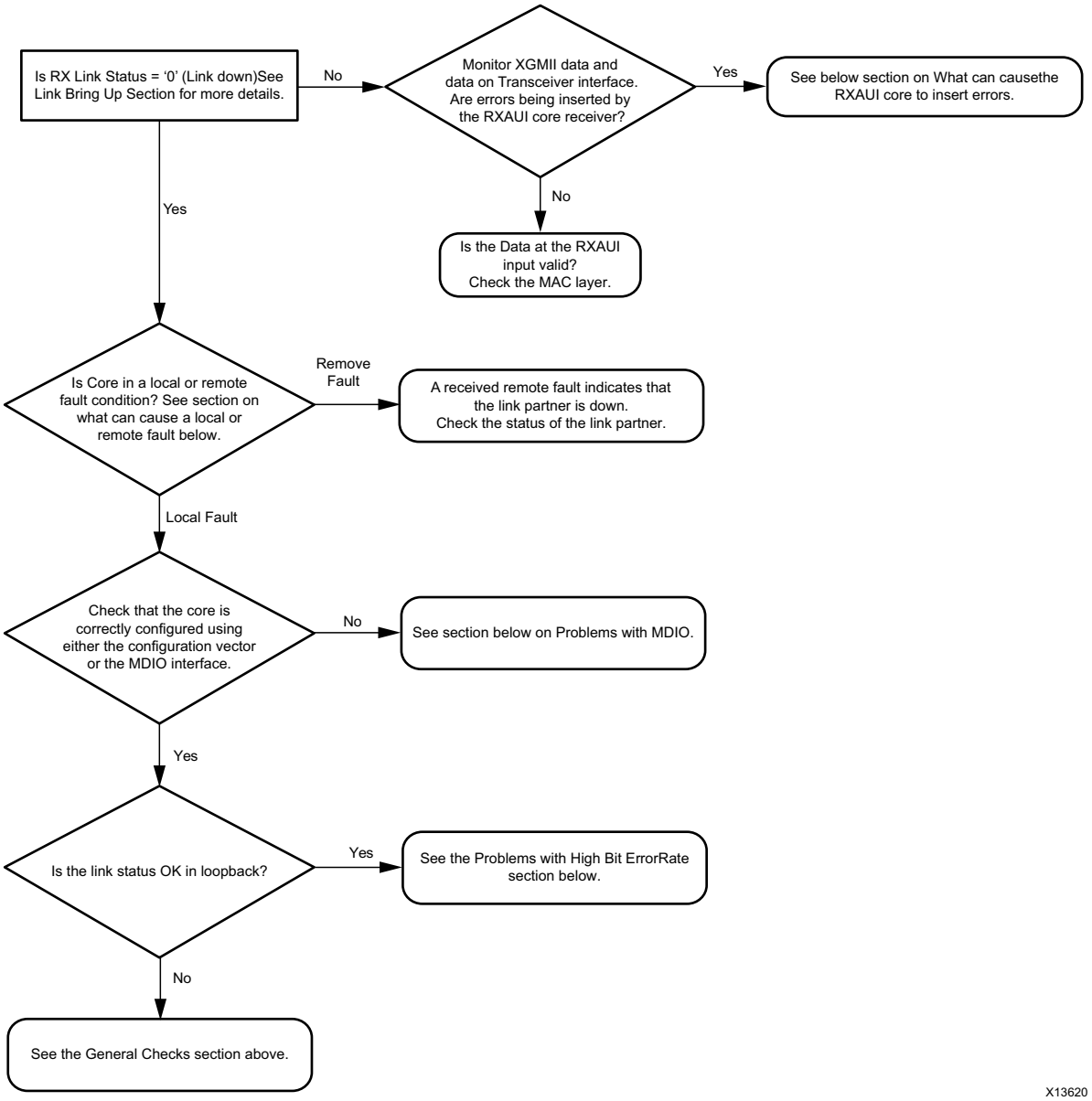

Figure C-2: **Flow Diagram for Debugging Problems with Data Reception or Transmission**

What Can Cause a Local or Remote Fault?

Local Fault and Remote Fault codes both start with the sequence TXD/RXD = 0x9C, TXC/RXC = 1 in XGMII lane 0. Fault conditions can also be detected by looking at the status vector or MDIO registers. The Local Fault and Link Status are defined as latching error indicators by the IEEE specification. This means that the Local Fault and Link Status bits in the status vector or MDIO registers must be cleared with the Reset Local Fault bits and Link Status bits in the Configuration vector or MDIO registers.

Local Fault

The receiver outputs a local fault when the receiver is not up and operational. This RX local fault is also indicated in the status and MDIO registers. The most likely causes for an RX local fault are:

- The transceiver has not locked or the receiver is being reset.
- At least one of the lanes is not synchronized – `SYNC_STATUS`
- The lanes are not properly aligned – `ALIGN_STATUS`

Note: The `SYNC_STATUS` and `ALIGN_STATUS` signals are not latching.

A TX local fault is indicated in the status and MDIO registers when the transceiver transmitter is in reset or has not yet completed any other initialization or synchronization procedures needed.

Remote Fault

Remote faults are only generated in the MAC reconciliation layer in response to a Local Fault message. When the receiver receives a remote fault, this means that the link partner is in a local fault condition.

When the MAC reconciliation layer receives a remote fault, it silently drops any data being transmitted and instead transmit IDLEs to help the link partner resolve its local fault condition. When the MAC reconciliation layer receives a local fault, it silently drops any data being transmitted and instead transmit a remote fault to inform the link partner that it is in a fault condition. Be aware that the Xilinx 10GEMAC core has an option to disable remote fault transmission.

Link Bring Up

The following link initialization stages describe a possible scenario of the Link coming up between device A and device B.

Stage 1: Device A Powered Up, but Device B Powered Down

- Device A is powered up and reset.
- Device B powered down
- Device A detects a fault because there is no signal received. The Device A RXAUI core indicates an RX local fault.
- The Device A MAC reconciliation layer receives the local fault. This triggers the MAC reconciliation layer to silently drop any data being transmitted and instead transmit a remote fault.
- RX Link Status = 0 (link down) in Device A

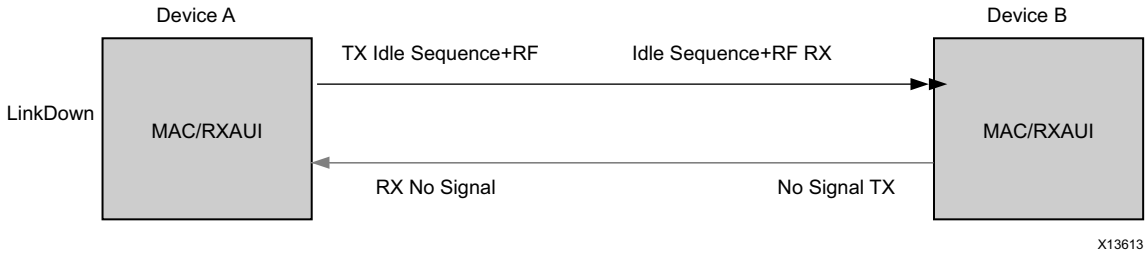

Figure C-3: **Device A Powered Up, but Device B Powered Down**

Stage 2: Device B Powers Up and Resets

- Device B Powers Up and Resets.
- Device B RXAUI completes Synchronization and Alignment.
- Device A has not synchronized and aligned yet. It continues to send remote faults.
- Device B RXAUI passes received remote fault to MAC.
- Device B MAC reconciliation layer receives the remote fault. It silently drops any data being transmitted and instead transmits IDLEs.
- Link Status = 0 (link down) in both A and B.

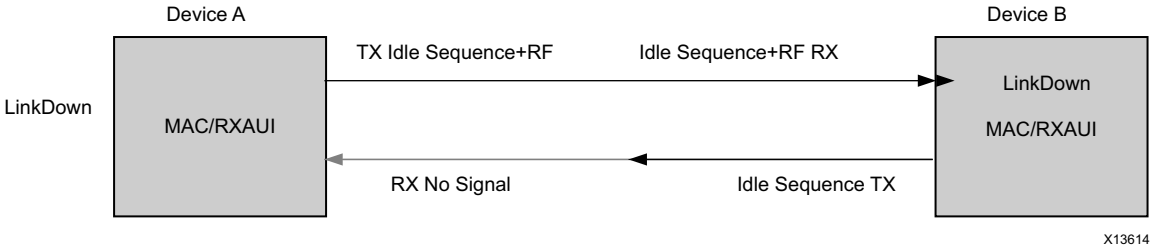

Figure C-4: **Device B Powers Up and Resets**

Stage 3: Device A Receives Idle Sequence

- Device A RXAUI RX detects idles, synchronizes and aligns.
- Device A reconciliation layer stops dropping frames at the output of the MAC transmitter and stops sending remote faults to Device B.
- Device A Link Status = 1 (Link Up)
- After Device B stops receiving the remote faults, normal operation starts.

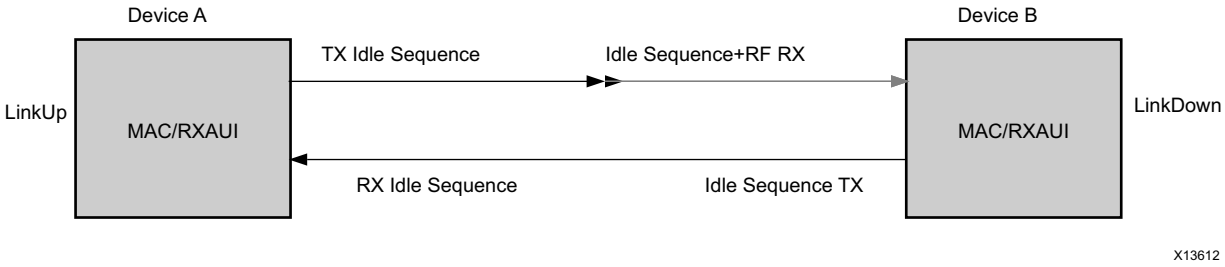

Figure C-5: **Device A Receives Idle Sequence**

Stage 4: Normal Operation

In Stage 4 shown in Figure C-6, Device A and Device B have both powered up and been reset. The link status is 1 (link up) in both A and B and in both the MAC can transmit frames successfully.

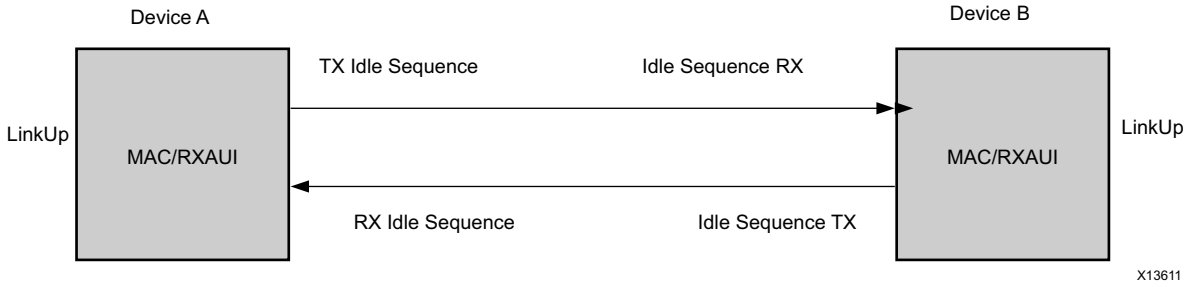

Figure C-6: **Normal Operation**

What Can Cause Synchronization and Alignment to Fail?

Synchronization (`SYNC_STATUS`) occurs when each respective XAUI logical lane receiver is synchronized to byte boundaries. Alignment (`ALIGN_STATUS`) occurs when the RXAUI receiver is aligned across all four logical XAUI lanes.

Following are suggestions for debugging loss of Synchronization and Alignment:

- Monitor the state of the `SIGNAL_DETECT[1:0]` input to the core. This should either be:
  - Connected to an optical module to detect the presence of light. Logic 1 indicates that the optical module is correctly detecting light; logic 0 indicates a fault. Therefore, ensure that this is driven with the correct polarity.
  - Tied to logic 1 (if not connected to an optical module).

Note: When `signal_detect` is set to logic 0, this forces the receiver synchronization state machine of the core to remain in the loss of sync state.

- Loss of Synchronization can happen when invalid characters are received.

- Loss of Alignment can happen when invalid characters are seen or if an /A/ code is not seen in all four XAUI logical lanes at the same time.
- See the section, High Bit Error Rate Issues.

Transceiver Specific

- Ensure that the polarities of the TXN/TXP and RXN/RXP lines are not reversed. If they are, these can be fixed by using the TXPOLARITY and RXPOLARITY ports of the transceiver.
- Check that the transceiver is not being held in reset or still be initialized by monitoring the `mgt_tx_reset`, `mgt_rx_reset`, and `mgt_rxlock` input signals to the RXAUI core. The `mgt_rx_reset` signal is also asserted when there is an RX buffer error. An RX buffer error means that the Elastic Buffer in the receiver path of the transceiver is either under or overflowing. This indicates a clock correction issue caused by differences between the transmitting and receiving ends. Check all clock management circuitry and clock frequencies applied to the core and to the transceiver.

What Can Cause the RXAUI Core to Insert Errors?

On the receive path the RXAUI core inserts errors RXD = FE, RXC = 1, when disparity errors or invalid data are received or if the received interframe gap (IFG) is too small.

Disparity Errors or Invalid Data

Disparity Errors or Invalid data can be checked for by monitoring the `mgt_codevalid` input to the RXAUI core.

Small IFG

The RXAUI core inserts error codes into the Received XGMII data stream, RXD, when there are three or fewer IDLE characters (0x07) between frames. The error code (0xFE) precedes the frame "Terminate" delimiter (0xFD).

The IEEE 802.3-2008 specification (Section 46.2.1) requires a minimum interframe gap of five octets on the receive side. This includes the preceding frame Terminate control character and all Idles up to and immediately preceding the following frame Start control character. Because three (or fewer) Idles and one Terminate character are less than the required five octets, this would not meet the specification; therefore, the RXAUI core is expected to signal an error in this manner if the received frame does not meet the specification.

High Bit Error Rate Issues

Symptoms

If the link comes up but then goes down again or never comes up following a reset, the most likely cause for a RX Local Fault is a Bit Error Rate (BER) that is too high. A high BER causes incorrect data to be received, which leads to the lanes losing synchronization or alignment.

Debugging

Compare the issue across several devices or PCBs to ensure that the issue is not a one-off case.

- Try using an alternative link partner or test equipment and then compare results.
- Try putting the core into loopback (both by placing the core into internal loopback, and by looping back the optical cable) and compare the behavior. The core should always be capable of gaining synchronization and alignment when looping back with itself from transmitter to receiver so direct comparisons can be made. If the core exhibits correct operation when placed into internal loopback, but not when loopback is performed using an optical cable, this can indicate a faulty optical module or a PCB issue.
- Try swapping the optical module on a misperforming device and repeat the tests.

Transceiver Specific Checks

- Monitor the `MGT_CODEVALID[7:0]` input to the RXAUI core by triggering on it using the Vivado Analyzer tool. This input is a combination of the transceiver RX disparity error and RX not in table error outputs.
- These signals should not be asserted over the duration of a few seconds, minutes, or even hours. If they are frequently asserted, it can indicate an issue with the transceiver.
- Place the transceiver into parallel or serial near-end loopback.
    - If correct operation is seen in the transceiver serial loopback, but not when loopback is performed using an optical cable, it can indicate a faulty optical module.
    - If the core exhibits correct operation in the transceiver parallel loopback but not in serial loopback, this can indicate a transceiver issue.
- A mild form of bit error rate can be solved by adjusting the transmitter Pre-Emphasis and Differential Swing Control attributes of the transceiver.

MDIO Problems

See MDIO Interface, page 61 for detailed information about performing MDIO transactions.

Things to check for:

- Ensure that the MDIO is driven properly. Check that the MDC clock is running and that the frequency is 2.5 MHz or less.
- Ensure that the RXAUI core is not held in reset.
- Read from a Configuration register that does not have all 0s as a default. If all 0s are read back, the read was unsuccessful. Check that the `PRTAD` field placed into the MDIO frame matches the value placed on the `PRTAD[4:0]` port of the RXAUI core.
- Verify in simulation and/or a Vivado Analyzer capture that the waveform is correct for accessing the host interface for a MDIO read/write.

If the debug suggestions listed previously do not resolve the issue, open a support case. See Contacting Technical Support for information on how to do this.

To discuss possible solutions, use the Xilinx User Community: forums.xilinx.com/xlnx/

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

References

These documents provide supplemental material useful with this product guide:

1. Dune Networks DN-DS-RXAUI-Spec v1.0, RXAUI - Reduced Pin XAUI
2. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
3. *7 Series FPGAs GTP Transceivers User Guide* (UG482)
4. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
5. *Vivado Design Suite User Guide, Designing with IP* (UG896)
6. *Vivado Design Suite User Guide: Getting Started* (UG910)
7. *Vivado Design Suite User Guide, Logic Simulation* (UG900)
8. ISE to Vivado Design Suite Migration Guide (UG911)
9. *Vivado Design Suite User Guide, Programming and Debugging* (UG908)
10. IEEE Std. 802.3-2008, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/16/2012	1.0	Initial Xilinx release. This Product Guide is derived from DS740 and UG693. Vivado Design Suite and Artix-7 support added.
03/20/2013	1.1	• Updated to v3.0 for Vivado Design Suite only and removed ISE. • Updated Fig. 1-2 Implementation of Dune Networks RXAUI Core. • Updated Table 2-5 Transceiver Interface Ports. • Updated Table 2-7 Configuration and Status Ports. • Added Tables 2-11 Clock and Resets Option Selected to 2-13 GTP Clocking Ports. • Updated SIGNAL_DETECT descriptions in Table 2-25 10G PMD Signal Receive OK Register Bit Definitions. • Added new Clocking and Reset Signals and Module to Debug Interface sections. • Updated Alignment Status and Synchronization Status Ports table. • Updated Fig. 3-1 7 Series GTX Transceivers to Fig. 3-3 7 Series GTP Transceivers. • Updated Fig. 4-1 RXAUI Main Screen. • Updated Constraining the Core section. • Updated Fig. 6-1 RXAUI Example Design and Test Bench and added Fig. 6-2. • Updated to new Debug section. • Updated to Questa SIM.
10/02/2013	4.0	• Revision number advanced to 4.0 to align with core version number. • Added 'Shared logic' core option throughout the document. • Updated Ports and Port description tables throughout Chapter 2. • Added Changing the clk156 Clock Buffer. • Updated Multiple Core Instances. • Updated Chapter 5, Constraining the Core. • Updated Chapter 8, Detailed Example Design. • Added Chapter 9, Test Bench. • Added Appendix B, Migrating and Upgrading.

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