LogiCORE IP Processor System Reset Module (v4.00a)

DS406 July 25, 2012 **Product Specification**

Introduction

The Xilinx® LogiCORE™ IP Processor System Reset Module core provides customized resets for an entire processor system, including the processor, the interconnect and peripherals. The core allows customers to tailor their designs to suit their application by setting certain parameters to enable/disable features. The features of designs are discussed in the Design Parameters section.

Features

- Supports asynchronous external reset input which is synchronized with clock
- Both the external and auxiliary reset inputs are selectable as active-High or active-Low
- Selectable minimum pulse width for reset inputs to be recognized
- DCM Locked input
- Power On Reset generation
- Parameterized active-Low reset signal generation for core and for interconnect
- Sequencing of reset signals coming out of reset:
  a. Bus structures come out of reset (Interconnect and bridge)
  b. Peripherals come out of reset 16 clock cycles later (UART, SPI, IIC)
  c. The MicroBlaze™ processor comes out of reset 16 clock cycles after the peripherals

LogiCORE IP Facts Table		
Core Specifics		
Supported Device Family(1)	Artix™-7, Virtex®-7, Kintex™-7	
Supported User Interfaces	N/A	
Resources		
	Min	Max
LUTs	N/A	N/A
I/Os	N/A	N/A
FFs	N/A	N/A
Provided with Core		
Documentation	Product Specification	
Design Files	VHDL	
Example Design	Not Provided	
Test Bench	Not Provided	
Constraints File	Not Provided	
Simulation Model	Not Provided	
Supported S/W Driver	N/A	
Tested Design Tools		
Design Entry Tools	Xilinx Vivado™ Design Suite(3)	
Simulation(2)	Mentor Graphic ModelSim	
Synthesis Tools	Vivado synthesis	
Support		
Provided by Xilinx @ www.xilinx.com/support		

1. For a complete list of supported derivative devices, see the Embedded Edition Derivative Device Support.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
3. Supports 7 series devices only.

Functional Description

The Processor Reset Module block diagram is shown in Figure 1.

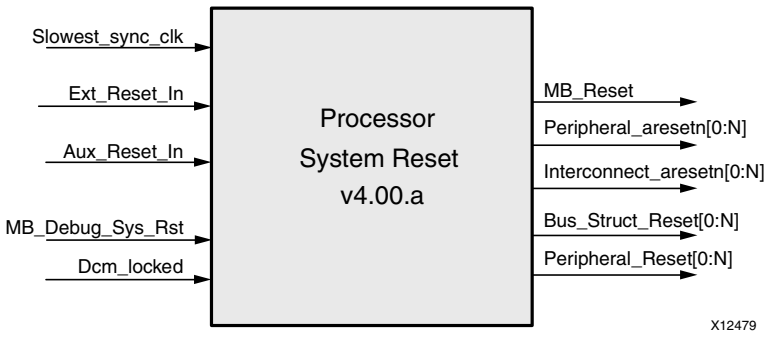

Figure 1: **Block Diagram for the Processor System Reset Module**

Processor System Reset Module Circuit Description

The core has five input signals and five output signals. There are eight generics that can be set by the user. Additional outputs can be generated through the use of the generics, C_NUM_BUS_RST, C_NUM_PERP_RST, C_NUM_INTERCONNECT_ARESETN and C_NUM_PERP_ARESETN. Figure 3 shows the Processor System Reset Module timing when an `Ext_Reset_In` occurs. The timing diagram is identical for an occurrence of C_NUM_BUS_RST. For this example C_NUM_BUS_RST is set to 5 and C_EXT_RESET_HIGH is set to 0, active-Low.

Core Functionality

The core receives C_EXT_RST_WIDTH and C_AUX_RST_WIDTH parameters. These parameters are used to set the minimum width of the external and auxiliary reset signals with respect to the `Slowest_sync_clk` to allow the change to be detected. For example, if C_EXT_RST_WIDTH is set to 5, then the `Ext_Reset_In` must become active and stay active for at least five clock cycles before a reset is initiated. C_AUX_RST_WIDTH sets the number of clock cycles a change on `Aux_Reset_In` must be before the change is detected and used by the Processor System Reset Module. `Aux_Reset_In` performs exactly the same way as `Ext_Reset_In`.

There is a one or two clock latency caused by the meta-stability circuit. Because `Ext_Reset_In` does not have to be synchronous with the input clock, the exact number of clocks cannot be determined. The reset becomes active in six or seven clocks after the input has gone active and stays active for five clocks. After `Ext_Reset_In` has gone inactive for five clocks the sequencing to come out of reset begins. If, during the sequencing, `Ext_Reset_In` goes active for five or more clocks all outputs become active again.

C_EXT_RESET_HIGH is used to set the logic level for which `Ext_Reset_In` causes a reset. If this generic is set to 1, when `Ext_Reset_In` is High on a rising edge of clock, a reset is initiated.

C_AUX_RESET_HIGH is used to set the logic level for which `Aux_Reset_In` causes a reset. If this generic is set to 0, when `Aux_Reset_In` is Low, a reset is initiated.

C_NUM_BUS_RST and C_NUM_INTERCONNECT_ARESETN are used to generate additional `Bus_Struct_Reset` and Interconnect Structure Reset signals. This helps with signal loading and routing. In general each bus can have its own `Bus_Struct_Reset` (`Interconnect_aresetn` in case of interconnect) signal. For example, if a system has one AXI4 interface then C_NUM_BUS_RST can be set to one. The `Bus_Struct_Reset` output(s) should reset the arbiter(s) and bridges located on the bus. The same explanation applies to the number of Interconnect instances present in the system.

Note: The reset signal polarity for interconnect instances are active-Low when asserted.

C_NUM_PERP_RST and C_NUM_PERP_ARESETN are used to generate additional Peripheral_Reset (active-High) and Peripheral_aresetn (active-Low) signals. This helps with signal loading and routing. In general every peripheral can have its own Peripheral_Reset signal (Peripheral_aresetn in case of peripherals connected to interconnect in a system). For example, if there is one ATM, two UARTs, one 10/100 Ethernet controller and one IIC on the AXI4, then C_NUM_PERP_RST can be set to five. However, the C_NUM_PERP_RST can be set to one and all peripheral resets can be driven by the same output. The same explanation applies to the number of peripherals connected to Interconnect instances present in the system.

Note: The reset signal polarity for peripherals connected to interconnects are active-Low when asserted.

MB_Debug_Sys_Rst is an input signal that performs the same type of reset as Ext_Reset_In. The width of this signal complies to the same width requirement as for Ext_Reset_In, set by the parameter C_EXT_RST_WIDTH . MB_Debug_Sys_Rst is always active-High, (unaffected by the parameter C_EXT_RESET_HIGH). Normally this signal is connected to the Microprocessor Debug Module, MDM.

DCM_Locked is an input to the reset module. If the system does not use any DCMs this input should be tied High. If the system uses one DCM to generate system clocks, the output from the DCM should be connected to the input on the reset module. If the system contains more than one DCM to generate system clocks, the DCM output that achieves lock last should be connected to the input.

The Slowest_Sync_Clk input should be connected to the slowest synchronous clock used in the system. This is typically the AXI4-Lite interface clock, but could be any of the bus or CPU clocks.

All outputs go active on the same edge of the clock. However, there is a sequencing that occurs when releasing the reset signal. The first reset signals to go inactive are the Bus_Struct_Reset and Interconnect_aresetn; 16 clocks later Peripheral_Reset and Peripheral_aresetn go inactive; 16 clocks later MB_Reset goes inactive. Now all the resets are inactive and processing can begin.

There are two generics which decides the vector width of active-Low reset output signals. The parameter C_NUM_INTERCONNECT_ARESETN and C_NUM_PERP_ARESETN decide the width of active-Low reset signals. Interconnect_aresetn provides the active-Low reset to interconnect and Peripheral_aresetn provides the active-Low reset to peripherals. The width of Interconnect_aresetn is similar to the Bus_Struct_Reset signal width. The width of Peripheral_aresetn is similar to the Peripheral_Reset signal width. The active-Low resets are mainly targeted for AXI-based peripherals or the peripherals which need an active-Low reset input. An example of using the Processor System Reset Module core is shown in Figure 2.

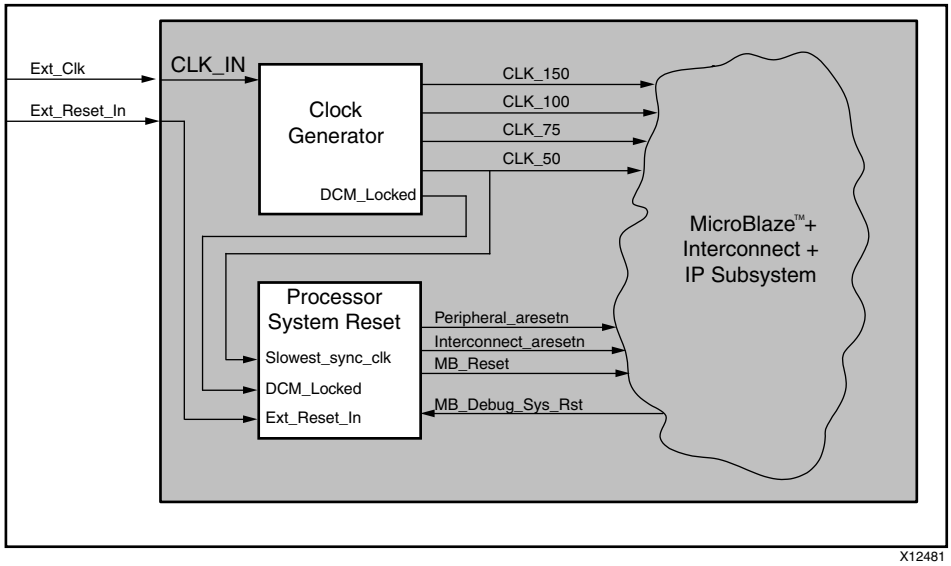

Figure 2: **Example of the Processor System Reset Module Core**

Figure 3 shows the core timing behavior. The Power On Reset condition causes all the reset outputs to become active within the first two clocks of a power up and remain active for 16 clocks. The resets then begin the sequencing as shown in Figure 3.

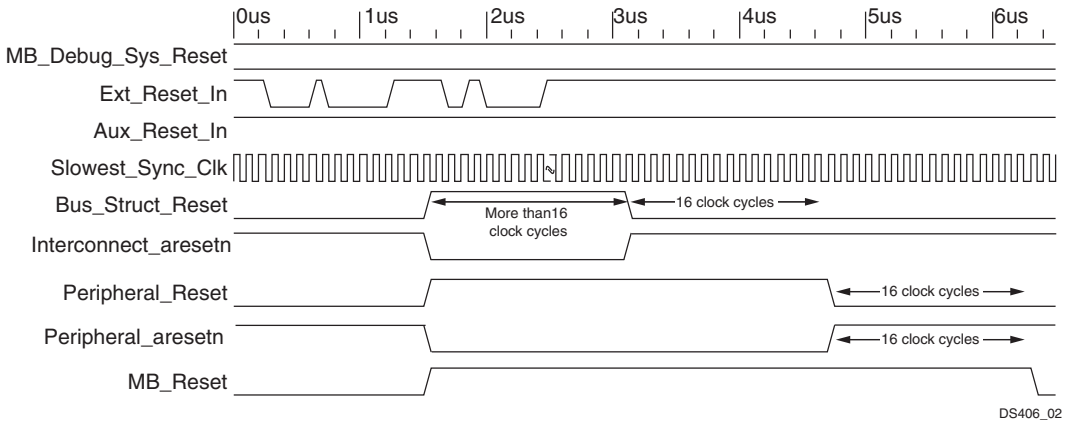

Figure 3: **Processor System Reset Module - Ext_Reset_In (Active Low)**

Design Parameters

To allow you to obtain a Processor System Reset Module that is uniquely tailored for your system, certain features can be parameterized in the Processor System Reset Module design, thereby providing a design that utilizes only the resources required by the system and runs with the best possible performance. The features that can be parameterized in the Xilinx Processor System Reset Module design are shown in Table 1.

Table 1: **Processor System Reset Module Design Parameters**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Processor System Reset Module Features					
G1	FPGA Family	C_FAMILY	virtex7, kintex7, artix7	virtex7	string
G2	Number of clocks before input change is recognized on the Ext_Reset_In and the MB_Debug_Sys_Rst inputs	C_EXT_RST_WIDTH(1)	1 - 16	4	integer
G3	Number of clocks before input change is recognized on the Aux_Reset_In input	C_AUX_RST_WIDTH(1)	1 - 16	4	integer
G4	Defines the active state of the Ext_Reset_In input	C_EXT_RESET_HIGH	1 = Reset generated when external reset = 1 0= Reset generated when external reset = 0	1	std_logic
G5	Defines the active state of the Aux_Reset_In input	C_AUX_RESET_HIGH	1 = Reset generated when external reset = 1 0 = Reset generated when external reset = 0	1	std_logic
G6	Number of Bus_Struct_Reset registered outputs. In general, equals number of instantiated buses.	C_NUM_BUS_RST	1 - 8	1	integer
G7	Number of Peripheral_Reset registered outputs. In general, equals number of peripherals.	C_NUM_PERP_RST	1 - 16	1	integer
G8	Number of Interconnect_aresetn registered outputs. In general, equals number of instantiated interconnects.	C_NUM_INTERCONNECT_ ARESETN	1 - 8	1	integer
G9	Number of Peripheral_aresetn registered outputs. In general, equals number of peripherals connected to interconnect.	C_NUM_PERP_ ARESETN	1 - 16	1	integer

Notes:

1. Though the core supports the external reset width for more than 16 cycles, it is recommended that you enter the reset widths in the specified range only.

I/O Signals

The I/O signals for the Processor System Reset Module are listed in Table 2.

Table 2: **Processor System Reset Module I/O Signals**

Port	Signal Name	Interface	I/O	Description
P1	Slowest_sync_clk	System	I	Slowest Synchronous Clock. Typically AXI4 Lite clock.
P2	Ext_Reset_In	System	I	External Reset Input. Active-High or Low based upon the generic C_EXT_RESET_HIGH.
P3	MB_Debug_Sys_Rst	System	I	MDM reset input. Always active-High, minimum width defined by parameter C_EXT_RST_WIDTH
P4	Aux_Reset_In	System	I	Auxiliary Reset Input. Active-High or Low based upon the generic C_AUX_RESET_HIGH.
P5	Dcm_locked	System	I	DCM Lock signal.

Table 2: **Processor System Reset Module I/O Signals *(Cont'd)***

Port	Signal Name	Interface	I/O	Description
P6	MB_Reset	System	O	MB core reset. Active-High.
P7	Bus_Struct_Reset[0 to C_NUM_BUS_RST - 1](1)	System	O	Bus Structures reset - for example, arbiters for bridges. Active-High
P8	Peripheral_Reset[0 to C_NUM_PERP_RST - 1](2)	System	O	Peripheral reset is for all peripherals attached to any bus that is synchronous with the Slowest_sync_clk. Active-High.
P9	Interconnect_aresetn [0 to C_NUM_INTERCONNECT_ARESETN - 1](1)	System	O	Interconnect_aresetn reset - for example, interconnects with active-Low reset inputs.
P10	Peripheral_aresetn [0 to C_NUM_PERP_ARESETN - 1](2)	System	O	Peripheral_aresetn is for all peripherals attached to interconnect that is synchronous with the Slowest_sync_clk. Active-Low.

Notes:

1. To help equalize loading on this signal, there can be from 1 to 8 copies generated with each copy being individually registered through a D-flip flop. In general each unique bus should receive a different copy of this signal.
2. To help equalize loading on this signal, there can be from 1 to 16 copies generated with each copy being individually registered through a D-flip flop. In general each peripheral should receive a different copy of this signal.

Port Dependencies

The width of some of the Processor System Reset Module signals depends on parameters set by generic inputs to the design. The dependencies between the Processor System Reset Module design parameters and I/O signals are shown in Table 3.

Table 3: **Parameter Port Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G6	C_NUM_BUS_RST	P7	-	The number of bus structure reset outputs is set by this generic
G7	C_NUM_PERP_RST	P8	-	The number of peripheral reset outputs is set by this generic
G8	C_NUM_INTERCONNECT_ARESETN	P9, P18	-	The number of interconnect instances active-Low reset outputs is set by this generic
G9	C_NUM_PERP_ARESETN	P10, P17	-	The number of peripherals connected to interconnects reset outputs is set by this generic
I/O Signals				
P7	Bus_Struct_Reset(0 to C_NUM_BUS_RST - 1)	-	G6	Width varies with the size of the C_NUM_BUS_RST.
P8	Peripheral_Reset(0 to C_NUM_PERP_RST - 1)	-	G7	Width varies with the size of the C_NUM_PERP_RST.
P9	Interconnect_aresetn (0 to C_NUM_INTERCONNECT_ARESETN - 1)	-	G8	Width varies with the size of the C_NUM_INTERCONNECT_ARESETN.
P10	Peripheral_aresetn [0 to C_NUM_PERP_ARESETN - 1]	-	G9	Width varies with the size of the C_NUM_PERP_ARESETN.

Design Implementation

Target Technology

The target technology is an FPGA listed in the Supported Device Family field in the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

Because the Processor System Reset IP core is used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the core is combined with other designs in the system, the utilization of FPGA resources and core timing will vary from the results reported here.

The Processor System Reset IP core resource utilization for various parameter combinations measured with a Kintex-7 FPGA as the target device are detailed in Table 4. The utilization figures should be considered as reference only.

Table 4: **Performance and Resource Utilization Benchmarks on a Kintex-7 FPGA**

C_EXT_RST_WIDTH	C_AUX_RST_WIDTH	C_NUM_INTERCONNECT_ARESETN	C_NUM_PERP_ARESETN	C_NUM_BUS_RST	C_NUM_PERP_RST	Slice LUTS	Slice Registers	FMax (MHz)
4	4	4	4	1	1	27	41	200 MHz
16	16	8	16	8	16	41	91	200 Mhz

1. Kintex-7 device: xc7k325tffg900-3

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite tool under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
5/25/07	1.0	Initial Xilinx release.
12/06/07	1.1	Added Virtex II P support
04/24/09	1.2	Replaced references to supported device families and tool name(s) with hyperlinks to PDF files; Updated trademark information.
06/01/09	1.3	Updated figure 2. Added note in the Table 1 regarding the usage of reset width.
04/19/10	1.4	Updated figure 1. Added two generics and two active-Low reset signals. Updated the version of the core.
7/23/10	1.5	Updated to 12.2; converted to new DS template; added Order Information section.
04/24/12	1.6	Updated for Vivado Release 2012.1. Version 4.00a of core. PPC related functionality removed.
07/25/12	1.7	Updated for Vivado release 2012.2. Characterization data added.

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