LogiCORE IP Initiator/Target v5 and v6 for PCI-X

DS208 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Initiator/Target v5 and v6 for PCI®-X core interface is a pre-implemented and fully tested module for Xilinx® FPGAs. Critical paths are controlled by constraints files to ensure predictable timing. This significantly reduces engineering time required to implement the PCI-X portion of your design.

The core meets the setup, hold, and clock-to-timing requirements as specified in the PCI-X specification. The interface is carefully optimized for best possible performance and utilization in Xilinx FPGA devices.

Features

- Fully 2.0 Mode 1 compliant LogiCORE IP for PCI-X, 64-bit, 133/66 MHz interface with 3.3V operation
- 3.0-compliant core for PCI up to 33 MHz
- Customizable, programmable, single-chip solution
- Pre-defined implementation for predictable timing
- Incorporates Xilinx Smart-IP™ Technology
- Fully verified design tested with Xilinx proprietary test bench and hardware
- Available through the Xilinx CORE Generator™ software v12.1 with applicable service pack
- Integrated extended capabilities:
  - PCI-X Capability Item
  - Power Management Capability Item
  - Message Signaled Interrupt Capability Item
- Supported functions for PCI-X
  - Split Completion
  - Memory Read DWORD
  - Memory Read Block
  - Memory Write Block
- Supported functions for PCI
  - Memory Read
  - Memory Read Multiple
  - Memory Read Line
- Memory Write and Invalidate

LogiCORE IP Facts				
Core Specifics				
Supported Device Family	See Table 1, page 2.			
Resources Used (1)	v6 PCI-X 64/133 in PCI-X Mode	v6 PCI64/33 Mode Only	v5 PCI-X64/133 in PCI-X Mode	v5 PCI64/33 Mode Only
LUTs	1748	1469	2310	1868
Slice Flip Flops	1109	954	1504	1350
IOB Flip Flops	94	257	253	253
IOBs	94	90	90	90
BUFGs / DCMs	2/1	2/0	1/1	2/0
Provided with Core				
Documentation	*Getting Started Guide v6* *Getting Started Guide v5* *User Guide v6* *User Guide v5*			
Design File Formats	Verilog/VHDL Simulation Model NGC Netlist (v6 core only) NGO Netlist (v5 core only)			
Constraints Files	User Constraints Files (UCF)			
Example Design	VHDL Verilog			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 12.1i			
Verification	Mentor Graphics® ModelSim® v6.5c and above			
Simulation	Mentor Graphics ModelSim v6.5c and above Synopsys VCS and VCS MX 2009.12 and above Cadence® Incisive Enterprise Simulator (IES) v9.2 and above			
Synthesis	XST Synplicity® Synplify Pro® D-2009.12			
Support				
Provided by Xilinx, Inc.				

1. Resource utilization depends on configuration of the interface and the user design. Unused resources are trimmed by the Xilinx technology mapper. The utilization figures reported in this table are representative of a maximum configuration.

Note: Xilinx provides technical support for this product when used as described in the getting started and user guides for this core. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed, or if customized beyond that allowed in the product documentation.

Table 1: **Core Implementation for PCI-X64**

Device Supported(1)	Core Version	Power Supply
PCI-X64/133		
Virtex®-5 XC5VFX70T-FF1136-1C/I(2)	v6	3.3V only
Virtex-5 XC5VLX50-FF1153-1C/I(2)	v6	3.3V only
Virtex-5 XC5VLX50T-FF1136-1C/I(2)	v6	3.3V only
Virtex-5 XC5VLX110-FF1153-1C/I(2)	v6	3.3V only
Virtex-5 XC5VLX110T-FF1136-1C/I(2)	v6	3.3V only
Virtex-5 XC5VSX50T-FF1136-1C/I(2)	v6	3.3V only
Virtex-5 XC5VSX95T-FF1136-1C/I(2)	v6	3.3V only
Virtex-4 XC4VFX20-FF672-10C/I	v5	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I	v5	3.3V only
Virtex-4 XC4VSX35-FF668-10C/I	v5	3.3V only
PCI-X64/100		
Virtex-5 XC5VFX70T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VLX50-FF1153-1C/I	v6	3.3V only
Virtex-5 XC5VLX50T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VLX110-FF1153-1C/I	v6	3.3V only
Virtex-5 XC5VLX110T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VSX50T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VSX95T-FF1136-1C/I	v6	3.3V only
Virtex-4 XC4VFX20-FF672-10C/I	v5	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I	v5	3.3V only
Virtex-4 XC4VSX35-FF668-10C/I	v5	3.3V only
PCI-X64/66		
Virtex-5 XC5VFX70T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VLX50-FF1153-1C/I	v6	3.3V only
Virtex-5 XC5VLX50T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VLX110-FF1153-1C/I	v6	3.3V only
Virtex-5 XC5VLX110T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VSX50T-FF1136-1C/I	v6	3.3V only
Virtex-5 XC5VSX95T-FF1136-1C/I	v6	3.3V only
Virtex-4 XC4VFX20-FF672-10C/	v5	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I	v5	3.3V only
Virtex-4 XC4VSX35-FF668-10C/I	v5	3.3V only
PCI64/33		
Virtex-5 XC5VFX70T-FF1136-1C/I(3)	v6	3.3V only

Table 1: **Core Implementation for PCI-X64 *(Cont'd)***

Device Supported(1)	Core Version	Power Supply
Virtex-5 XC5VLX50-FF1153-1C/I(3)	v6	3.3V only
Virtex-5 XC5VLX50T-FF1136-1C/I(3)	v6	3.3V only
Virtex-5 XC5VLX110-FF1153-1C/I(3)	v6	3.3V only
Virtex-5 XC5VLX110T-FF1136-1C/I(3)	v6	3.3V only
Virtex-5 XC5VSX50T-FF1136-1C/I(3)	v6	3.3V only
Virtex-5 XC5VSX95T-FF1136-1C/I(3)	v6	3.3V only
Virtex-4 XC4VFX20-FF672-10C/I(3)	v5	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I(3)	v5	3.3V only
Virtex-4 XC4VSX35-FF668-10C/I(3)	v5	3.3V only

Notes:

1. For Virtex-4 and Virtex-5, use the UCF Generator in the CORE Generator software.
2. Virtex-5 devices in PCI-X 133 mode require a 200 MHz reference clock.
3. Virtex-4 and Virtex-5 devices in PCI mode require a 200 MHz reference clock.
4. Packages listed are supported in both standard and lead-free variants (where available). For example, FF1136 indicates support for both FF1136 and FFG1136 packages.

Supported PCI and PCI-X Functions

- Memory Write
- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Interrupt Acknowledge
- Bus Parking
- Type 0 Configuration Space Header
- Full 64-bit Addressing Support
- Up to 6 Base Address Registers
- Expansion ROM Base Address Register
- Instant-On Base Address Registers
- Parity Generation, Parity Error Detection
- Full Command/Status Registers

Applications

- Embedded applications in networking, industrial, and telecommunication systems
- PCI-X add-in boards such as frame buffers, network adapters, and data acquisition boards
- Hot swap Compact PCI-X boards
- Any applications that require a PCI-X interface

Smart-IP Technology

Drawing on the architectural advantages of Xilinx FPGAs, Xilinx Smart-IP technology ensures the highest performance, predictability, reproducibility, and flexibility in designs for PCI-X. Smart-IP technology is incorporated in every interface for PCI-X.

Xilinx Smart-IP technology leverages the Xilinx architectural advantages, such as look-up tables and segmented routing, as well as floor planning information, such as logic mapping and location constraints. This technology provides the best physical layout, predictability, and performance. Additionally, these features allow for significantly reduced compile times over competing architectures.

To guarantee the critical setup, hold, minimum clock-to-out, and maximum clock-to-out timing, the core interface is delivered with Smart-IP constraints files that are unique for a device and package combination. These constraints files guide the implementation tools so that the critical paths are always within specification.

Xilinx provides Smart-IP constraints files for many device and package combinations. Constraints files for unsupported device and package combinations may be generated using the web-based user constraints file generator.

Other features that enable efficient implementation of a PCI-X system include:

- **Block SelectRAM™ memory:** Blocks of on-chip ultra-fast RAM with synchronous write and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.
- **SelectRAM™ memory:** Distributed on-chip ultra-fast RAM with synchronous write option and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.

The interface is carefully optimized for best possible performance and utilization in Xilinx FPGA devices.

Functional Description

Figure 1 illustrates the core interface for PCI-X partitioned into six major blocks and a user application.

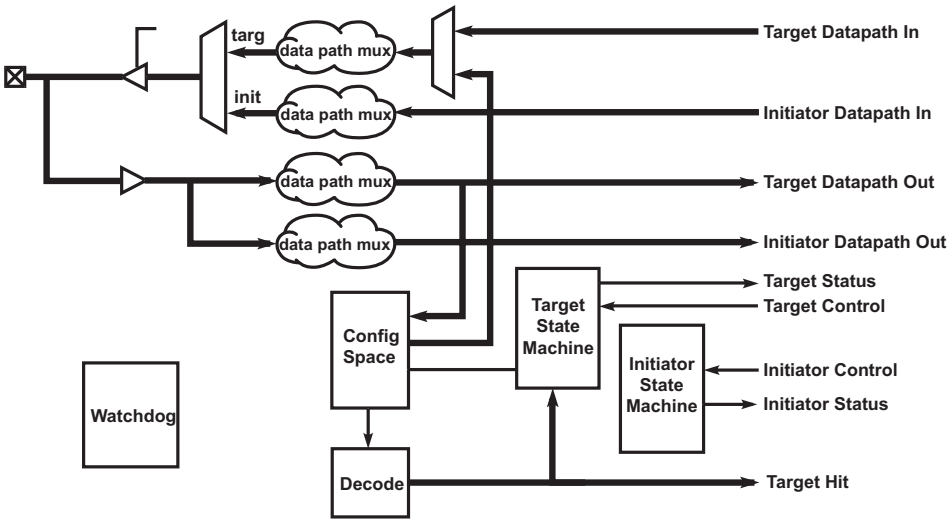

Figure 1: **Block Diagram**

Datapath

There are four datapaths, in and out for both target and initiator. To improve timing and ease of design, the four unidirectional datapaths are multiplexed inside the interface. All data transfers are register-to-register. Since fewer registers are on each datapath, loading is reduced and false timing paths are eliminated.

Decode

When an address is broadcast on the bus, the decode module compares it to the base address registers for a match. If one occurs, the target state machine is activated.

Configuration Space

This block provides the first 64 bytes of Type 0, version 3.0 Configuration Space Header, and an additional 64 bytes reserved for extended capabilities, as shown in Table 2, page 6. The remaining 128 bytes of configuration space is available to the user for application specific registers. Together, these support software-driven Plug-and-Play initialization and configuration. This includes information for Command, Status, Base Address Registers, and the extended capabilities required for PCI-X.

Three extended capabilities are provided in the interface:

- PCI-X Capability Item
- Power Management Capability Item
- Message Signalled Interrupt Capability Item

These capability items may be linked or delinked from the capabilities list as required, and user functions can be integrated into the capabilities list.

Table 2: **Configuration Space Header for PCI-X**

31	24	23	16	15	8	7	0	
Device ID				Vendor ID				00h
Status				Command				04h
Class Code						Rev ID		08h
BIST		Header Type		Latency Timer		Cache Line Size		0Ch
Base Address Register 0 (BAR0)								10h
Base Address Register 1 (BAR1)								14h
Base Address Register 2 (BAR2)								18h
Base Address Register 3 (BAR3)								1Ch
Base Address Register 4 (BAR4)								20h
Base Address Register 5 (BAR5)								24h
Cardbus CIS Pointer								28h
Subsystem ID				Subsystem Vendor ID				2Ch
Expansion ROM Base Address								30h
Reserved						CapPtr		34h
Reserved								38h
Max Lat		Min Gnt		Interrupt Pin		Interrupt Line		3Ch
Power Management Capability				NxtCap		PM Cap		40h
Data		PMCSR BSE		PMCSR				44h
Message Control				NxtCap		MSI Cap		48h
Message Address								4Ch
Message Upper Address								50h
Reserved				Message Data				54h
PCI-X Command				NxtCap		PCI-X Cap		58h
PCI-X Status								5Ch
Reserved								60h-7Fh
Available User Configuration Space								80h-FFh

Notes:

1. Shaded areas are not implemented and return zero.

Watchdog

The watchdog monitors various system conditions, including bus mode and bus width. This module also indicates if run-time reconfiguration is required for loading different bitstreams.

Target State Machine

This block controls interfaces for PCI-X and PCI for target functions. The controller is a high-performance state machine using one-hot encoding for maximum performance.

Initiator State Machine

This block controls interfaces for PCI-X and PCI for initiator functions. The initiator control logic also uses one-hot encoding for maximum performance.

User Interface

The interface for PCI-X provides a simplified user application interface that allows you to create one design to handle both PCI-X and PCI transactions without design changes, and both 32-bit and 64-bit data transfers without external data width conversion. This eliminates the need for multiple designs to support PCI-X and PCI and varying bus widths.

This streamlined interface also simplifies the amount of work needed to create a user application. The user interface can be designed as either a 32-bit or 64-bit interface and the core interface for PCI-X will automatically handle data conversions regardless of the width of the PCI-X or PCI bus.

Interface Configuration

The core interface can be easily configured to fit unique system requirements using the Xilinx CORE Generator GUI. For the v5 core, the HDL configuration file may be changed to configure the core after the core has been generated. The following customization options, among many others, are supported by the interface and are described in the *Initiator/Target for PCI-X User Guide.*

- Device and vendor ID
- Base Address Registers (number, size, and mode)
- Expansion ROM BAR
- Cardbus CIS pointer
- Interrupt Connectivity
- Extended Command Use
- Capability Configuration

Burst Transfer

The PCI-X bus derives its performance from its ability to support burst transfers. The performance of any application for PCI-X depends largely on the size of the burst transfer. Buffers to support PCI-X burst transfer can efficiently be implemented using on-chip RAM resources.

Supported PCI Commands

Table 3 defines the PCI bus commands supported by the core interface, and Table 4, page 9 defines the supported PCI-X bus commands.

Table 3: **PCI Bus Commands**

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read(1)	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple(2)	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Line(2)	Yes	Yes
1111	Memory Write Invalidate(2)	Yes	Yes

Notes:

1. This command can only be used for a single DWORD transfer.
2. These commands have fixed byte enables of 0h.

Table 4: **PCI-X Bus Commands**

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read Dword	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Alias to Memory Read Block	Yes	Yes
1001	Alias to Memory Write Block	Yes	Yes
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Split Completion	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Block	Yes	Yes
1111	Memory Write Block	Yes	Yes

Bandwidth

The core interface supports fully compliant zero wait-state burst operations for sourcing and receiving data. This interface supports a sustained bandwidth of up to 1066 MB/sec. The design can be configured to take advantage of the ability of the core interface to do very long bursts.

The flexible user application interface, combined with support for many different features, gives users a solution that lends itself to use in many high-performance applications. Because you are not locked into one DMA engine, you can create an optimized design that is application-specific.

Recommended Design Experience

The core interface is pre-implemented, allowing engineering focus on the unique user-application functions of a PCI-X design. However, PCI-X is a high-performance design that is challenging to implement in any technology. For this reason, previous experience building high-performance, pipelined FPGA designs using Xilinx implementation software, constraint files, and guide files is recommended. The challenge to implement a complete PCI-X design including user application functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation of your specific requirements.

Timing Specifications

The maximum speed at which your user design is capable of running can be affected by the size and quality of the design. The key timing parameters for the PCI-X 133 MHz are shown in Table 6, for the PCI-X 66MHz in Table 5, and for the PCI 33MHz in Table 7.

Table 5: **Timing Parameters for PCI-X 66 MHz**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	15(1)	20
T_{high}	CLK High Time	6	-
T_{low}	CLK Low Time	6	-
T_{val}	CLK to Signal Valid Delay (bused signals)	0.7(2)	3.8(2)
T_{val}	CLK to Signal Valid Delay (point to point signals)	0.7(2)	3.8(2)
T_{on}	Float to Active Delay	0(2)	-
T_{off}	Active to Float Delay	-	7(2)
T_{su}	Input Setup Time to CLK (bused signals)	1.7(2)	-
T_{su}	Input Setup Time to CLK (point to point signals)	1.7(2)	-
T_{h}	Input Hold Time from CLK	0.5(2)	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:

1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCIX.
3. Operation at 100 MHz requires Tsu of 1.2 and Tcyc of 10.

Table 6: **Timing Parameters for PCI-X 133 MHz**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	7.5(1)	20
T_{high}	CLK High Time	6	-
T_{low}	CLK Low Time	6	-
T_{val}	CLK to Signal Valid Delay (bused signals)	0.7(2)	3.8(2)
T_{val}	CLK to Signal Valid Delay (point to point signals)	0.7(2)	3.8(2)
T_{on}	Float to Active Delay	0(2)	-
T_{off}	Active to Float Delay	-	7(2)
T_{su}	Input Setup Time to CLK (bused signals)	1.2(2)	-
T_{su}	Input Setup Time to CLK (point to point signals)	1.2(2)	-
T_{h}	Input Hold Time from CLK	0.5(2)	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:

1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCIX.
3. Operation at 100 MHz requires Tsu of 1.2 and Tcyc of 10.

Table 7: **Timing Parameters for PCI 33 MHz**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	30(1)	-
T_{high}	CLK High Time	11	-
T_{low}	CLK Low Time	11	-
T_{val}	CLK to Signal Valid Delay (bused signals)	2(2)	11(2)
T_{val}	CLK to Signal Valid Delay (point to point signals)	2(2)	11(2)
T_{on}	Float to Active Delay	2(2)	-
T_{off}	Active to Float Delay	-	28(1)
T_{su}	Input Setup Time to CLK (bused signals)	7(2)	-
T_{su}	Input Setup Time to CLK (point to point signals)	10(2)	-
T_{h}	Input Hold Time from CLK	0(2)	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:

1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCI33_3 or PCIX.

Ordering Information

This core can be accessed through the Xilinx CORE Generator v12.1. The Xilinx CORE Generator software is bundled with the ISE Foundation v12.1 software at no additional charge. To purchase the Xilinx Initiator/Target v5 and v6 for PCI-X core, please contact your local Xilinx **sales representative**.

Visit the Initiator/Target for PCI/PCI-X product offering page for more information.

Part Numbers

- EF-DI-PCIX64-VE-SITE
  - v6 and v5 64-bit Initiator/Target for PCI-X
  - v4 and v3 32-bit and 64-bit 33/66 MHz Initiator/Target for PCI
- DX-DI-64IP-XVE
  - Upgrade from DO-DI-PCI64/DO-DI-PCI-AL/EF-DI-PCI-AL-SITE to EF-DI-PCIX64-VE-SITE

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/28/02	1.0	New template
11/04/02	1.1	Update for core compliance of 2.0 Mode1; performance of 64-bit/133 MHz; support of PCI v2.3; support of Xilinx design tool v5.Ii Service Pack 2.
12/05/02	1.2	In Introduction section, 1066 Mbytes/sec was 800 Mbytes/sec; in Features section, first bullet, 133/66 MHz was 133/66/33 MHz
3/03/03	1.3	Revised date to 3/7/03; added PCI-X64/PCI-X64/100 Resource Utilization data; revised Xilinx tools to v5.2i; added Virtex-II Pro to PCI-X 64 Supported Devices list.
4/17/03	1.4	Revised date to 4/14/03; in Table 4, Clock Cycle Time, Min 7.5 was Min 15; Input Setup Time to CLK (bused signals) and Input Setup Time to CLK (point to point signals), Min 1.2 was Min 1.7.
5/8/03	1.5	Updated Xilinx tools to 5.2i SP2.
5/29/03	1.6	Updated speed grade for PCI-X 64/133, Virtex-II 2VP7FF672 device changed to -7C; was 6C
9/17/03	1.7	Updated Xilinx Tools v6.1i SP1 was v5.2i SP2; date was May 29, 2003.
11/14/03	1.8	In Supported Devices table, added XC prefix to all device numbers; changed all PCI-X 64/133 devices to XC2VP7FF672-6 was -7; Xilinx Tools v6.1i SP2 was v6.1i SP1;
1/25/04	1.9	Changed Xilinx Tools to v6.1i SP3; in Supported Devices table, added Virtex-Pro XC2VP20FF1152-6C in each family group; in first page, changed year date to 2004.
3/10/04	1.10	Updated to v3.0.126, updated Xilinx tools to 6.2i SP1, added note 11 to Supported devices table, added suffix /I to all Virtex-II Pro devices, added Virtex-II Pro XC2VP30...through XC2VP50...to each supported category.
4/26/04	1.11	Updated build version to v5.0.78, updated Xilinx tools to 6.2i SP2, changed date to April 26, 2004.
7/15/04	1.12	Updated build to v5.0.79, and added support for Xilinx tools v6.2i SP3. The data sheet is updated to the new template.
9/23/04	1.13	Updated document to fix a typographical error in the Core Implementation table on page 3.

Date	Version	Revision
11/11/04	1.14	Updated support for Xilinx tools v6.3i; updated PCI spec to v3.0; added Exemplar LeonardoSpectrum and Cadence NC-Verilog entry and verification tools.
12/8/04	1.15	Updated to build 5.0.90 and Virtex-4 support.
3/7/05	1.16	Updated to Xilinx tools 7.1i and PCI-X build 5.0.95.
5/13/05	2.0	Updated build to 3.0.100, addition of SP2.
8/31/05	3.0	Updated build to 3.0.101, updated SP2 to SP3 for 7.1i
9/12/05	4.0	Updated build to 3.0.102, updated SP3 to SP4 for 7.1i.
1/18/06	5.0	Updated build to 3.0.105, ISE software to v8.1i, release date.
2/14/06	5.5	Advanced build to 108, added SP2 support to ISE v8.1i, updated release date.
7/13/06	6.0	Added core v6, support for Virtex-5, ISE to v8.2i, build number to 160, release date
2/15/07	6.5	Added core v6 support for Virtex-5 LXT, ISE to v9.1i
5/17/07	7.0	Changed title of document and core references to comply with PCI-SIG trademark conventions. Advanced support for IUS to v5.7.
8/08/07	7.5	Updated document for IP1 Jade Minor release. Advanced build to 163.
10/10/07	8.0	Updated device table, references to trademarks, release date.
3/24/08	8.5	Updated tools to ISE v10.1.
4/25/08	9.0	Added core v6 support for Virtex-5 FXT devices. Improved clock-management logic for PCI-X 133 MHz mode.
9/19/08	9.5	Updated to support ISE v10.1 Service Pack 3.
4/24/09	10.0	Updated to support ISE v11.1. Removed support for deprecated devices: Virtex-II, Virtex-II Pro, and Virtex-E.
4/19/10	11.0	Updated to support ISE v12.1. Updated "Part Numbers."

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