LogiCORE IP OBSAI v5.1

DS612 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP OBSAI core implements an OBSAI RP3 interface supporting RP3-01 at 768 Mb/s, 1.5 Gb/s, and 3 Gb/s line rates using GTP or GTX transceivers in Virtex®-5, Spartan®-6 and Virtex-6 FPGAs. 6 Gb/s line rate is supported in Virtex-6 devices.

The OBSAI core can be configured as a master or slave for use in base station or Remote RF Units (RRUs).

Features

- Designed to *OBSAI RP3 v4.2* specification[Ref 1]
- Supports CDMA or WCDMA/WiMAX 802.16/LTE framing formats
- GTP or GTX Transceivers support 768 Mb/s, 1.5 Gb/s, and 3 Gb/s line rates in Virtex-5 devices
- GTPA1 Transceivers support 768 Mb/s, 1.5 Gb/s, and 3 Gb/s line rates in Spartan-6 devices
- GTXE1 Transceivers support 768 Mb/s, 1.5 Gb/s, 3 Gb/s and 6 Gb/s line rates in Virtex-6 devices
- GTXE2 Transceivers support 768 Mb/s, 1.5 Gb/s, 3 Gb/s and 6 Gb/s line rates in Kintex™-7 and Virtex-7 devices
- Physical and Data Link Layer functions provided
- Supports RP1 Ethernet Messages[Ref 2], [Ref 3]
- Ethernet interface connects directly to LogiCORE IP MACs
- Supports RP1 Frame Clock Burst Messages
- Provides dedicated serial interfaces for RP1 frame clock bursts
- Supports fully configurable Modulo-Index transmission rules for RP3-01 message types
- Creates and processes Round Trip Time (RTT) messages
- Creates (Master mode core) or processes (Slave mode core) HW Reset Messages
- Provides Generic RP3 Messaging interfaces to support Application Layer messaging
- Supports RP3-01 auto-negotiation

LogiCORE IP Facts				
Core Specifics				
Supported Device Family[1]	Virtex-5 LXT/SXT/FXT[2] Virtex-6 LXT/SXT/HXT/CXT Spartan-6 LXT Virtex-7 Kintex-7			
Supported User Interfaces	AXI4-Lite Control/Status Interface			
Resources Used				
Configuration		**LUTs**	**FFs**	**Block RAMs**
Virtex-6 RP3-01 Master, Ethernet (default)		3460	2490	5
Provided with Core				
Documentation	Product Specification User Guide			
Design Files	NGC netlist			
Example Design	VHDL			
Test Bench	VHDL			
Constraints File	User Constraints File (.ucf)			
Simulation Model	VHDL			
Tested Design Tools				
Design Entry Tools	ISE v13.1 software			
Simulation[3]	Mentor Graphics ModelSim v6.6d			
Synthesis Tools	XST 13.1			
Support				
Provided by Xilinx, Inc.				

1. For the complete list of supported devices, see the readme.txt file for this core.
2. Virtex-5 LX20T FPGA is not supported due to clocking resource limitations.
3. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Features (Continued)

- Microprocessor-neutral Control/Status interface (Virtex-5 devices)
- AXI4-Lite Control/Status interface (Virtex-6, Spartan-6, Kintex-7 and Virtex-7 devices)
- Special Features: Delivered through CORE Generator™ software -- Hardware Verified

Overview

OBSAI RP3 is a high-speed serial interface designed to connect radio and baseband units within a wireless system. OBSAI RP3-01 is an extension to RP3, which provides the ability to site Remote RF Units (RRUs) at a different location from the Baseband Unit (BBU). RP3-01 enables RP1 messages defined in the *OBSAI RP1 Specification v2.1*[Ref 2] to be passed using only the RP3 physical interface. In RP3-01, the same serial RP3 interface carries both data and control information. The OBSAI RP3-01 interface is specified in the *OBSAI RP3 v5.1* specification[Ref 1].

Applications

Figure 1 shows a typical OBSAI system with a RRU.

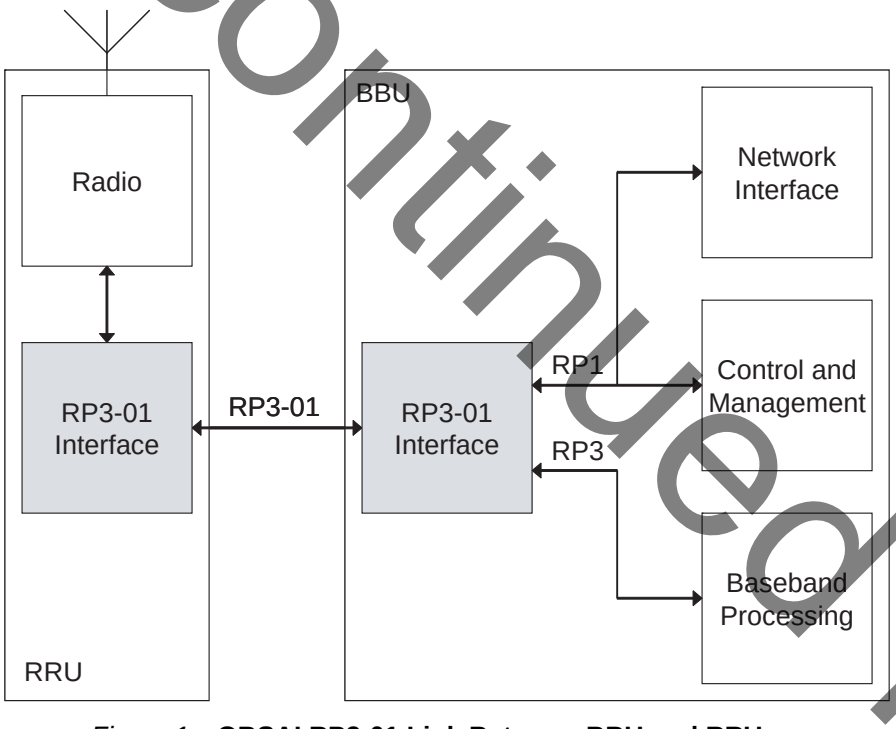

Figure 1: **OBSAI RP3-01 Link Between BBU and RRU**

Functional Description

Figure 2 illustrates a block diagram of the OBSAI RP3-01 core implementation.

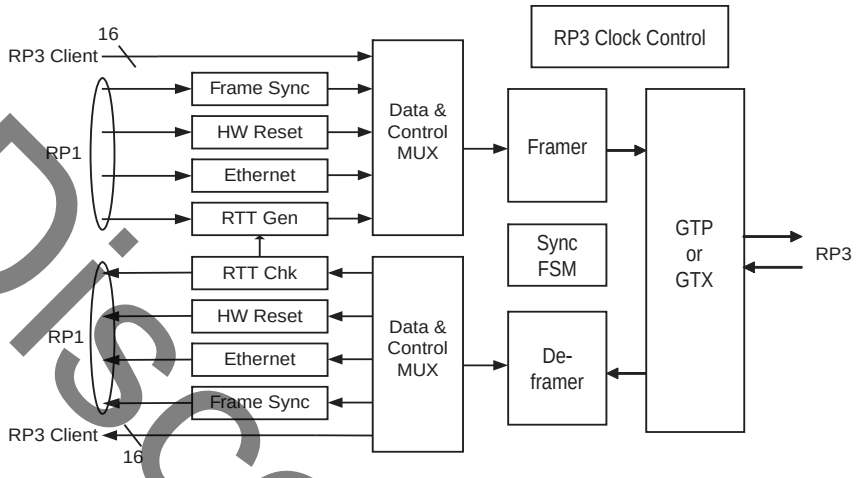

Figure 2: **OBSAI Core Implementation**

The major functional blocks of the core include:

- **Transmit Data and Control Multiplexer**. Inserts Control Messages in the RP3 data stream during control slots or empty data slots if permitted.
- **Transmit RP3-01 Control Interfaces**. Ethernet, O&M, and Timing Synchronizations Messages can be inserted in the RP3 data stream.
- **Transmit RP3 Generic Message Interface**. Allows the transmission of Application Layer generated RP3 messages such as Generic Control or Generic Packet types.
- **RP3 Transmit Framer**. Creates a single stream to the device-specific transceiver.
- **RP3 Receive De-framer**. Extracts messages from the data from the device-specific transceiver.
- **Receive Data and Control Demultiplexer**. Extracts Control messages from the stream and passes them to the RP3-01 control interfaces.
- **ReceiveRP3-01 Control Interfaces**. Extracts the Ethernet, O&M, and Frame Clock Burst data from the Control Messages.
- **Receive RP3 Generic Message Interface**. Extracts selected RP3 message types such as Generic Control or Generic Packet types and passes them to a separate interface for Application Layer use.
- **Clock Control**. Manages the switching of the GTP or GTX transceiver speed and generates the correct clocks to the other parts of the core and to the higher-layer logic created by the user.

Device Utilization

Virtex-5 FPGAs

Table 1 provides approximate device utilization figures for a core configured to support WCDMA framing format on a Virtex-5 SXT or LXT device. The values include the RocketIO™ transceiver and clock control logic.

Table 1: **Device Utilization - Virtex 5 FPGA**

Parameter Values				Device Resources					
Mode	Master/ Slave	Include Ethernet	Include Generic Messaging	LUTs	Registers	Block RAM (18K)	PLL	BUFG	BUFR
RP3	Master	N/A	N/A	1680	1360	1	1	4	1
	Slave	N/A	N/A	1665	1360	0	1	4	1
RP3-01	Master	N	N	2700	1930	1	1	4	1
	Master	Y	N	3250	2520	5	1	4	1
	Master	N	Y	2970	2270	3	1	4	1
	Slave	N	N	2660	2140	0	1	4	1
	Slave	Y	N	3200	2730	4	1	4	1
	Slave	N	Y	2930	2480	2	1	4	1

Note: All configurations use a single GTP_DUAL tile (FXT/LXT) or GTX_DUAL tile (FXT)

Virtex-6 FPGAs

Table 2 provides approximate device utilization figures for a core configured to support WCDMA framing format on a Virtex-6 LXT device. The values include the GTXE1 transceiver and clock control logic.

Table 2: **Device Utilization - Virtex 6 FPGA**

Parameter Values				Device Resources					
Mode	Master/ Slave	Include Ethernet	Include Generic Messaging	LUTs	Registers	Block RAM (18K)	MMCM	BUFG	BUFR
RP3	Master	N/A	N/A	1790	1340	1	1	4	1
	Slave	N/A	N/A	1780	1350	0	1	4	1
RP3-01	Master	N	N	2830	1910	1	1	4	1
	Master	Y	N	3460	2490	5	1	4	1
	Master	N	Y	3140	2240	3	1	4	1
	Slave	N	N	2980	2130	0	1	4	1
	Slave	Y	N	3580	2710	4	1	4	1
	Slave	N	Y	3290	2460	2	1	4	1

Note: All configurations use a single GTXE1 transceiver.

Spartan-6 FPGAs

Table 3 provides approximate device utilization figures for a core configured to support WCDMA framing format on a Spartan-6 LXT device. The values include the GTPA1 transceiver and clock control logic.

Table 3: **Device Utilization - Spartan-6 FPGA**

Parameter Values				Device Resources							
Mode	Master/ Slave	Include Ethernet	Include Generic Messaging	LUTs	Registers	Block RAM (18K)	PLL	DCM	BUFG	BUFIO2	BUFIO2FB
RP3	Master	N/A	N/A	1400	1330	1	1	1	5	2	2
	Slave	N/A	N/A	1380	1340	0	1	1	5	2	2
RP3-01	Master	N	N	2280	1900	1	1	1	5	2	2
	Master	Y	N	2750	2490	5	1	1	5	2	2
	Master	N	Y	2500	2240	3	1	1	5	2	2
	Slave	N	N	2550	2150	0	1	1	5	2	2
	Slave	Y	N	2860	2740	4	1	1	5	2	2
	Slave	N	Y	2620	2480	2	1	1	5	2	2

Note: All configurations use a single GTPA1 transceiver.

Kintex-7 and Virtex-7 FPGAs

Table 4 provides approximate device utilization figures for a core configured to support WCDMA framing format on Kintex-7 and Virtex-7 devices. The values include the GTPA1 transceiver and clock control logic.

Table 4: **Device Utilization - Kintex-7 and Virtex-7 FPGAs[1]**

Parameter Values				Device Resources					
Mode	Master/ Slave	Include Ethernet	Include Generic Messaging	LUTs	Registers	Block RAM (18K)	MMCM	BUFG[2]	BUFR[2]
RP3	Master	N/A	N/A	1150	1590	1	1	2	1
	Slave	N/A	N/A	1170	1590	0	1	2	1
RP3-01	Master	N	N	2450	2350	1	1	2	1
	Master	Y	N	2860	2960	5	1	2	1
	Master	N	Y	2620	2680	3	1	2	1
	Slave	N	N	2190	2490	0	1	2	1
	Slave	Y	N	2680	3100	4	1	2	1
	Slave	N	Y	2360	2820	2	1	2	1

1. All configurations use a single GTXE2 Transceiver.
2. Virtex-7 case, Kintex-7 uses 3 BUFG, 0 BUFR

References

1. *OBSAI RP3 Specification v4.2* (www.obsai.com)
2. *OBSAI RP1 Specification v2.1*. (www.obsai.com)
3. *IEEE Standard 803.3-2005* (www.standards.ieee.org/getieee802/)
4. *Xilinx AXI Reference Guide* (UG761)

Support

Visit www.xilinx.com/support for technical support. Xilinx provides technical support for this product when used as described in product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation or if customized.

Also see the IP Release Notes Guide for more information about the core.

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License. The core is generated using the Xilinx ISE® CORE Generator software, which is a standard component of the Xilinx ISE Design Suite.

For full access to the functionality of this core in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for pricing and availability of this and other Xilinx LogiCORE IP modules. Information about additional LogiCORE IP modules can be found on the Xilinx.com Intellectual Property page.

Related Information

Xilinx products are not intended for use in life-support appliances, devices, or systems. Use of a Xilinx product in such application without the written consent of the appropriate Xilinx officer is prohibited.

List of Acronyms

Table 5: **List of Acronyms**

Acronym	Spelled Out
AXI	Advanced eXtensible Interface
BBU	Baseband Unit
CDMA	Code-Division Multiple Access
FF	Flip-Flop
FPGA	Field Programmable Gate Array
Gb/s	Gigabits per second
HDL	Hardware Description Language
HW	Hardware
ISE	Integrated Software Environment
LTE	Long Term Evolution
LUT	Lookup Table
MAC	Media Access Controller
NGC	Native Generic Circuit
OBSAI	Open Base Station Architecture Initiative
PLL	Phase-Locked Loop
RAM	Random Access Memory
RRU	Remote RF Units
RTT	Round Trip Time
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
WCDMA	Wide band Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
8/8/07	1.0	Initial Xilinx release.
3/24/08	1.2	Update core to version 1.2; Xilinx tools v10.1.
4/16/08	2.1	Update core to version 2.1; Add FXT support.
4/24/09	3.1	Update core to version 3.1; Add RP3 v4.1 and Virtex-6 FPGA support.
6/24/09	3.2	Update core to version 3.2; Xilinx tools v11.2.
9/16/09	3.3	Update core to version 3.3; Xilinx tools v11.3.
4/19/10	4.1	Update core to version 4.1; Xilinx tools v12.1. Add 6G line rate and Spartan-6 FPGA support.
7/23/10	4.2	Update core to version 4.2; Xilinx tools v12.2.
3/1/11	5.1	Update core to version 5.1; Xilinx tools v13.1.

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