LogiCORE IP LTE RACH Detector v1.0

XMP041 August 15, 2011 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP LTE RACH Detector core decodes P-RACH data encoded according to the 3GPP TS 36.211 v9.0 (2009-12) Physical Channels and Modulation specification.

Features

- Channel detection for 3GPP TS 36.211 v9.0.0 (2009-12)
- Supports Formats 0-4
- Supports up to 64 roots
- Supports up to 4 antennas
- Supports Multiplexing in Frequency, for up to 6 frequency channels
- Variable Latency – supports all RACH configuration indexes
- Bit accurate C model available for the core
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- For use with the Xilinx CORE Generator™ software v13.2.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex®-7, Kintex™-7, Artix™-7, Zynq™-7000, Virtex-6, Virtex-5, Spartan®-6
Supported User Interfaces	Interface similar to AXI and can be connected to an AXI4-Stream Interface
Provided with Core	
Documentation	Product Specification Product Brief C Model User Guide
Design Files	VHDL and Netlist
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	C Model
Tested Design Tools	
Design Entry Tools	CORE Generator 13.2
Simulation(2)	Mentor Graphics ModelSim
Synthesis Tools	Not Provided.
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.
2. For the supported version of the tools, see the ISE Design Suite 13: Release Notes Guide

Overview

The LTE RACH detector core provides a RACH detection solution for the 3GPP TS 36.211 v9.0.0 (2009-12) specification. The LTE RACH detector searches through the received antenna samples and correlates against one or more (up to 64) RACH preamble sequences. The sequences are generated from Zadoff-Chu sequences, as defined in section 5.7 of 3GPP TS 36.211 v9.0.0 (2009-12).

At the eNode-B, the correlation results from the RACH detector are used to detect UE access attempts and compute/update UE transmission timing advance to ensure that the signals received from all UEs are time synchronized within the cyclic prefix (CP).

The RACH detector core performs a cyclic correlation for each Zadoff-Chu root it is configured to detect. This identifies all of the peaks resulting from each cyclic shifted copy of the root.

The architecture has been designed to provide efficient use of the FPGA. All processing-intensive and timing-critical operations are performed by the FPGA. The interface to the core can be attached to any bus-based system. The memory-mapped interface allows for simple integration and validation within the system.

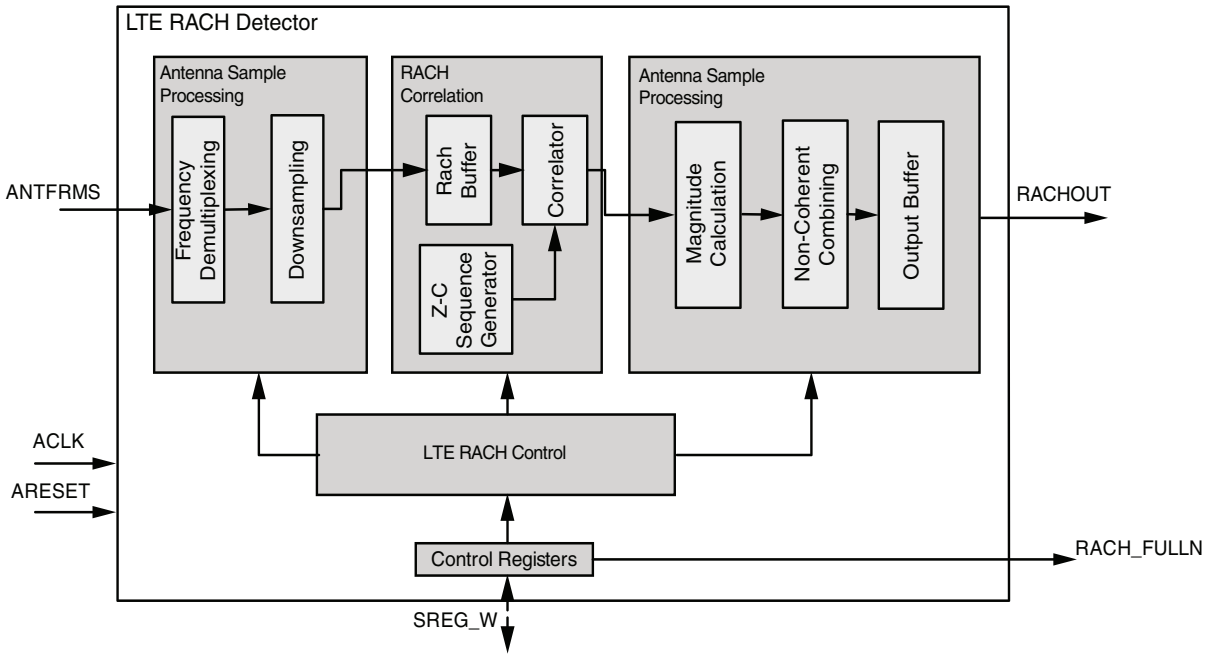

Figure 1: **internal Structure of the LTE RACH Detector Core**

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_rach_detector_eval/index.htm

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the IP Release Notes Guide (XTP025) for further information on this core. There is a link to all the DSP IP and then to the relevant core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

The LTE RACH detector core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator software v13.2. The CORE Generator software is shipped with Xilinx ISE Design Suite software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE RACH Detector product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/19/10	1.0	Initial Xilinx release.
06/22/11	1.1	Added new family support; ISE Design Suite 13.2.
08/15/11	1.2	Updated to include web registration information.

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