LogiCORE IP LTE PUCCH Receiver v1.0

XMP156 August 15, 2011 **Product Brief**

Overview

The Xilinx® LogiCORE™ IP LTE Physical Uplink Control Channel (PUCCH) Receiver implements an AXI4-Stream compliant, high-performance, optimized block for the 3GPP TS 36.211 v9.00 Physical uplink control channel.

The data and control for the core are input on independent AXI4-Stream channels as slave interfaces and the resulting status is output via an AXI4-Stream master interface.

Features

- Drop-in module for Virtex®-5, Virtex-6, Virtex-7 and Kintex™-7 FPGAs
- AXI4-Stream compliant interfaces
- Physical Uplink Control Channel Receiver for 3GPP TS 36.211
- TDD/FDD compliant
- Supports 1, 2 or 4 antenna operation
- Supports all format types including Mixed Format
- Supports both Normal and Shortened slots
- Supports normal and extended Cyclic Prefix
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- Bit-accurate C model
- Compliant with all required conformance tests (3GPP TS36.141 Base Station conformance testing)
- Customer demonstration testbench
- User guide available for detailed information on core usage.
- For use with Xilinx CORE Generatort™ tool 13.1

LogiCORE IP Facts	
Core Specifics	
Supported Device Family(1)	Kintex-7, Virtex-7 Virtex-5, Virtex-6
Supported User Interfaces	AXI4-Stream
Provided with Core	
Documentation	Product Brief Product Specification User Guide
Design Files	Netlist and C model
Example Design	N/A
Test Bench	VHDL
Constraints File	N/A
Simulation Model	UniSim, VHDL and Verilog
Tested Design Tools	
Design Entry Tools	CORE Generator tool 13.1 System Generator for DSP 13.1
Simulation	Mentor Graphics ModelSim 6.6d Cadence Incisive Enterprise Simulator (IES) 10.2 Synopsys VCS and VCS MX 2010.06 ISIM13.1
Synthesis Tools	XST 13.1
Support	
Provided by Xilinx, Inc.	

1. For the complete list of supported devices, see the release notes for this core.

Functional Description

The LTE PUCCH Receiver core provides a receiver solution for the 3GPP 36.211 Physical Uplink Control Channel (PUCCH). The architecture has been designed to provide efficient use of the FPGA resources while also offering a low bandwidth processor interface to reduce system-level overhead. Timing critical operations are performed by the FPGA.

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/pucch_eval/index.htm

References

1. 3GPP TS 36.211, v9.0.0 (2009-12), "Physical Channels and Modulation (Release 9)"
2. 3GPP TS 36.212, v9.0.0 (2009-12), "Multiplexing and channel coding (Release 9)"

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the IP Release Notes Guide (XTP025) for further information on this core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

The LTE PUCCH Receiver core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator software v13.1. The CORE Generator software is shipped with Xilinx ISE® Design Suite software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE UL PUCCH Receiver product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

Date	Version	Description of Revisions
03/01/2011	1.0	First release of the core.
08/15/11	1.1	Updated to include web registration information.

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