LogiCORE IP
LTE Fast Fourier Transform v1.0

XMP125 August 15, 2011 **Product Brief**

Introduction

The Xilinx LogiCORE™ IP LTE Fast Fourier Transform (FFT) implements all transform lengths required by the 3GPP LTE specification, including the 1536-point transform for 15 MHz bandwidth support.

Features

- Forward and inverse complex FFT, run-time configurable
- Supports transform point sizes 128, 256, 512, 1024, 1536, 2048
- Data sample precision b_x = 14 – 17
- Phase factor precision b_w = 14 – 17
- Optional run-time configurable point size
- Run-time configurable fixed scaling schedule, or unscaled datapath
- Bit/digit reversed or natural output order
- Optional cyclic prefix insertion
- Four architectures offer a trade-off between core size and transform time

Overview

The LTE FFT core computes an N-point forward DFT or inverse DFT where N can be 128, 256, 512, 1024, 1536, or 2048.

The input data is a vector of N complex values represented as dual b_x-bit two's-complement numbers, that is, b_x bits for each of the real and imaginary components of the data sample, where b_x is in the range 14 to 17 bits inclusive. Similarly, the phase factors b_w can be 14 to 17 bits wide.

The N element output vector is represented using b_x bits for each of the real and imaginary components of the output data. Input data is presented in natural order and the output data can be in either natural or bit/digit reversed order.

Two arithmetic options are available for computing the FFT:

- Full-precision unscaled arithmetic
- Scaled fixed-point arithmetic, with a user-specified scaling schedule

The point size N, the choice of forward or inverse transform, the scaling schedule and the cyclic prefix length are run-time configurable. Transform type (forward or inverse), scaling schedule and cyclic prefix length can be changed on a frame-by-frame basis. Changing the point size immediately resets the core.

Four architecture options are available:

- Pipelined, Streaming I/O
- Radix-4, Burst I/O
- Radix-2, Burst I/O
- Radix-2 Lite, Burst I/O

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_fft_eval/index.htm.

Ordering Information

The LTE Fast Fourier Transform IP core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator software v13.1. The CORE Generator software is shipped with Xilinx ISE® Design Suite software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE Fast Fourier Transform product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/23/10	1.0	Initial Xilinx release.
03/01/11	1.1	Support added for Virtex-7 and Kintex-7. ISE Design Suite 13.1
08/15/11	1.2	Updated to include web registration information.

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