JESD204 PHY v2.0

LogiCORE IP Product Guide

Vivado Design Suite

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XILINX
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Introduction

The Xilinx® LogiCORE™ IP JESD204 PHY core implements a JESD204B physical interface to simplify sharing serial transceiver channels between transmit and receive cores. This core is not intended to be used standalone and should only be used only in conjunction with the JESD204 core.

Note: This core is provided as standalone IP for use in the JESD204 IP example design only.

Features

- Designed to JEDEC® JESD204B [Ref 1]
- Supports 1 to 12 lane configurations
- Supports Subclass 0, 1, and 2
- Physical Layer functions provided
- Supports transceiver sharing between TX and RX cores

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™ Architecture, Zynq®-7000 All Programmable SoC, 7 Series
Supported User Interfaces	N/A
Resources	See Table 2-1, Table 2-2, and Table 2-3.
Provided with Core	
Design Files	RTL
Example Design	Verilog
Test Bench	Verilog
Constraints File	XDC
Simulation Model	Verilog
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The LogiCORE™ IP JESD204 PHY core implements a JESD204B Physical interface supporting line rates between 1.0 and 12.5 Gb/s on 1 to 12 lanes using GTX, GTH, or GTP transceivers. See the device data sheets listed in References for maximum line rates supported by each device and family. The JESD204 PHY core can be configured with independent transmit and receive line rates.

Figure 1-1 shows a block diagram of the JESD204 PHY core with no shared logic in the example design.

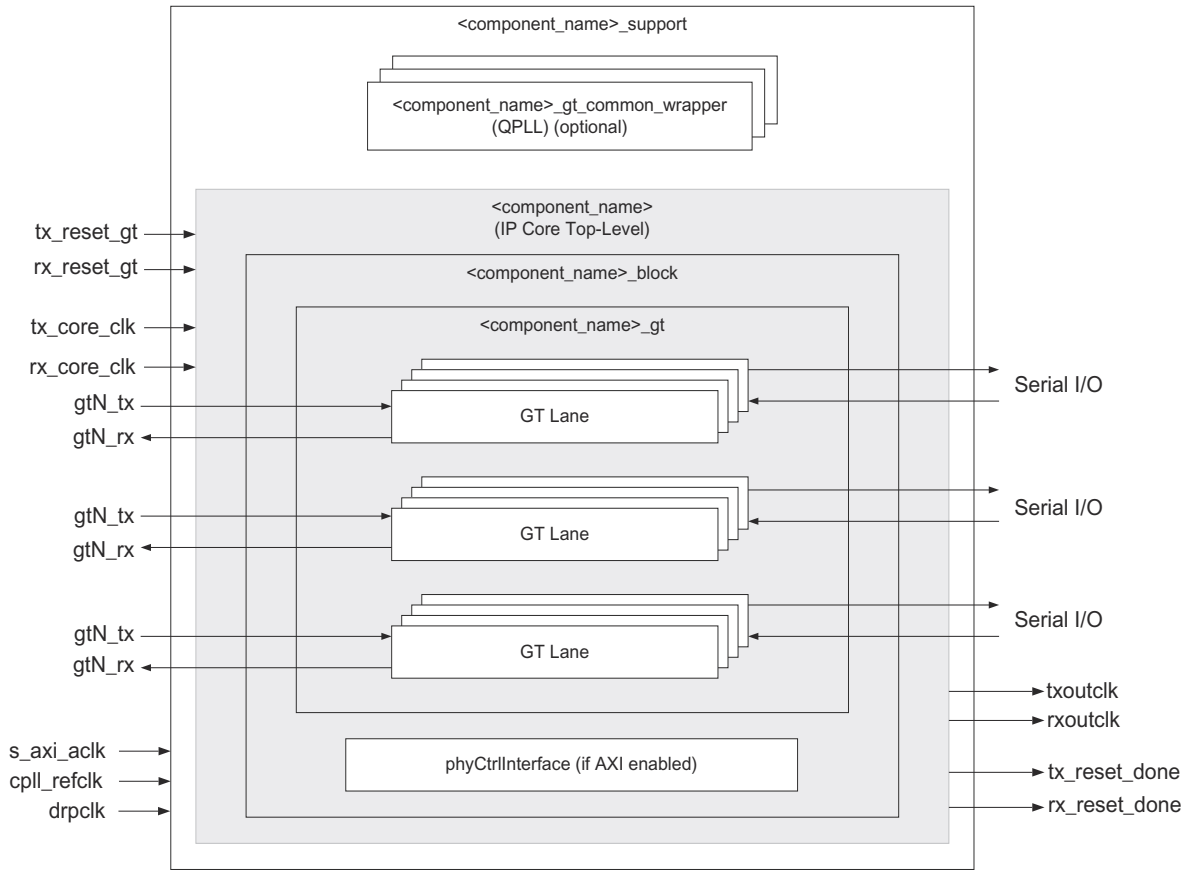

Figure 1-1: **JESD204 PHY Block Diagram – No Shared Logic in Example Design**

Figure 1-2 shows a block diagram of the JESD204 PHY core with shared logic in the core.

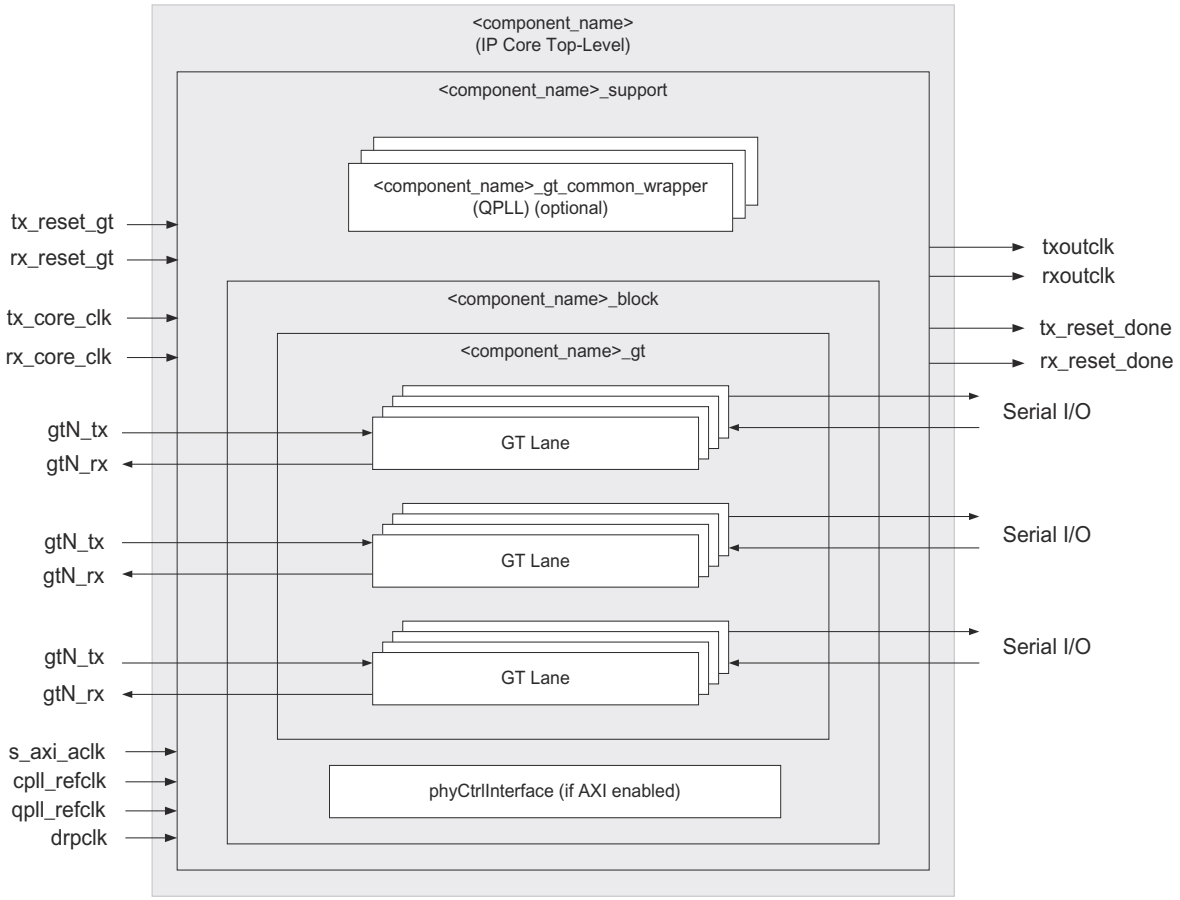

Figure 1-2: **JESD204 PHY Block Diagram – Shared Logic in Core**

When used in conjunction with the JESD204, the JESD204 PHY core is a fully-verified solution design delivered by using the Xilinx® Vivado® Design Suite. In addition, an example design is provided in Verilog. For more information, see the *JESD204 LogiCORE IP Product Guide* (PG066) [Ref 2].

Applications

The JESD204 PHY core is a sub-core of the JESD204 core. For application information, see the *JESD204 LogiCORE IP Product Guide* (PG066) [Ref 2]. Figure 1-3 shows a JESD204 PHY used in the JESD204 design.

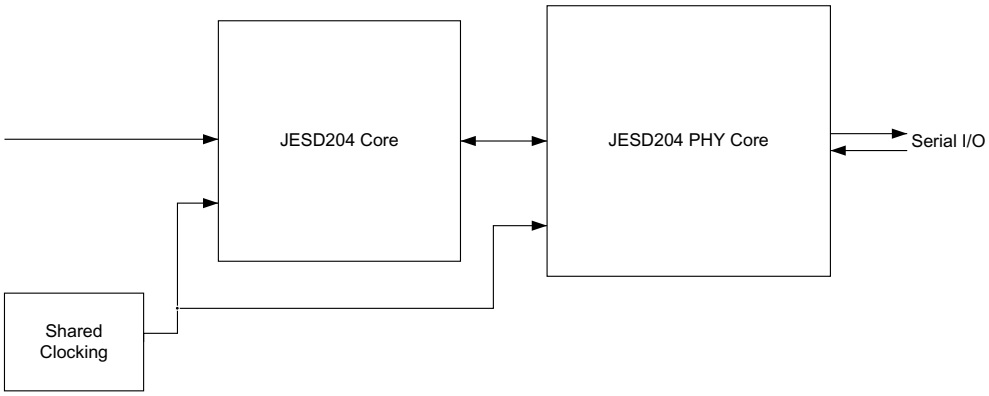

Figure 1-3: **JESD204 PHY Used in JESD204 Solution**

The JESD204 PHY allows complex transceiver and JESD204 core sharing to be accomplished. Figure 1-4, shown in Vivado IP integrator, utilizes two JESD204 PHY IPs to share transceivers between four JESD204 IP cores.

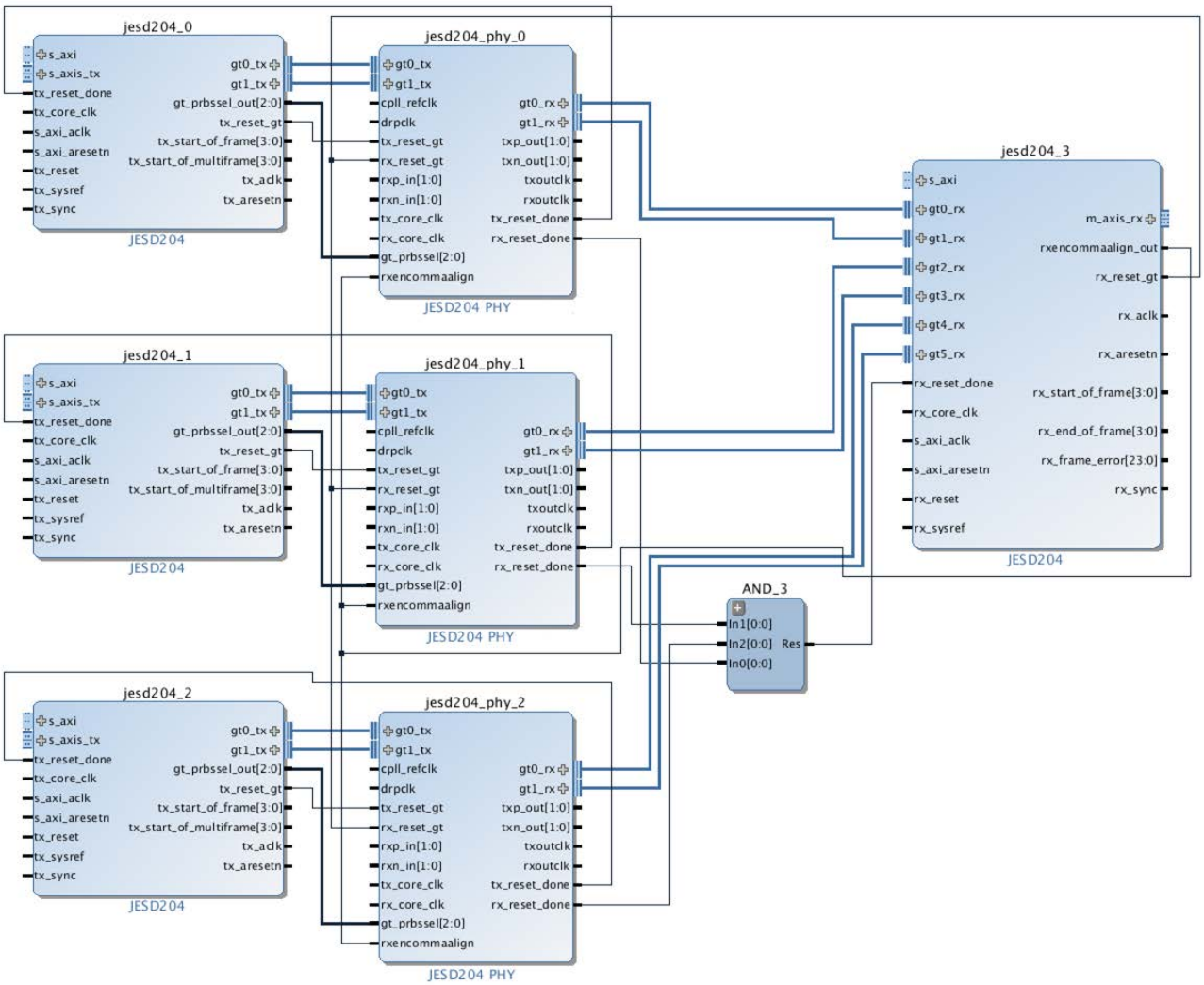

Figure 1-4: **IP Integrator Example Design**

The JESD204 PHY supports the simple one JESD204, one JESD204 PHY solution to the extremely complex multi-JED204 interleaved JESD204 PHY configurations. See the *JESD204 LogiCORE IP Product Guide* (PG066) [Ref 2] and the JESD204 Evaluation Lounge for complex JESD204 and JESD204 PHY transceiver sharing examples.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

This chapter details the resource utilization and ports for the JESD204 PHY core.

Performance

The core meets the performance specification of JESD204B. The maximum serial line rate is limited by the maximum GTX/GTP/GTH line rate for the chosen device. See the appropriate device data sheet listed in References in Appendix C.

Resource Utilization

Table 2-1, Table 2-2, and Table 2-3 provide approximate resource counts for the various core options.

Table 2-1: **Device Utilization – GTXE2/GTHE2 Devices (XC7K325T FFG900 -2)**

Number of Transceivers	FF	LUTs	BUFG
1	351	223	5
2	402	262	5
3	455	302	5
4	506	338	5
5	559	377	5
6	610	413	5
7	663	455	5
8	714	494	5
9	767	531	5
10	818	567	5
11	871	608	5
12	922	648	5

Table 2-2: **Device Utilization – GTPE2 Devices (XC7A200T FBG676 -2)**

Number of Transceivers	FF	LUTs	BUFG
1	406	276	6
2	531	377	6
3	656	476	6
4	781	577	6
5	906	676	6
6	1031	775	6
7	1156	876	6
8	1281	977	6

Table 2-3: **Device Utilization – GTHE3 Devices (XCVU095 FFVD 1924 -2 E ES1)**

Number of Transceivers	FF	LUTs	BUFG	BUFG_GT
1	440	252	3	1
2	711	424	3	2
3	982	658	3	3
4	1253	854	3	4
5	1524	1050	3	5
6	1795	1246	3	6
7	2066	1447	3	7
8	2337	1643	3	8
9	2608	1839	3	9
10	2879	2035	3	10
11	3150	2231	3	11
12	3421	2432	3	12

Port Descriptions

This section contains details about the JESD204 PHY ports.

Clock and Reset Ports

The clock and reset ports available on the delivered core component depend on the Shared Logic selection when customizing the core. Table 2-4 lists the ports available regardless of core settings.

Table 2-4: **Common Clock and Reset Ports**

Signal Name	Direction	Description
Clocks		
tx_core_clock	In	JESD204 core logic clock used to drive txusrclk2 of transceiver. Frequency = serial line rate/40.
rx_core_clock	In	JESD204 core logic clock used to drive rxusrclk2 of transceiver. Frequency = serial line rate/40.
txoutclk	Out	Output clock from transceiver. Can be used as JESD204 TX core clock when in Subclass 0 mode.
rxoutclk	Out	Output clock from transceiver. Can be used as JESD204 RX core clock when in Subclass 0 mode.
drp_clk	In	Dynamic Reconfiguration Port (DRP) clock. A free-running DRP clock is required for UltraScale devices and optional for 7 series devices.
cpll_refclk	In	Reference clock for the Transceiver Channel PLL.
qpll_refclk	In	Reference clock for the Quad Common PLL in 7 series.
qpll0/1_refclk	In	Reference clock for the Quad Common PLL(s) in UltraScale devices.
Resets		
tx_reset_gt	In	Core asynchronous logic reset.
rx_reset_gt	In	Core asynchronous logic reset.

Table 2-5 lists the ports that are available only when using Shared Logic in the example design.

Table 2-5: **Clocks and Resets for Shared Logic in Example Design**

Signal Name[(1)]	Direction	Description
Clocks		
txusrclk	In	Present only on GTP devices. Input Clock to transceiver.
rxusrclk	In	Present only on GTP devices. Input Clock to transceiver.
commonM_qpll_clk_in	In	Clock input for the QPLL (Quad M). Always present.
commonM_qpll_refclk_in	In	Reference clock input for the QPLL (Quad M). Always present.
commonM_pll0_clk_in	In	Reference clock input for the PLL (Quad M). Only present when PLL0 is selected.
commonM_pll0_refclk_in	In	Clock input for the PLL (Quad M). Only present when PLL0 is selected.
commonM_pll1_clk_in	In	Clock input for the PLL (Quad M). Only present when PLL0 is selected.
commonM_pll1_refclk_in	In	Reference clock input for the PLL (Quad M). Only present when PLL1 is selected.
commonM_qpll0_clk_in	In	Clock input for the QPLL (Quad M). Only present when QPLL0 is selected.

Table 2-5: **Clocks and Resets for Shared Logic in Example Design *(Cont'd)***

Signal Name[1]	Direction	Description
commonM_qpll0_refclk_in	In	Reference clock input for the QPLL (Quad M). Only present when QPLL0 is selected.
commonM_qpll1_clk_in	In	Clock input for the QPLL (Quad M). Only present when QPLL1 is selected.
commonM_qpll1_refclk_in	In	Reference clock input for the QPLL (Quad M). Only present when QPLL1 is selected.
Resets		
qpll_reset_out	Out	Reset output from transceiver logic to reset Common Block. Present only when QPLL selected.
qpll0_reset_out	Out	Reset output from transceiver logic to reset QPLL0 Common Block when QPLL0 is selected or the AXI-4 Lite Management Interface is enabled and at least one channel is using either QPLL0 or QLL1. ***Note:*** This port is only applicable to UltraScale devices.
qpll1_reset_out	Out	Reset output from transceiver logic to reset QPLL1 Common Block when QPLL1 is selected or the AXI-4 Lite Management Interface is enabled and at least one channel is using either QPLL0 or QLL1. ***Note:*** This port is only applicable to UltraScale devices.
commonM_pll0_reset_out	Out	Reset output from transceiver logic used to reset Common Block. Only present when PLL0 selected.
commonM_pll1_reset_out	Out	Reset output from transceiver logic used to reset Common Block. Only present when PLL1 selected.
pll_reset_out	Out	Reset output from transceiver used to reset Common Block. Only present on UltraScale devices.
mmcm_reset	Out	Reset output from transceiver to reset MMCM. Only present for GTP devices.

Notes:

1. M = Number of QUADs – 1

Table 2-6 lists the ports that are available only when using Shared Logic in the core.

Table 2-6: **Clocks for Shared Logic in Core**

Signal Name[1]	Direction	Description
Clocks		
commonM_qpll_clk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL enabled.
commonM_qpll_refclk_out	Out	Reference clock output from the QPLL (Quad M). Only present when QPLL enabled.
commonM_qpll_lock_out	Out	Lock output from the QPLL (Quad M). Only present when QPLL is enabled.

Table 2-6: **Clocks for Shared Logic in Core *(Cont'd)***

Signal Name[1]	Direction	Description
commonM_pll0_clk_out	Out	Clock output from the PLL (Quad M). Only present when PLL0 is enabled.
commonM_pll0_refclk_out	Out	Reference clock input from the PLL (Quad M). Only present when PLL0 is enabled.
commonM_pll0_lock_out	Out	Lock output from the PLL0 (Quad M). Only present when PLL0 is enabled.
commonM_pll1_clk_out	Out	Clock output from the PLL (Quad M). Only present when PLL0 is enabled.
commonM_pll1_refclk_out	Out	Reference clock output from the PLL (Quad M). Only present when PLL1 is enabled.
commonM_pll1_lock_out	Out	Lock output from the PLL1 (Quad M). Only present when PLL1 is enabled.
commonM_qpll0_clk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL0 is enabled.
commonM_qpll0_refclk_out	Out	Reference clock output from the QPLL (Quad M). Only present when QPLL0 is enabled.
commonM_qpll0_lock_out	Out	Lock output from the QPLL0 (Quad M). Only present when QPLL0 is enabled.
commonM_qpll1_clk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL1 is enabled.
commonM_qpll1_refclk_out	Out	Reference clock output from the QPLL (Quad M). Only present when QPLL1 is enabled.
commonM_qpll1_lock_out	Out	Lock output from the QPLL1 (Quad M). Only present when QPLL1 enabled.

Notes:

1. M = Number of QUADs – 1

Transceiver Interface Ports – TX

The transceiver ports available on the delivered core component depend on the Shared Logic selection when customizing the core; see Table 2-7 or Table 2-8.

Table 2-7: **Transceiver Interface Ports – Shared Logic in Example Design**

Signal Name	Direction	Description
gt*N*_txdata[31:0]	In	TX data to transceiver. *N* = 0 … [Lanes – 1]
gt*N*_txcharisk[3:0]	In	TX Char is K to transceiver. *N* = 0 … [Lanes – 1]
gt_prbssel[2:0][1]	In	PRBS select to transceiver.

Notes:

1. For UltraScale devices, the width of gt_prbssel is [3:0].

Table 2-8: **TX Core: Transceiver Interface Ports – Shared Logic in Core**

Signal Name	Direction	Description
txp_out[N:0]	Out	Positive differential serial data output N = (Lanes – 1)
txn_out[N:0]	Out	Negative differential serial data output N = (Lanes – 1)

Transceiver Interface Ports – RX

The transceiver ports available on the delivered core component depend on the Shared Logic selection when customizing the core; see Table 2-9 or Table 2-10.

Table 2-9: **Transceiver Interface Ports – Shared Logic in Example Design**

Signal Name	Direction	Description
gt*N*_rxdata[31:0]	Out	RX data from transceiver. *N* = 0 ... [Lanes – 1]
gt*N*_rxcharisk[3:0]	Out	RX Char is K from transceiver. *N* = 0 ... [Lanes – 1]
gt*N*_rxdisperr[3:0]	Out	RX disparity error from transceiver. *N* = 0 ... [Lanes – 1]
gt*N*_rxnotintable[3:0]	Out	RX Not In Table from transceiver. *N* = 0 ... [Lanes – 1]

Table 2-10: **RX Core: Transceiver Interface Ports – Shared Logic in Core**

Signal Name	Direction	Description
rxp_in[N:0]	In	Positive differential serial data input N = (Lanes – 1)
rxn_in[N:0]	In	Negative differential serial data input N = (Lanes – 1)

Transceiver Debug Interface

IMPORTANT: *The ports in the Transceiver Control and Status Interface must be driven in accordance with the appropriate GT user guide. Using the input signals listed in Table 2-11 and Table 2-12 might result in unpredictable behavior of the IP core.*

The transceiver debug interface (when present) provides access to transceiver control and status pins for debug purposes. See the appropriate transceiver user guide (*UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 10], *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 11], or *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 12]) for a detailed description of these pins.

Table 2-11: **Optional Transceiver Debug Ports (7 Series Devices)**

Signal Name[(1)(2)]	Direction	Clock Domain	Description
gtN_drpaddr[8:0]	In	drp_clk	DRP Address Bus
gtN_drpdi[15:0]	In	drp_clk	Data bus for writing configuration data from the FPGA logic resources to the transceiver.

Table 2-11: **Optional Transceiver Debug Ports (7 Series Devices) *(Cont'd)***

Signal Name[(1)(2)]	Direction	Clock Domain	Description
gtN_drpen	In	drp_clk	DRP Enable Signal 0 = No read or write operation performed 1 = Enables a read or write operation
gtN_drpwe	In	drp_clk	DRP Write Enable 0: = Read operation when DEN is 1 1 = Write operation when DEN is 1
gtN_drpdo[15:0]	Out	drp_clk	Data bus for reading configuration data from the GTX/GTH transceiver to the FPGA logic resources.
gtN_drprdy	Out	drp_clk	Indicates operation is complete for write operations and data is valid for read operations.
gtN_loopback[2:0]	In	Async	Transceiver loopback: • 000 = No loopback • 001 = Near-end PCS Loopback • 010 = Near-end PMA Loopback • 100 = Far-end PMA Loopback • 110 = Far-end PCS Loopback ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_txpostcursor[4:0]	In	tx_core_clock	Transmit Differential Driver control. (TX only) ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_txprecursor[4:0]	In	tx_core_clock	Transmit Differential Driver control. (TX only) ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_txdiffctrl[3:0]	In	Async	Transmit Differential Driver control. (TX only) ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_txpolarity	In	tx_core_clock	Transmit polarity control. (TX only) ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_rxpolarity	In	rx_core_clock	Receive polarity control. (RX only) ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_cplllock_out	Out	Async	Active-High signal indicating that the channel PLL has locked to the input reference clock.
gtN_eyescandataerror_out	Out	Async	Asserted when an EYESCAN error occurs.
gtN_eyescanreset_in	In	Async	This port is pulsed High to initiate the EYESCAN reset process.
gtN_eyescantrigger_in	In	rx_core_clock	A High on this port causes an EYESCAN trigger event.
gtN_rxbufreset_in	In	Async	This port is driven High and then deasserted to start the RX elastic buffer reset process.
gtN_rxbufstatus_out[2:0]	Out	rx_core_clock	RX Elastic Buffer Status

Table 2-11: **Optional Transceiver Debug Ports (7 Series Devices) *(Cont'd)***

Signal Name[(1)(2)]	Direction	Clock Domain	Description
gtN_rxbyteisaligned_out	Out	rx_core_clock	RX Byte Alignment Status
gtN_rxbyterealign_out	Out	rx_core_clock	RX Byte Alignment has changed.
gtN_rxcdrhold_in	In	Async	Hold the CDR control loop frozen.
gtN_rxcommadet_out	Out	rx_core_clock	RX Comma detect out
gtN_rxdfelpmreset_in	In	Async	DFE reset
gtN_rxlpmen_in	In	Async	LPM mode enable
gtN_rxmonitorout_out	Out	Async	RX Monitor Out
gtN_rxmonitorsel_in	In	Async	RX Monitor Out mode select
gtN_rxpcsreset_in	In	Async	PCS Reset
gtN_rxpd_in[1:0]	In	Async	RX Power Down ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_rxpmareset_in	In	Async	PMA Reset
gtN_rxprbscntreset_in	In	rx_core_clock	RX PRBS Counter Reset
gtN_rxprbserr_out	Out	rx_core_clock	RX PRBS Error Detect
gtN_rxprbssel_in	In	rx_core_clock	RX PRBS Select
gtN_rxresetdone_out	Out	rx_core_clock	RX Reset Done
gtN_rxstatus_out[2:0]	Out	rx_core_clock	Encodes RX status and error codes
gtN_txbufstatus_out[1:0]	Out	tx_core_clock	TX Elastic Buffer Status
gtN_txpcsreset_in	In	Async	TX PCS Reset
gtN_txinhibit	In	tx_core_clock	TX Inhibit
gtN_txpd_in	In	tx_core_clock	TX Power Down ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_txpmareset_in	In	Async	TX PMA Reset
gtN_txprbsforceerr_in	In	tx_core_clock	TX PRBS Force Error
gtN_txresetdone_out	Out	tx_core_clock	TX Reset Done
gtN_rxlpmhfhold_in	In	rx_core_clock	(GTP Only) LPM Mode Control
gtN_rxlpmhfoverden_in	In	rx_core_clock	(GTP Only) LPM Mode Control
gtN_rxlpmlfhold_in	In	rx_core_clock	(GTP Only) LPM Mode Control

Notes:

1. N is the number of the transceiver channels.
2. If you are migrating from a 7 series to an UltraScale architecture-based device, the prefixes of the optional transceiver debug ports for single-lane cores are changed from `gt0`, `gt1` to `gt`, and the postfix `_in` and `_out` are dropped. For multi-lane cores, the prefixes of the optional transceiver debug ports `gt(n)` are aggregated into a single port (see Table 2-12).

Table 2-12: **Optional Transceiver Debug Ports (UltraScale Architecture-Based Devices)**

Signal Name[(1)]	Direction	Clock Domain	Description
gtN_drpaddr [8:0]	In	drp_clk	DRP Address Bus ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_drpdi [15:0]	In	drp_clk	Data bus for writing configuration data from the FPGA logic resources to the transceiver. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_drpen	In	drp_clk	DRP Enable Signal 0 = No read or write operation performed 1 = Enables a read or write operation ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_drpwe	In	drp_clk	DRP Write Enable 0 = Read operation when DEN is 1 1 = Write operation when DEN is 1 ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_drpdo [15:0]	Out	drp_clk	Data bus for reading configuration data from the GTX/GTH transceiver to the FPGA logic resources. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gtN_drprdy	Out	drp_clk	Indicates operation is complete for write operations and data is valid for read operations. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_txpmareset [(LANES-1):0]	In	Async	This port is pulsed High to start the TX PMA reset process.
gt_txpcsreset [(LANES-1):0]	In	Async	This port is pulsed High to start the TX PCS reset process.
gt_txresetdone [(LANES-1):0]	Out	tx_core_clock	A High on this port indicates that the TX reset process has completed.
gt_rxpmareset [(LANES-1):0]	In	Async	This port is pulsed High to start the RX PMA reset process.
gt_rxpcsreset [(LANES-1):0]	In	Async	This port is pulsed High to start the RX PCS reset process.
gt_rxbufreset [(LANES-1):0]	In	Async	This port is driven High and then deasserted to start the RX elastic buffer reset process.
gt_rxpmaresetdone [(LANES-1):0]	Out	Async	A High on this port indicates that the RX PMA reset process has completed.
gt_rxresetdone [(LANES-1):0]	Out	rx_core_clock	A High on this port indicates that the RX reset process has completed.
gt_txbufstatus [(LANES*2)-1:0]	Out	tx_core_clock	Elastic Buffer Status

Table 2-12: **Optional Transceiver Debug Ports (UltraScale Architecture-Based Devices) *(Cont'd)***

Signal Name[(1)]	Direction	Clock Domain	Description
gt_rxbufstatus [(LANES*3)-1:0]	Out	rx_core_clock	RX Elastic Buffer Status
gt_cplllock [(LANES-1):0]	Out	refclk	Active-High signal indicating that the channel PLL has locked to the input reference clock.
gt_rxrate [(LANES*3)-1:0]	In	rx_core_clock	Link signaling rate control
gt_eyescantrigger [(LANES-1):0]	In	rx_core_clock	A High on this port causes an EYESCAN trigger event.
gt_eyescanreset [(LANES-1):0]	In	Async	This port is pulsed High to initiate the EYESCAN reset process.
gt_eyescandataerror [(LANES-1):0]	Out	Async	Asserted when an EYESCAN error occurs.
gt_loopback [(LANES*3)-1:0]	In	Async	Transceiver loopback: • 000 = No loopback • 001 = Near-end PCS Loopback • 010 = Near-end PMA Loopback • 100 = Far-end PMA Loopback • 110 = Far-end PCS Loopback ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_rxpolarity [(LANES-1):0]	In	rx_core_clock	Set High to invert the incoming serial data. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_txpolarity [(LANES-1):0]	In	tx_core_clock	Set High to invert the outgoing serial data. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_rxdfelpmreset [(LANES-1):0]	In	Async	Reset for the LPM and DFE datapath.
gt_rxlpmen [(LANES-1):0]	In	Async	Set to 1 to select the LPM datapath.
gt_txprecursor [(LANES*5)-1:0]	In	tx_core_clock	Transmitter pre-cursor pre-emphasis control. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_txpostcursor [(LANES*5)-1:0]	In	tx_core_clock	Transmitter post-cursor pre-emphasis control. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_txdiffctrl [(LANES*4)-1:0]	In	Async	Driver swing control. ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_txprbsforceerr [(LANES-1):0]	In	tx_core_clock	Set High to drive errors into the PRBS transmitter.
gtN_txinhibit	In	tx_core_clock	TX Inhibit

Table 2-12: **Optional Transceiver Debug Ports (UltraScale Architecture-Based Devices) *(Cont'd)***

Signal Name[(1)]	Direction	Clock Domain	Description
gt_rxprbssel [(LANES*4)-1:0]	In	rx_core_clock	Receiver PRBS checker test pattern control.
gt_rxprbserr [(LANES-1):0]	In	rx_core_clock	A High on this port indicates that PRBS errors have occurred.
gt_rxprbscntreset [(LANES-1):0]	In	rx_core_clock	Reset the PRBS error counter
gt_rxcdrhold [(LANES-1):0]	In	Async	Hold the CDR control loop frozen
gt_dmonitorout [(LANES*15-1):0]	Out	Async	Digital Monitor Output Bus
gt_rxdisperr [(LANES*4-1):0]	Out	rx_core_clock	Receiver disparity error indicator
gt_rxnotintable [(LANES*4-1):0]	Out	rx_core_clock	Receiver not in table error indicator
gt_rxcommadet [(LANES-1):0]	Out	rx_core_clock	A High on this port indicates that the comma alignment block has detected a valid comma.
gt_rxpd [(LANES-1):0]	In	Async	RX Power Down ***Note:*** Not present when AXI4-Lite Management Interface is enabled.
gt_txpd [(LANES-1):0]	In	tx_core_clock	TX Power Down ***Note:*** Not present when AXI4-Lite Management Interface is enabled.

Notes:

1. N is the number of the transceiver channels.

Register Space

The JESD204 PHY core is configured using an AXI4-Lite Register Interface. The register map is shown in Table 2-13.

Table 2-13: **PHY Address Register Map**

Offset	Register Name	Access Type
0x000	Version (0x000)	R
0x004	IP Configuration (0x004)	R
0x008	Number of Common DRP Interfaces (0x008)	R
0x00C	Number of Transceiver DRP Interfaces (0x00C)	R
0x010	Number of Transceiver Register Banks (0x010)	R
0x014	Timeout Enable (0x014)	R/W
0x018	Reserved	–

Table 2-13: **PHY Address Register Map *(Cont'd)***

Offset	Register Name	Access Type
0x01C	Timeout Value (0x01C)	R/W
0x020	cmm_interface_sel (0x020)	R/W
0x024	gt_interface_sel (0x024)	R/W
0x028 to 0x07F	Reserved	–
0x080	PLL Status (0x080)	R
0x084 to 0x0FF	Reserved	–
Common/Transceiver DRP Control		
0x100/0x200	Common (0x100)/Transceiver (0x200) DRP Select	R/W
0x104/0x204	Common (0x104)/Transceiver (0x204) DRP Address	R/W
0x108/0x208	Common (0x108)/Transceiver (0x208) DRP Write Data	R/W
0x10C/0x20C	Common (0x10C)/Transceiver (0x20C) DRP Read Data	R
0x110/0x210	Common (0x110)/Transceiver (0x210) DRP Reset	R/W
0x114/0x214	Common (0x114)/Transceiver (0x214) DRP Access Status	R
0x118/0x218	Reserved	–
0x11C/0x21C	Common (0x11C)/Transceiver (0x21C) DRP Access Complete	R
0x120 to 0x1FF/ 0x220 to 0x2FF	Reserved	–
Common QPLL Control		
0x300	PLL Select (0x300)	R/W
0x304	QPLL0 Power Down (0x304)	R/W
0x308	QPLL1 Power Down (UltraScale Only) (0x308)	R/W
0x30C to 0x3FF	Reserved	–
Transceiver Control – Bank 1		
0x400	Transceiver Select (Bank 1) (0x400)	R/W
0x404	RXPD (0x404) (RX Power Down)	R/W
0x408	CPLLPD (0x408) (CPLL Power Down)	R/W
0x40C	Transmit PLL Clock Select (0x40C)	R/W
0x410	Receive PLL Clock Select (0x410)	R/W
0x414	TX Postcursor (0x414)	R/W
0x418	TX Precursor (0x418)	R/W
0x41C	Loopback (0x41C)	R/W
0x420 to 0x4FF	Reserved	–
Transceiver Control – Bank 2		
0x500	Transceiver Select (Bank 2) (0x500)	R/W
0x504	TXPD (0x504)	R/W

Table 2-13: **PHY Address Register Map *(Cont'd)***

Offset	Register Name	Access Type
0x508	TXDIFFCTRL (0x508)	R/W
0x50C	TXINHIBIT (0x50C)	R/W
0x510	TXPOLARITY (0x510)	R/W
0x514 to 0x5FF	Reserved	–
Transceiver Control – Bank 3		
0x600	Transceiver Select (Bank 3) (0x600)	R/W
0x604	RXPOLARITY (0x604)	R/W
0x610 to 0xFF	Reserved	–

Table 2-14: **Version (0x000)**

Bits	Default Value	Description
31:24	–	Version: Major
23:16	–	Version: Minor
15:8	–	Version: Revision
7:0	–	Reserved (read 0x00)

Table 2-15: **IP Configuration (0x004)**

Bits	Default Value	Description
31:24	–	FPGA Type 0 = 7 series 1 = UltraScale All other values are reserved.
23:16	–	Speed Grade 1 = –1 2 = –2 3 = –3 All other values are reserved.
15:8	–	Package 1 = FF or RF 2 = FB 3 = FFV or FLV 4 = FBV All other values are reserved.
7:0	–	Transceiver Type 2 = GTX 3 = GTHE2 5 = GTHE3 All other values are reserved.

Table 2-16: **Number of Common DRP Interfaces (0x008)**

Bits	Default Value	Description
31:0	–	Reading this register returns the number of GT_COMMON blocks in the core. Normally one common block is included per four transceivers (See *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 10] or *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 11] for details). The number returned here can be used by software to loop round the correct number of times to configure all the QPLLs in the core using the DRP interfaces on the GT_COMMON block. The valid range for the "Common DRP Select" register is 1..N, where N is the value contained in this register.

Table 2-17: **Number of Transceiver DRP Interfaces (0x00C)**

Bits	Default Value	Description
31:0	–	Reading this register returns the number of GT_CHANNEL blocks (same as the number of lanes). The number returned here can be used by software to loop round the correct number of times to configure all the transceivers in the core using the DRP interfaces on the transceiver. The valid range for the "Transceiver DRP Select" register is 1..N, where N is the value contained in this register.

Table 2-18: **Number of Transceiver Register Banks (0x010)**

Bits	Default Value	Description
31:0	–	Reading this register returns the number of the number of lanes in the core. The number returned here can be used by software to loop round the correct number of times to access the registers which are common to all lanes. The valid range for the "Transceiver Select (PLL Control)" and "Transceiver Select (Bank 1 to 3)" registers is 1..N, where N is the value contained in this register.

Table 2-19: **Timeout Enable (0x014)**

Bits	Default Value	Description
31:1	–	Reserved
0	1	Enable the AXI4-Lite timeout. This ensures that transactions to the transceiver registers do not lock the AXI4-Lite bus which can happen if the transceiver is in reset or not being clocked when an access is attempted for example. If a timeout occurs during an AXI transaction, it is indicated on the bresp bus as a SLVERR response, allowing the firmware to act accordingly.

Table 2-20: **Timeout Value (0x01C)**

Bits	Default Value	Description
31:12	–	Reserved
11:0	128	Set the number of AXI clock cycles to wait before terminating the AXI4-Lite access without completing. If using timeout, the value must be modified according to the relationship between the AXI and DRP clock. The IP handles the DRP access by stretching the AXI interface response until it is completed. If the DRP clock is much slower than the AXI clock, this results in an unintentional timeout of the value is not increased. The timeout counts up so this value should be programmed with 4096-timeout. The complete timeout length is this value + 2 cycles. Valid timeout value are 0 to 4094. Care must be taken to not set to small a value. Base setting this value on the slowest clock of the set, rx_core_clk, tx_core_clk, and drpclk.

Table 2-21: **cmm_interface_sel (0x020)**

Bits	Default Value	Description
31:2	–	Reserved
1:0	–	Set the number corresponding to the Common DRP to be accessed. The range is 0 to 1-N, where N is the value returned in the Number of Common DRP Interfaces register (0x008). This value should match the value in 0x100 and 0x300 if the common block is present and being addressed.

Table 2-22: **gt_interface_sel (0x024)**

Bits	Default Value	Description
31:2	–	Reserved
1:0	–	Set the number corresponding to the Transceiver DRP to be accessed. The range is 0 to M-1, where M is the value returned in the Number of Transceiver DRP Interfaces register (0x00C). This value should match the value in 0x200, 0x400, 0x500, and 0x600 if a transceiver is being accessed.

Table 2-23: **PLL Status (0x080)**

Bits	Default Value	Description
31:5	–	Reserved
4	–	Returns 1 when a transmit reset is in progress.
3	–	Returns 1 when a receive reset is in progress.
2	–	Returns 0 when all the CPLLs are locked.
1	–	Returns 0 when all the QPLLs (7 series) or QPLL0s (UltraScale) are locked.
0	–	Returns 0 when all the QPLL1s are locked (UltraScale only, always returns 0 for 7 series devices).

Notes:

1. Reading all 0 means the core is ready.

Common/Transceiver DRP Control

The DRP interface provides a "mailbox" mechanism for read/write to multiple DRPs. Bits[31:30] of the DRP Address are used to auto-initiate a read or write of the DRP interface. A Status register is provided to allow you to check the access has completed without error. There are two mailboxes, one at 0x100 for the COMMON DRPs and one at 0x200 for the transceiver DRPs.

Table 2-24: **Common (0x100)/Transceiver (0x200) DRP Select**

Bits	Default Value	Description
31:0	–	Set the number corresponding to the DRP to be accessed. For Common DRPs the range is 0 to N-1, where N is the value returned in the "Number of Common DRP interfaces" register (0x008) and for Transceiver DRPs the range is 0 to M-1, where M is the value returned in the "Number of Common DRP interfaces" register (0x008). When programming this register, cmm_interface_sel (0x020), for the common, or gt_interface_sel (0x024) for the transceiver, should be set to the same value.

Table 2-25: **Common (0x104)/Transceiver (0x204) DRP Address**

Bits	Default Value	Description
31	–	Set to 1 to perform a write to the DRP.
30	–	Set to 1 to perform a read from the DRP.
29:0	–	DRP register address (See *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 10] or *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 11] for a complete DRP address map).

Notes:

1. The lower Bits[29:0] can be read/written without triggering a DRP access allowing the firmware to test the address value if required. If both upper bits are set the access is ignored as DRP cannot be read/written at the same time. This will result in 0x0 being read in these upper two bits.

Table 2-26: **Common (0x108)/Transceiver (0x208) DRP Write Data**

Bits	Default Value	Description
31:16	–	Reserved, the DRP registers are all 16 bits
15:0	–	Data to be written to the selected DRP register

Table 2-27: **Common (0x10C)/Transceiver (0x20C) DRP Read Data**

Bits	Default Value	Description
31:16	–	Reserved, the DRP registers are all 16 bits
15:0	–	Data read back from the selected DRP register

Table 2-28: **Common (0x110)/Transceiver (0x210) DRP Reset**

Bits	Default Value	Description
31:1	–	Reserved
0	0	Write a 1 to reset the DRP interface. Self-clearing. UltraScale only.

Table 2-29: **Common (0x114)/Transceiver (0x214) DRP Access Status**

Bits	Default Value	Description
31:3	–	Reserved
2	–	Access Type 0 = read 1 = write This register is only set when "DRP Access in Progress" bit is set to allow a read of all zeros check of the register for completion. Sticky on Timeout Error, updated on new DRP access.
1	–	Reserved
0	–	DRP Access in Progress Set on a write of 1 to either of the top two bits of DRP Address register and auto cleared when DRP data is valid.

Table 2-30: **Common (0x11C)/Transceiver (0x21C) DRP Access Complete**

Bits	Default Value	Description
31:1	–	Reserved
0	–	When asset to 1, the AXI4-Lite does not complete the final write to the DRP Address register until the DRP access has completed. When set, there is no need to poll the DRP Access in Progress bit of the DRP Access Status register.

DRP Access Sequence Example

Both the number of transceivers and common block present are held in the Configuration register bank and can be used as maximum values in the configuration loops, saving firmware regeneration.

As an example, to program each COMMON PLL block:

1. Read how many COMMON blocks exist in the system (`num_com` = AXI read 0x8).
2. Loop over each COMMON `i = 0; i < num_com; i++`.
3. Set the DRP number to access (0 to (`num_com` – 1)) (AXI Write i to 0x008). To write to the DRP,
   a. Program the value to write over the DRP interface (AXI Write <value> 0x108).
   b. Program the DRP address value also setting the write flag
4. To set the write flag, OR the address with 0x8000_0000 (AXI Write (<address> | 0x8000_0000) to 0x104). To read from the DRP,
   a. Program the DRP address value and also set the read flag.
5. To set the read flag, OR the address with 0x4000_0000 (AXI Write (<address> | 0x4000_0000) to 0x104).

Common QPLL Control

Table 2-31: **PLL Select (0x300)**

Bits	Default Value	Description
7:0	0	Set the number corresponding to the PLL DRP to be accessed. The range is 0 to N-1, where N is the value returned in the "Number of Common DRP interfaces" register (0x008). When programming this register, cmm_interface_sel (0x020) should be set to the same value.

Table 2-32: **QPLL0 Power Down (0x304)**

Bits	Default Value	Description
0	0	1 = Power Down QPLL (7 series) QPLL0 (UltraScale)

Table 2-33: **QPLL1 Power Down (UltraScale Only) (0x308)**

Bits	Default Value	Description
0	0	1 = Power Down QPLL1 (UltraScale Only)

Transceiver Control

The following controls are split into three banks internally to minimize the clock domain crossings required for each interface. This does require three separate writes to the select registers. The AXI read/write manages the clock domain crossing, with the result that the AXI accesses are longer than standard.

Table 2-34: **Transceiver Select (Bank 1) (0x400)**

Bits	Default Value	Description
7:0	0	Set the number corresponding to the Transceiver DRP to be accessed. The range is 0 to M-1, where M is the value returned in the "Number of Transceiver DRP interfaces" register (0x00C). When programming this register, gt_interface_sel (0x024) should be set to the same value.

Table 2-35: **RXPD (0x404)**

Bits	Default Value	Description
1:0	0	Power up or down the RX of the GT transceiver. 00 = Power state for normal operation. 11 = Power saving state with lowest power.

Table 2-36: **CPLLPD (0x408)**

Bits	Default Value	Description
0	0	1 = Power Down CPLL

Table 2-37: **Transmit PLL Clock Select (0x40C)**

Bits	Default Value	Description
1:0	0	Selects the PLL to drive the TX datapath: 00 = CPLL 10 = QPLL0 (UltraScale Only) 11 = QPLL (7 series) QPLL1 (UltraScale)

Table 2-38: **Receive PLL Clock Select (0x410)**

Bits	Default Value	Description
1:0	0	Selects the PLL to drive the RX datapath: 00 = CPLL 10 = QPLL0 (UltraScale Only) 11 = QPLL (7 series) QPLL1 (UltraScale)

Table 2-39: **TX Postcursor (0x414)**

Bits	Default Value	Description
4:0	0	Driver Swing Control. The default is user specified. All listed values are in mV_{PPD}.

[3:0]	mV_{PPD}
4'b0000	269
4'b0001	336
4'b0010	407
4'b0011	474
4'b0100	543
4'b0101	609
4'b0110	677
4'b0111	741
4'b1000	807
4'b1001	866
4'b1010	924
4'b1011	973
4'b1100	1,018
4'b1101	1,056
4'b1110	1,092
4'b1111	1,119

Note: The peak-to-peak differential voltage is defined when TXPOSTCURSOR = 5'b00000 and TXPRECURSOR = 5'b00000.

Table 2-40: **TX Precursor (0x418)**

<table>
<tr><th>Bits</th><th>Default Value</th><th>Description</th></tr>
<tr><td>4:0</td><td>0</td><td>Transmitter precursor TX pre-emphasis control. The default is user specified. All listed values (dB) are typical.
<table>
<tr><th>[4:0]</th><th>Emphasis (dB)</th><th>Coefficient Units</th></tr>
<tr><td>5'b00000</td><td>0.00</td><td>0</td></tr>
<tr><td>5'b00001</td><td>0.22</td><td>1</td></tr>
<tr><td>5'b00010</td><td>0.45</td><td>2</td></tr>
<tr><td>5'b00011</td><td>0.68</td><td>3</td></tr>
<tr><td>5'b00100</td><td>0.92</td><td>4</td></tr>
<tr><td>5'b00101</td><td>1.16</td><td>5</td></tr>
<tr><td>5'b00110</td><td>1.41</td><td>6</td></tr>
<tr><td>5'b00111</td><td>1.67</td><td>7</td></tr>
<tr><td>5'b01000</td><td>1.94</td><td>8</td></tr>
<tr><td>5'b01001</td><td>2.2</td><td>9</td></tr>
<tr><td>5'b01010</td><td>2.50</td><td>10</td></tr>
<tr><td>5'b01011</td><td>2.79</td><td>11</td></tr>
<tr><td>5'b01100</td><td>3.10</td><td>12</td></tr>
<tr><td>5'b01101</td><td>3.41</td><td>13</td></tr>
<tr><td>5'b01110</td><td>3.74</td><td>14</td></tr>
<tr><td>5'b01111</td><td>4.08</td><td>15</td></tr>
<tr><td>5'b10000</td><td>4.44</td><td>16</td></tr>
<tr><td>5'b10001</td><td>4.81</td><td>17</td></tr>
<tr><td>5'b10010</td><td>5.19</td><td>18</td></tr>
<tr><td>5'b10011</td><td>5.60</td><td>19</td></tr>
<tr><td>5'b10100</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b10101</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b10110</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b10111</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11000</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11001</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11010</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11011</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11100</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11101</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11110</td><td>6.02</td><td>20</td></tr>
<tr><td>5'b11111</td><td>6.02</td><td>20</td></tr>
</table>
Note: The TXPRECURSOR values are defined when the TXPOSTCURSOR = 5'b00000
Emphasis = 20log10(Vhigh/Vlow) = |20log10 (Vlow/Vhigh)|</td></tr>
</table>

Table 2-41: **Loopback (0x41C)**

Bits	Default Value	Description
2:0	0	Loopback modes are specialized configurations of the transceiver datapath where the traffic stream is folded back to the source. 000 = Normal operation 001 = Near-end PCS Loopback 010 = Near-end PMA Loopback 011 = Reserved 100 = Far-end PMA Loopback 101 = Reserved 110 = Far-end PCS Loopback

Table 2-42: **Transceiver Select (Bank 2) (0x500)**

Bits	Default Value	Description
7:0	0	Set the number corresponding to the Transceiver DRP to be accessed. The range is 0 to M-1, where M is the value returned in the "Number of Transceiver DRP interfaces" register (0x00C). When programming this register, gt_interface_sel (0x024) should be set to the same value.

Table 2-43: **TXPD (0x504)**

Bits	Default Value	Description
1:0	0	Power up or down the TX of the GT transceiver. 00 = Power state for normal operation. 11 = Power saving state with lowest power.

Table 2-44: **TXDIFFCTRL (0x508)**

<table>
<tr><th>Bits</th><th>Default Value</th><th>Description</th></tr>
<tr><td>3:0</td><td>0</td><td>Driver Swing Control. The default is user specified. All listed values are in mV_{PPD}.
<table>
<tr><th>[3:0]</th><th>mV_{PPD}</th></tr>
<tr><td>4'b0000</td><td>269</td></tr>
<tr><td>4'b0001</td><td>336</td></tr>
<tr><td>4'b0010</td><td>407</td></tr>
<tr><td>4'b0011</td><td>474</td></tr>
<tr><td>4'b0100</td><td>543</td></tr>
<tr><td>4'b0101</td><td>609</td></tr>
<tr><td>4'b0110</td><td>677</td></tr>
<tr><td>4'b0111</td><td>741</td></tr>
<tr><td>4'b1000</td><td>807</td></tr>
<tr><td>4'b1001</td><td>866</td></tr>
<tr><td>4'b1010</td><td>924</td></tr>
<tr><td>4'b1011</td><td>973</td></tr>
<tr><td>4'b1100</td><td>1,018</td></tr>
<tr><td>4'b1101</td><td>1,056</td></tr>
<tr><td>4'b1110</td><td>1,092</td></tr>
<tr><td>4'b1111</td><td>1,119</td></tr>
</table>
Note: The peak-to-peak differential voltage is defined when TXPOSTCURSOR = 5'b00000 and TXPRECURSOR = 5'b00000.</td></tr>
</table>

Table 2-45: **TXINHIBIT (0x50C)**

Bits	Default Value	Description
0	0	When High, this signal blocks transmission of TXDATA and forces MGTHTXP to 0 and MGTHTXN to 1.

Table 2-46: **TXPOLARITY (0x510)**

Bits	Default Value	Description
0	0	The TXPOLARITY port is used to invert the polarity of outgoing data. 0 = Not inverted. TXP is +ve, and TXN is -ve. 1 = Inverted. TXP is -ve, and TXN is +ve.

Table 2-47: **Transceiver Select (Bank 3) (0x600)**

Bits	Default Value	Description
7:0	0	Set the number corresponding to the Transceiver DRP to be accessed. The range is 0 to M-1, where M is the value returned in the "Number of Transceiver DRP interfaces" register (0x00C). When programming this register, gt_interface_sel (0x024) should be set to the same value.

Table 2-48: **RXPOLARITY (0x604)**

Bits	Default Value	Description
0	0	The RXPOLARITY port can invert the polarity of incoming data: 0 = Not inverted. RXP +ve and RXN -ve. 1 = Inverted. RXP is -ve and RXN is +ve.

Line Rate Switching

The recommended sequence for line rate switching is as follows:

- Ensure all valid data has been sent/received
- Power down the PLL (optional)
- Modify the PLL dividers through the appropriate DRP interface
- Select the correct `refclk` source for each transceiver in RX and TX
- Note if only using one direction the other can be powered down
- Adjust any other control signals
- Power up the PLLs (can be optional)
- Reset the PLL

DRP Mailboxes

The DRP mailbox interface gives complete access to the common and transceiver DRP address maps as given in the following:

- Ultrascale GTH *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 10]
- *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 11]

Xilinx recommends to reference the appropriate user guide, along with the data sheet for minimum/maximum `refclk` frequencies, line rates, etc. for the correct speed/package combination as well as consideration of system supply voltage.

The following sections highlight the registers of interest in the DRP register space when line rate switching. In general, the DRP registers are tightly packed and read modify write sequences should be used to modify the required bits.

UltraScale Devices DRP Registers

Three PLLs are available in UltraScale devices:

- QPLL0
- QPLL1
- CPLL

Outclk Dividers

Table 2-49 is applicable to both PLL types.

Table 2-49: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
007C	10:8	R/W	TXOUT_DIV	2:0	1	0	
					2	1	
					4	2	
					8	3	
					16	4	
0063	2:0	R/W	RXOUT_DIV	2:0	1	0	
					2	1	
					4	2	
					8	3	
					16	4	

QPLL0/1

The QPLL VCOs have different operating bands, see the device specific data sheet for more information.

- **QPLL0** – 9.8 to 16.3 GHz
- **QPLL1** – 8.0 to 13.0 GHz

The frequency out of the PLL is given by,

F(pllClkOut) = F(pllClkIn) × (N / M × 2)

Where N = QPLL(0/1)_FBDIV and M = QPLL(0/1)_REFCLK_DIV.

To calculate the line rate use,

F(linerate) = F(pllClkOut) × 2 / D

Where D = (R/T)XOUT_DIV.

Table 2-50: **Valid Divider Settings**

Factor	Attribute	Valid Settings
M	QPLL0_REFCLK_DIV QPLL1_REFCLK_DIV	1, 2, 3, 4
N	QPLL0_FBDIV QPLL1_FBDIV	16, 20, 32, 40, 64, 66, 80, 100
D	RXOUT_DIV TXOUT_DIV	1, 2, 4, 8, 16

Table 2-51 shows addresses of interest as well as the bits and encoding that must be used to select the correct divider values when interpreting the register content.

Table 2-51: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
0008	15:0	R/W	QPLL0_CFG0	15:0	0 to 65535	0 to 65535	
0009	15:0	R/W	COMMON_CFG0	15:0	0 to 65535	0 to 65535	
0010	15:0	R/W	QPLL0_CFG1	15:0	0 to 65535	0 to 65535	
0011	15:0	R/W	QPLL0_CFG2	15:0	0 to 65535	0 to 65535	
0014	7:0	R/W	QPLL0_FBDIV	7:0	16	14	
					20	18	
					32	30	
					40	38	
					64	62	
					66	64	
					80	78	
					100	98	
0018	11:7	R/W	QPLL0_REFCLK_DIV	7:0	1	16	
					2	0	
					3	1	
					4	2	
0088	15:0	R/W	QPLL1_CFG0	15:0	0 to 65535	0 to 65535	
0089	15:0	R/W	COMMON_CFG1	15:0	0 to 65535	0 to 65535	
0090	15:0	R/W	QPLL1_CFG1	15:0	0 to 65535	0 to 65535	
0091	15:0	R/W	QPLL1_CFG2	15:0	0 to 65535	0 to 65535	

Table 2-51: **DRP Address Map *(Cont'd)***

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
0094	7:0	R/W	QPLL1_FBDIV	7:0	16	14	
					20	18	
					32	30	
					40	38	
					64	62	
					66	64	
					80	78	
					100	98	
0098	11:7	R/W	QPLL1_REFCLK_DIV	7:0	1	16	
					2	0	
					3	1	
					4	2	

CPLL

The CPLL operating limits are shown for each transceiver type.

- **GTH** – 2.0 to 6.25 GHz

The frequency out of the PLL is given by,

F(pllClkOut) = F(pllClkIn) × (N1 × N2 / M)

Where N = QPLL(0/1)_FBDIV and M = QPLL(0/1)_REFCLK_DIV.

To calculate the line rate use,

F(linerate) = F(pllClkOut) × 2 / D

Where D = (R/T)XOUT_DIV.

Table 2-52: **Valid Divider Settings**

Factor	Attribute	Valid Settings
M	CPLL_REFCLK_DIV	1, 2
N2	CPLL_FBDIV	1, 2, 3, 4, 5
N1	CPLL_FBDIV_45	4, 5
D	RXOUT_DIV TXOUT_DIV	1, 2, 4, 8

Table 2-53 shows the addresses of interest as well as the bits and encoding that must be used to select the correct divider values when interpreting the register content.

Table 2-53: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
0028	15:8	R/W	CPLL_FBDIV	7:0	1	16	N2
					2	0	
					3	1	
					4	2	
					5	3	
0028	7	R/W	CPLL_FB_DIV_45	0	4	0	N1
					5	1	
002A	15:11	R/W	CPLL_REFCLK_DIV	4:0	1	16	M
					2	0	
002B	15:0	R/W	CPLL_INIT_CFG0	15:0	0 to 65535	0 to 65535	

7 Series FPGAs DRP Registers

Two PLLs are available in 7 series FPGAs:

- QPLL
- CPLL

Outclk Dividers

These are applicable to both PLL types.

Table 2-54: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
0088	6:4	R/W	TXOUT_DIV	2:0	1	0	
					2	1	
					4	2	
					8	3	
					16	4	

Table 2-54: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
0088	2:0	R/W	RXOUT_DIV	2:0	1	0	
					2	1	
					4	2	
					8	3	
					16	4	

QPLL

The QPLL VCO operates within two different operating bands, see the device specific data sheet for more information. Note that if switching between these bands, Bit[6] in the QPLL_CFG register must be modified to select the correct band.

- **GTX Lower** – 5.93 to 8.0 GHz
- **GTX Upper** – 9.8 to 12.5 GHz
- **GTH** – 8.0 to 13.1 GHz

The frequency out of the PLL is given by,

F(pllClkOut) = F(pllClkIn) × (N / M × 2)

Where N = QPLL(0/1)_FBDIV and M = QPLL(0/1)_REFCLK_DIV.

To calculate the line rate use,

F(linerate) = F(pllClkOut) × 2 / D

Where D = (R/T)XOUT_DIV.

Table 2-55: **Valid Divider Settings**

Factor	Attribute	Valid Settings
M	QPLL_REFCLK_DIV	1, 2, 3, 4
N	QPLL_FBDIV QPLL_FBDIV_RATIO	16, 20, 32, 40, 64, 66*, 80, 100
D	RXOUT_DIV TXOUT_DIV	1, 2, 4, 8, 16

Table 2-56 shows the addresses of interest as well as the bits and encoding that must be used to select the correct divider values when interpreting the register content.

Table 2-56: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
0032	15:0	R/W	QPLL_CFG	15:0	0 to 65535	0 to 65535	Reserved. This attribute is the configuration setting for the QPLL. QPLL_CFG[6] selects the QPLL frequency band. 0 = Upper band 1 = Lower band The recommended value from the 7 series FPGAs Transceivers Wizard should be used.
0033	15:11	R/W	QPLL_REFCLK_DIV	4:0	1	16	
					2	0	
					3	1	
					4	2	
0033	10:0	R/W	QPLL_CFG	26:16	0 to 2047	0 to 2047	
0036	9:0	R/W	QPLL_FBDIV	9:0	0 to 1023	0 to 1023	Supported divider values (16,20,32,40,64,66,80,100)
0037	6	R/W	QPLL_FBDIV_RATIO	0	0 to 1	0 to 1	*Set to 1 for all N values apart from N = 66, then set to 0

CPLL

The CPLL operating limits are shown for each transceiver type.

- **GTX** – 1.6 to 3.3 GHz
- **GTH** – 1.6 to 5.16 GHz

The frequency out of the PLL is given by,

F(pllClkOut) = F(pllClkIn) × (N1 × N2 / M)

Where N = QPLL(0/1)_FBDIV and M = QPLL(0/1)_REFCLK_DIV.

To calculate the line rate use,

F(linerate) = F(pllClkOut) × 2 / D

Where D = (R/T)XOUT_DIV.

Table 2-57: **Valid Divider Settings**

Factor	Attribute	Valid Settings
M	CPLL_REFCLK_DIV	1, 2
N2	CPLL_FBDIV	1, 2, 3, 4, 5
N1	CPLL_FBDIV_45	4, 5
D	RXOUT_DIV TXOUT_DIV	1, 2, 4, 8

Table 2-58 shows the addresses of interest as well as the bits and encoding that must be used to select the correct divider values when interpreting the register content.

Table 2-58: **DRP Address Map**

DRP Addr (Hex)	DRP Bits	R/W	Attribute Name	Bits	Encoding	DRP Encoding	Notes
005C	15:8	R/W	CPLL_CFG	7:0	0 to 255	0 to 255	
005D	15:0	R/W	CPLL_CFG	23:8	0 to 65535	0 to 65535	
005E	12:8	R/W	CPLL_REFCLK_DIV	4:0	1	16	M
					2	0	
005E	7	R/W	CPLL_FB_DIV_45	0	4	0	N1
					5	1	
005E	6:0	R/W	CPLL_FBDIV	6:0	1	16	N2
					2	0	
					3	1	
					4	2	
					5	3	

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core. The JESD204 PHY core can be used in two modes:

- The JESD204 PHY core is instantiated automatically by the JESD204 core during generation. This is transparent, and all ports and parameters are controlled by the JESD204 IP. Using the IP in this mode requires no user intervention and is not described in this document; see the *JESD204 LogiCORE IP Product Guide* (PG066) [Ref 2] for details about this mode. This mode is fully supported for production systems except in UltraScale™ devices.
- The JESD204 PHY core is instantiated in the example design provided with the JESD204 IP as a stand-alone IP core. In this case, the JESD204 PHY IP top level is available directly for instantiation in designs, and the JESD204 PHY IP GUI is available. This chapter describes using the JESD204 PHY in this mode.

JESD204 PHY Configuration Options

The JESD204 PHY can be generated in six main logical configurations.

Table 3-1: **JESD204 PHY Configuration Options**

AXI Enabled	Shared Logic	Transceiver Debug	Description
0	0	0	No AXI logic present, no COMMON.
0	0	1	No AXI logic present, no COMMON, current JESD204 transceiver ports list.
0	1	0	No AXI logic present, COMMON in core.
0	1	1	No AXI logic present, COMMON in core, current JESD204 transceiver ports list.
1	0	0	AXI logic present, no COMMON or COMMON AXI control registers.
1	0	1	AXI logic present, no COMMON or COMMON AXI control registers, transceiver debug ports are minus ports mapped to AXI control.
1	1	0	AXI logic present, COMMON in core.
1	1	1	AXI logic present, COMMON in core, transceiver debug ports are minus ports mapped to AXI control.

The common PLL DRP interface is not presented at the JESD204 PHY core output ports under any circumstance and can only be accessed with the AXI interface enabled and a QPLL selected as a `refclk` source.

In UltraScale devices, when the AXI interface is enabled and QPLL0/1 is selected as one of the PLLs, both PLL `refclk` ports appear. This is different to non-AXI mode where only the `refclk` of the selected PLL appears. This is to maximize flexibility when using the AXI interface for line rate switching.

IMPORTANT: *When used as a sub-core of the JESD204 core, AXI is disabled by default and cannot be enabled. You must use the JESD204 core with* ***Shared Logic in Example Design*** *and a separate JESD204 PHY to get access to the AXI JESD204 PHY interface.*

General Design Guidelines

This section includes tips about getting started with the JESD204 PHY core.

Use the Example Design as a Starting Point

Each instance of the JESD204 PHY core created by the Vivado® Design Suite is delivered with an example design that can be implemented in an FPGA and simulated. This design can be used as a starting point for your own design or can be used to troubleshoot your application, if necessary.

See Chapter 5, Example Design for information about using and customizing the example designs for the JESD204 PHY core. For more information on the Vivado IP integrator, see the *JESD204 LogiCORE IP Product Guide* (PG066) [Ref 2].

Degree of Difficulty

JESD204 designs are challenging to implement in any technology, and the degree of difficulty is further influenced by:

- Maximum system clock frequency
- Targeted device architecture
- Nature of your application

All JESD204 implementations require careful attention to system performance requirements. Pipelining, logic mapping, placement constraints, and logic duplication are all methods that help boost system performance.

Clocking

This section describes the options available for clocking the JESD204 PHY core and the transceiver(s). The following clocks are used in the JESD204 PHY core.

- **DRP Clock** – The transceiver requires an auxiliary clock for internal use and also for the reset state machines within the JESD204 PHY core. See the appropriate device family data sheet for the min and max DRP clock frequencies permitted.
- **Core Clock** – The JESD204 PHY core operates using a 32-bit (4-byte) datapath. The device clock for the core logic therefore runs at one quarter of the byte clock rate (1/ 40^{th} of the serial line rate). For the JESD204 and JESD204 PHY cores, this is referred to as the core clock.
- **Reference Clock** – The GTP/GTX/GTH serial transceivers require a stable, low-jitter reference clock that has a device and speed grade dependant range. In some circumstances, the same source clock can supply both the reference clock and core clock. Two reference clocks are required if both CPLL and QPLL (GTX/GTH devices) or PLL0 and PLL1 (GTP devices) are selected in the GUI.
- **AXI4-Lite Configuration Interface Clock** – Required if the AXI is enabled. This is asynchronous to any other clock and can be driven by the processor subsystem.

Resets

Separate resets are provided for transmit and receive directions. This enables the JESD204 PHY core to be used by a transmit JESD204 link and a receive JESD204 link independently. There is no system reset. The system reset causes the JESD204 cores attached to the JESD204 PHY to reset the JESD204 PHY.

- **Transmit Reset** – The transmit reset input (`tx_reset_gt`) initiates a complete transceiver reset sequence for the transmit logic, and `tx_reset_done` is asserted when the reset sequence is complete.
- **Receive Reset** – The receive reset input (`rx_reset_gt`) initiates a complete transceiver reset sequence for the receive logic, and `rx_reset_done` is asserted when the reset sequence is complete.

Protocol Description

See the *JESD204 LogiCORE IP Product Guide* (PG066) for a full description of the protocol [Ref 2].

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5].

Note: Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Configuration Tab

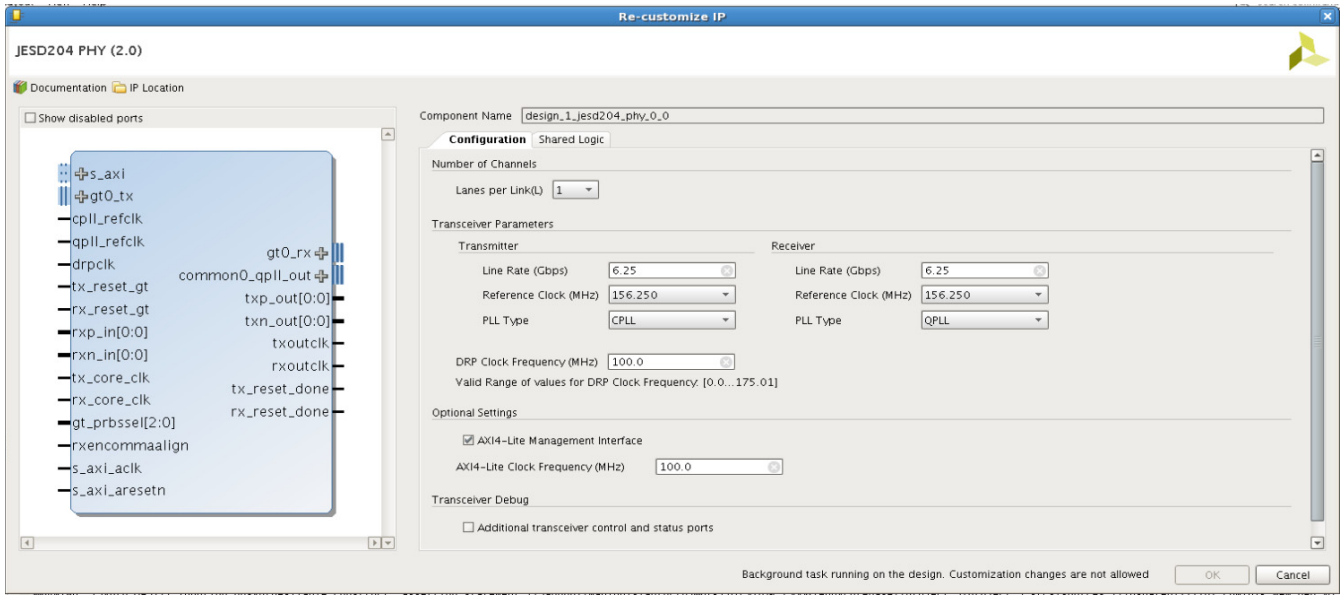

Figure 4-1: **Configuration Tab**

- **Number of Channels (Transceivers)**
  - **Lanes per Link** – The core supports 1 to 12 lanes. The number of transmit lanes always matches the number of receive lanes. For asymmetric interfaces, multiple cores can be generated and multiple PHY cores can be connected to a single JESD204 core.
- **Transceiver Parameters, Transmitter, and Receiver**
  - **Line Rate** – The serial line rate in Gb/s can be selected for transmit and receive independently. The minimum rate is 1 Gb/s and the maximum depends on the chosen device and speed grade.
  - **Reference Clock** – The reference clock must be selected from the drop-down list, which presents a list of valid reference clock frequencies for the selected line rate. Independent reference clocks can only be selected if different PLLs are selected for transmit and receive.
  - **PLL Type** – Select the QPLL or CPLL for transmit and receive. See the appropriate device transceiver user guide for more details and limitations.
  - **DRP Clock Frequency** – The frequency of the DRP clock being applied to the core so reset delays can be adjusted by the reset state machines.
- **Optional Settings**
  - **AXI4-Lite Management Interface** – Select to include the AXI4-Lite configurations interface. This allows AXI-based access to the Transceiver and Common DRPs along with a selection of transceiver pins that allow line rate switching in the core.

  - **AXI4-Lite Clock Frequency** – The AXI4-Lite clock can be connected to the main processor clock. When applicable, the clock domain boundary crossings are handled inside the IP to simplify implementation. Also, when a clock boundary is involved the AXI access is stretched, resulting in an extended access time.

- **Transceiver Debug** – Select to include additional transceiver control and status ports for debugging purposes. See Transceiver Debug Interface in Chapter 2 for more information.

Shared Logic Tab

The JESD204 PHY can be generated with Shared Logic (Quad PLL(s)) included in the core or with Shared Logic included with the example design. Shared Logic should always be included in the core when using the JESD204 PHY with a JESD204 IP core.

User Parameters

Table 4-1 shows the relationship between the GUI fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl console).

Table 4-1: **Vivado IDE Parameter to User Parameter Relationship**(1)

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Lanes per Link	C_LANES	2
Line Rate		
Transmit	GT_Line_Rate	6.25
Receive	RX_GT_Line_Rate	6.25
Reference Clock		
Transmit	GT_REFCLK_FREQ	156.25
Receive	RX_GT_REFCLK_FREQ	156.25
PLL Type		
Transmit	C_PLL_SELECTION	0 (= CPLL)
Receive	RX_PLL_SELECTION	0 (= CPLL)
DRP Clock Frequency	DRPCLK_FREQ	10.0
Shared Logic	SupportLevel	1 (= Include Shared Logic in Core)
Transceiver Debug	TransceiverControl	FALSE
AXI-Lite Interface	AXI_Lite	FALSE

Notes:

1. Parameters and default values will differ based on the selected device.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Constraining the Core

This section describes how to constrain a design containing the JESD204 core. This is accomplished by using the XDC delivered with the core at generation time. An additional XDC file is generated with the IP example design; only the core XDC file should be used in user designs.

Required Constraints

This section defines the constraint requirements for the core. Constraints are provided in several XDC files which are delivered with the core and the example design to give a starting point for constraints for the user design.

There are four XDC constraint files associated with this core:

- `<corename>_example_design.xdc`
- `<corename>_ooc.xdc`
- `<corename>.xdc`
- `<corename>_clocks.xdc`

The first is used only by the example design; the second file is used for Out Of Context support where this core can be synthesized without any wrappers; the third file is the main XDC file for this core.

Clock Frequencies

The reference clock and core clock frequency constraints vary depending on the selected line rate and reference clock when generating the core. See the generated XDC for details.

Clock Domains

There are also several paths where clock domains are crossed. These include the management interface. See the generated XDC file for details.

Clock Management

Reference clock and core clock resources require location constraints appropriate to your top level design.

Clock Placement

Reference clock input should be given location constraints appropriate to your top level design and to the placement of the transceivers.

Core clock input (if required) should be given location constraints appropriate to your top level design.

Banking

All ports should be given location constraints appropriate to your top level design within banking limits.

Transceiver Placement

Transceivers should be given location constraints appropriate to your design. In some cases, example transceiver location constraints can be found in the example design XDC file. For 7 series devices, the GT location constraints are in the transceiver's XDC file.

I/O Standard and Placement

All ports should be given I/O standard and location constraints appropriate to your top level design.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6].

IMPORTANT: *For cores targeting 7 series or Zynq-7000 AP SoC devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.*

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

The JESD204 PHY core is not intended to be used as a standalone solution. However, an example design does exist for the IP core. The example design is a lightweight harness that can operate in external TX to RX loopback or as independent RX/TX channel mode. See the example design provided with the JESD204 IP for a more detailed example of the use of the *JESD204 LogiCORE IP Product Guide* (PG066) [Ref 2].

To open the example design, right-click the IP and select **Open IP Example Design** as shown in Figure 5-1.

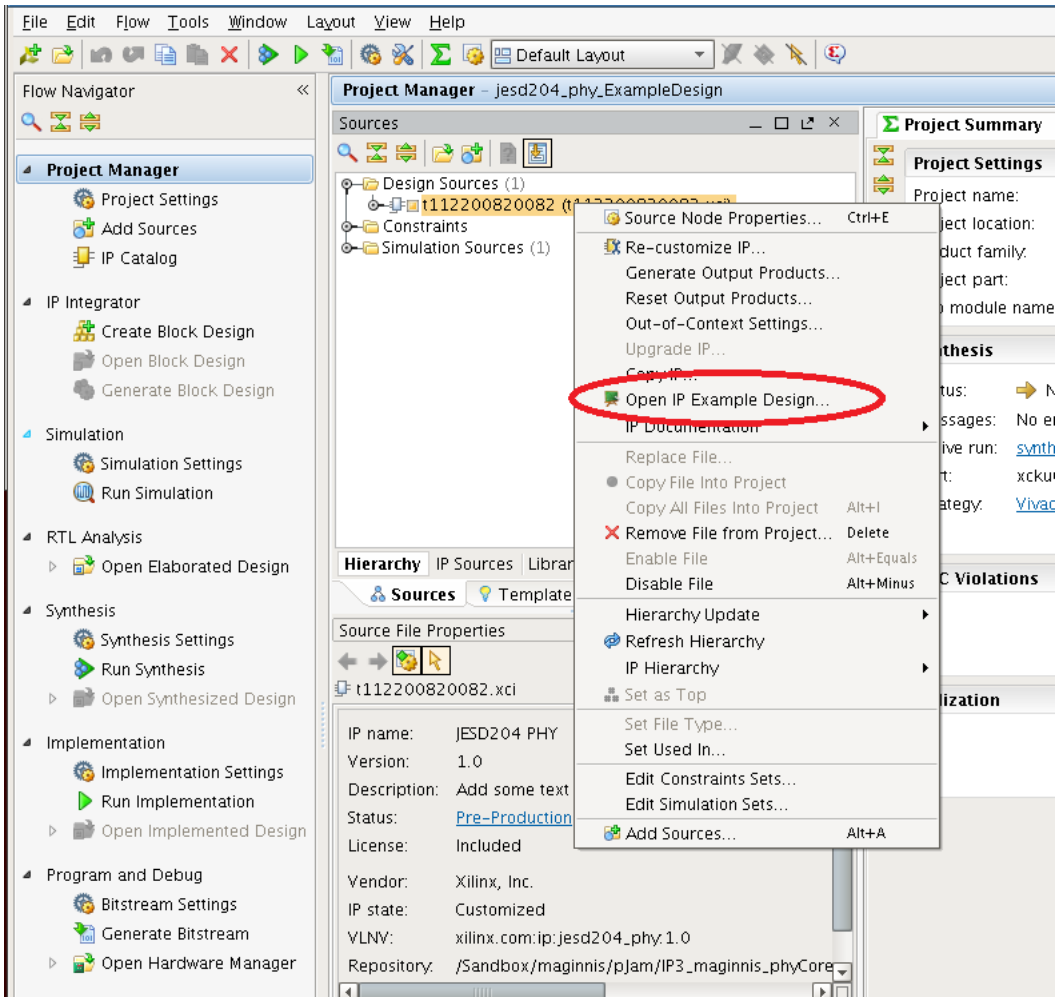

Figure 5-1: **Opening the Example Design**

The example design generates data internally for the TX path. This is checked externally and can also be fed back into the RX path, where a simple check function exists to verify the incoming data is 8'hBC.

The `clks_in` module places the appropriate clock buffers on the clock paths dependent on the technology chosen.

The sequencer is responsible for indicating when the example design can test the incoming data as well as sequencing the data that is transmitted. When both the RX and TX channels are out of reset, it sends out K28.5 symbols. These are followed by four `/R/….../A/` frames mimicking what is seen on a JESD204 data interface. Note `/Q/` and the 14 bytes of `/Q/` data are not sent. They just increment counter values.

Figure 5-2 shows a block diagram for the example design.

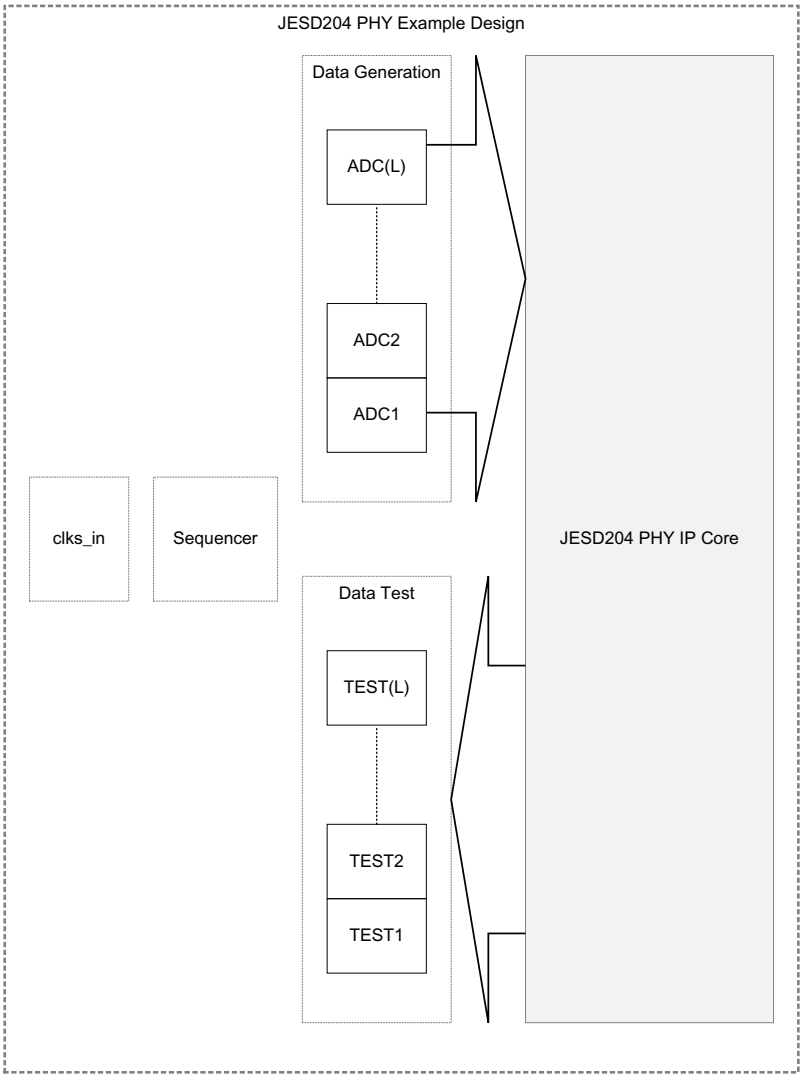

Figure 5-2: **Example Design Block Diagram**

Figure 5-3 and Figure 5-4 show the clock structure for different and identical PLL types, respectively.

TIP: *If different PLLs are selected for the RX and TX paths, the port names for refclk are named as "rx" and "tx." If they are the same, the port is named as "common."*

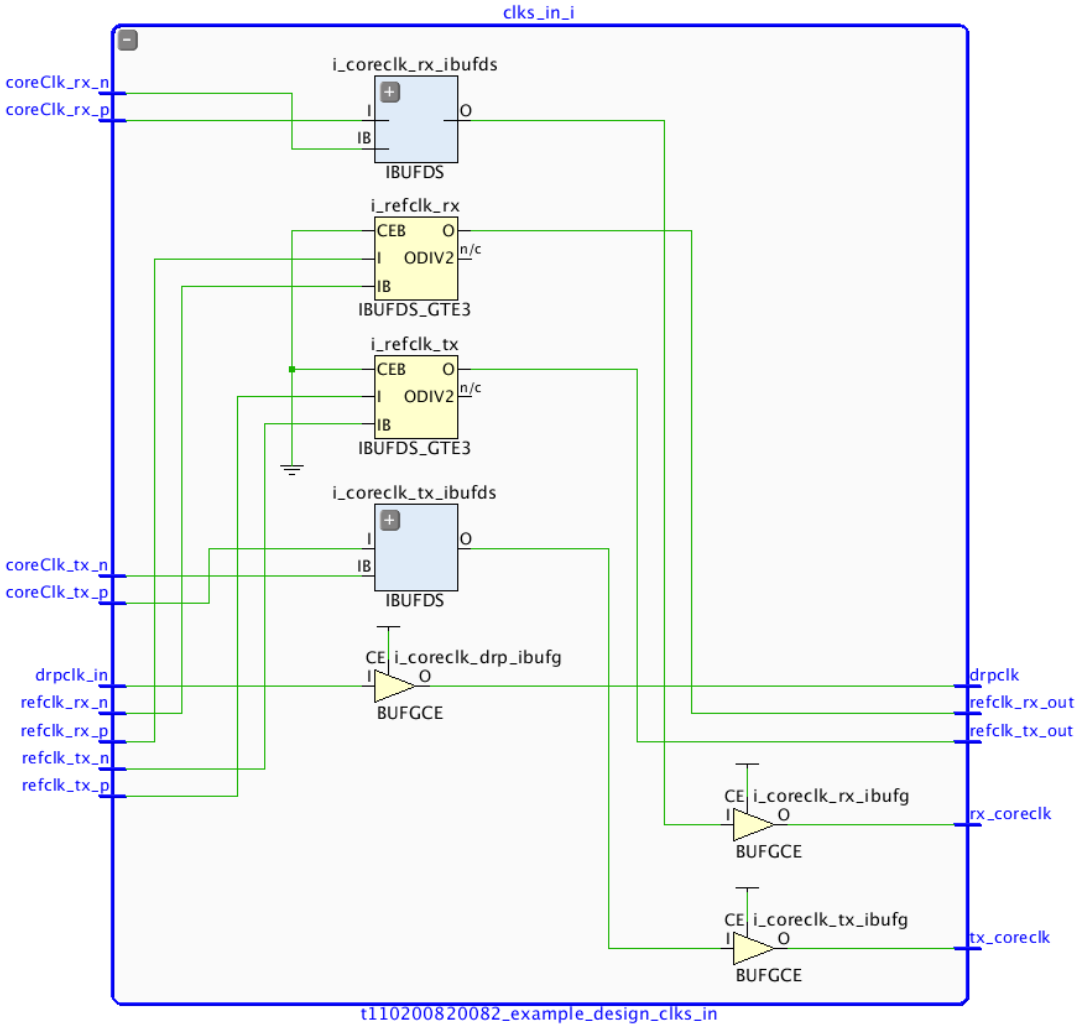

Figure 5-3: **Clock Structure with Different PLL Types**

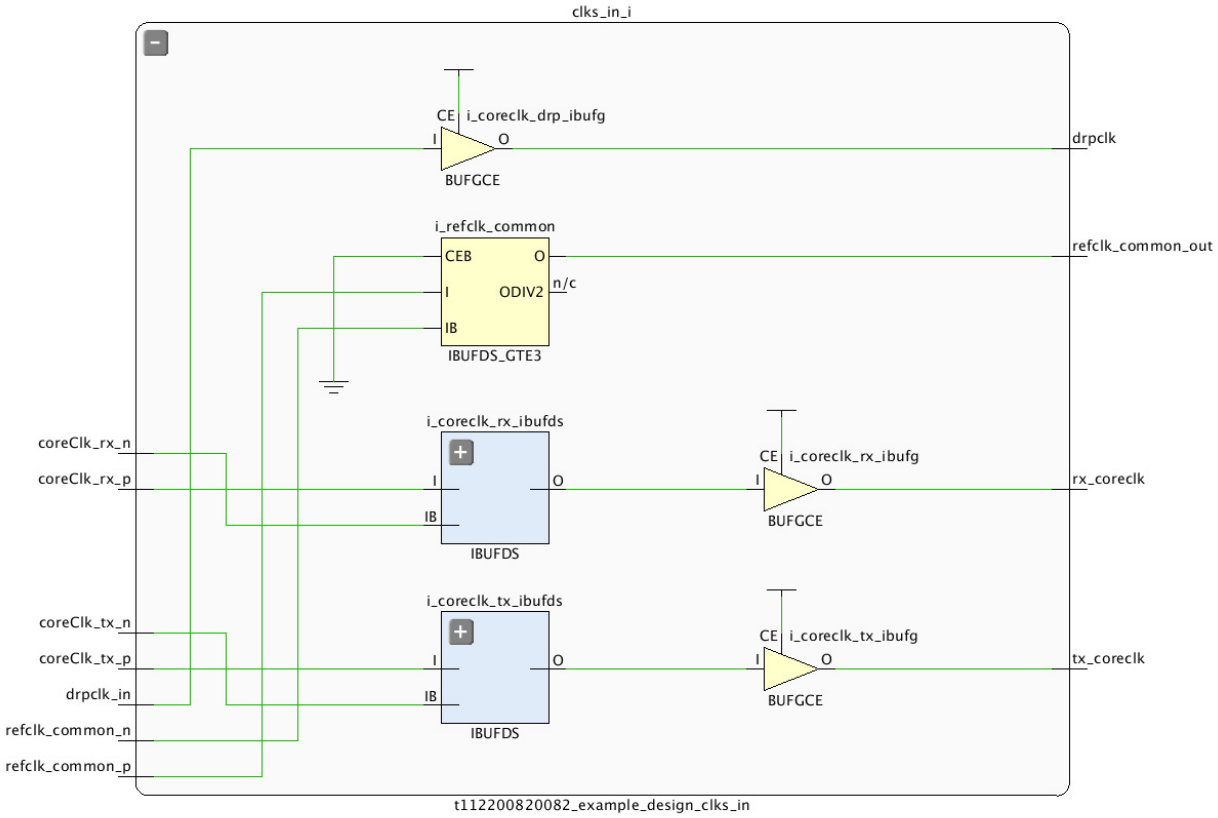

Figure 5-4: **Clock Structure with Matching PLL Types**

Test Bench

This chapter contains information about the test bench provided in the Vivado® Design Suite. Figure 6-1 shows the test bench block diagram.

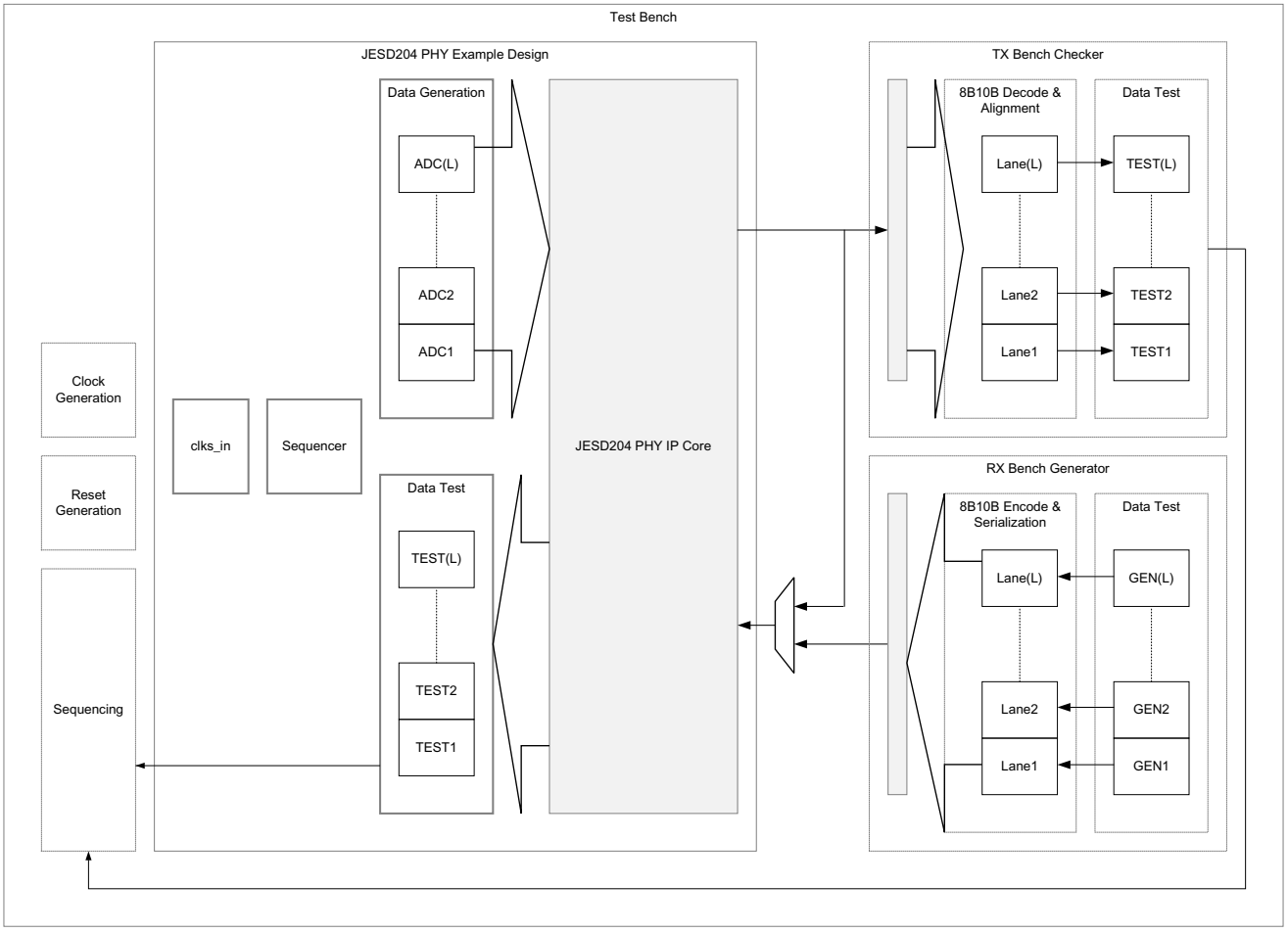

Figure 6-1: **Test Bench Block Diagram**

Hierarchy is used extensively to create per-lane stimulus and checker blocks which allow easier signal viewing in the waveform window.

The test bench provides all clocks required by the design. If the TX and RX line rates are equal, the loopback path is automatically selected for simulation at IP build time.

Several event messaging functions exist at the top-level. These indicate when the lanes are out of reset and the bit rates used by the RX and TX channels. A timeout function is also included.

The data generation and testing functions exist in separate modules instantiated in the top-level test bench. This enables clear navigation to a lane data stream with the waveform viewer. The data stream starts when both the TX and RX paths are out of reset. K28.5 (/K/) symbols are transmitted to allow the transceivers to bit align.

An ILA-type sequence, consisting of just the K28.0 (/R/), K28.3 (/A/) and data, is sent to allow the test bench to align to a 32-bit boundary. The bench continues to run for a specified length of core clock cycles before finishing.

IMPORTANT: *To change any IP parameters, you must reconfigure the IP and regenerate the example design.*

AXI Interface

If the IP is generated with the AXI interface, this is presented in the test bench along with tasks to write/read over the interface. Basic examples are given at the start of the test, however the tasks might be used to test out custom sequences.

For UltraScale devices, see *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 10], *Appendix B* for a detailed DRP register map and for 7 series devices, see *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 11], *Appendix D*.

Verification, Compliance, and Interoperability

The JESD204 core has been verified using both simulation and hardware testing.

Simulation

A highly parameterizable transaction-based simulation test suite has been used to verify the core. Tests include:

- Scrambling and alignment
- Loss and regain of synchronization
- Frame transmission
- Frame reception
- Recovery from error conditions

Hardware Testing

The core has been used in many hardware test platforms within Xilinx and in interoperability testing with external hardware vendors.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the JESD204 PHY, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the JESD204 PHY. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx® Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the JESD204 PHY Core

AR: 61911

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Additional Resources.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Log in to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address JESD204 PHY design issues. It is important to know which tools are useful for debugging various situations.

Vivado Lab Edition

Vivado® Lab Edition inserts logic analyzer and virtual I/O cores directly into your design. Vivado Lab Edition also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx.

The Vivado logic analyzer is used with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 8].

Reference Boards

Various Xilinx development boards support the JESD204 PHY. These boards can be used to prototype designs and establish that the core can communicate with the system.

7 Series FPGA Evaluation Boards

- AC701
- KC705
- ZC706
- VC709

Simulation Debug

The simulation debug flow for QuestaSim is illustrated in Figure B-1. A similar approach can be used with other simulators.

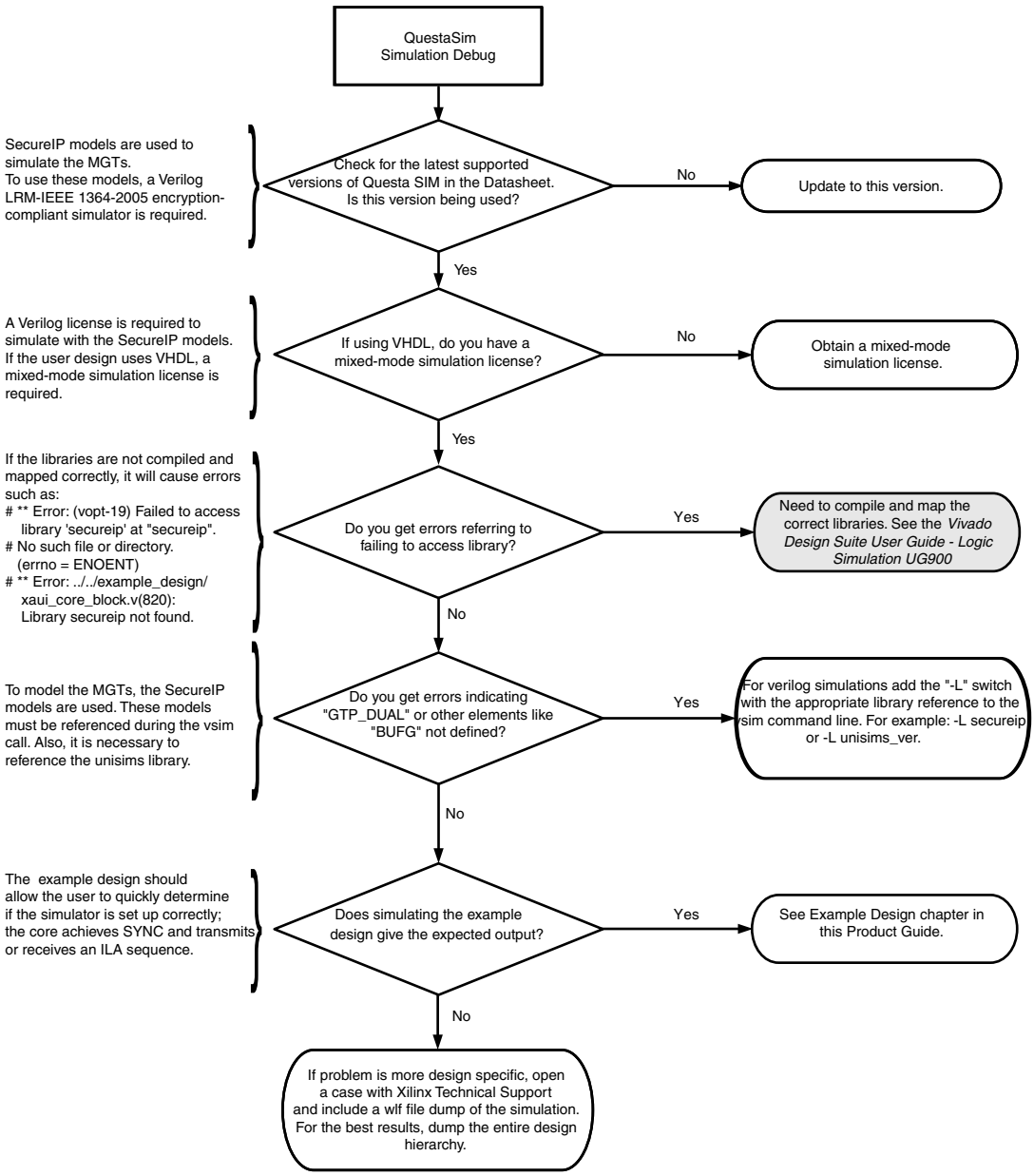

Figure B-1: **QuestaSim Debug Flow Diagram**

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. Vivado Lab Edition is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using Vivado Lab Edition for debugging the specific problems.

General Checks

- Ensure that all the timing constraints for the core were met during implementation.
- Ensure that all clock sources are clean and in particular that the transceiver reference clocks meet the GTX/GTH/GTP transceiver requirements from the appropriate FPGA Data Sheet.
- Ensure that all GTX/GTH/GTP transceiver PLLs have obtained lock by monitoring the QPLLLOCK_OUT and/or CPLLLOCK_OUT port either using Vivado Lab Edition or by routing the signals to a spare pin.
- Ensure that when regenerating a new GTX/GTH/GTP transceiver the reference clock of the new transceiver matches that of the design.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *Serial Interface for Data Converters* (JESD204B)
2. *JESD204 LogiCORE IP Product Guide* (PG066)
3. *Vivado® Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
4. *Vivado Design Suite User Guide: Designing with IP* (UG896)
5. *Vivado Design Suite User Guide: Getting Started* (UG910)
6. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
7. *ISE® to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
9. *Vivado Design Suite User Guide: Implementation* (UG904)
10. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
11. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
12. *7 Series FPGAs GTP Transceivers User Guide* (UG482)
13. *Artix-7 FPGAs Data Sheet* (DS181)
14. *Kintex-7 FPGAs Data Sheet* (DS182)
15. *Virtex-7 T and XT FPGAs Data Sheet* (DS183)
16. *Kintex UltraScale Architecture Data Sheet* (DS892)
17. *Virtex UltraScale Architecture Data Sheet* (DS893)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/01/2015	2.0	• Updated Applications section. • Added GT Port important note in Transceiver Control and Status Ports section. • Updated Table 2-4: Common Clock and Reset Ports. • Added qpll0_reset_out and qpll1_reset_out to Table 2-5: Clocks and Resets for Shared Logic in Example Design. • Added Register Space and Line Rate Switching section. • Added JESD204 PHY Configuration Options section. • Updated Clocking section. • Updated Fig. 4-1: Configuration Tab. • Added Optional Settings in Configuration Tab section. • Updated User Parameters. • Added constraint file in Required Constraints section. • Added UNISIM important note in Simulation section. • Added AXI Interface section in Test Bench chapter.
10/01/2014	1.0	Initial Xilinx release.

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