LogiCORE IP JESD204 v3.1

PB011 December 18, 2012 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP JESD204 core implements a JESD204B interface supporting a line rate of up to 12.5 Gb/s on 1, 2, 3, 4, 5, 6, 7, or 8 lanes using GTX or GTH transceivers in Kintex™-7 and Virtex-7 FPGAs. The JESD204 core can be configured as Transmit or Receive. The core supports sharing a GTX or GTH transceiver between a transmitter and receiver.

Features

- Designed to JEDEC JESD204B
- Supports 1, 2, 3, 4, 5, 6, 7, or 8 lane configurations
- Supports Initial Lane Alignment
- Supports scrambling
- Supports 1-256 octets per frame
- Supports 1-32 frames per multi frame
- Supports Subclass 0, 1 and 2
- Physical and Data Link Layer functions provided
- AXI4-Lite configuration interface
- AXI4-Stream data interface
- Supports GTX or GTH transceiver sharing
- Delivered by Xilinx Vivado™ Design Suite

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex®-7, Kintex™-7
Supported User Interfaces	AXI4-Stream, AXI4-Lite
Provided with Core	
Design Files	Vivado: Encrypted RTL
Example Design	Verilog
Test Bench	Verilog
Constraints File	Vivado: XDC
Simulation Model	Verilog
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado™ Design Suite v2012.4(3)
Simulation	ModelSim
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the release notes for this core.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
3. Supports 7 series devices only.

Applications

JESD204 is a high-speed serial interface designed to connect Analog-to-Digital Converter (ADCs) and Digital-to-Analog Converter (DACs) to logic devices. The JESD204 interface is specified in the *JEDEC JESD204A Specification 2008* and the *JEDEC JESD204B Specification 2011*. Figure 1 and Figure 2 illustrate how the JESD204 provides the interface between an ADC/DAC and user logic over an example 4 lane interface.

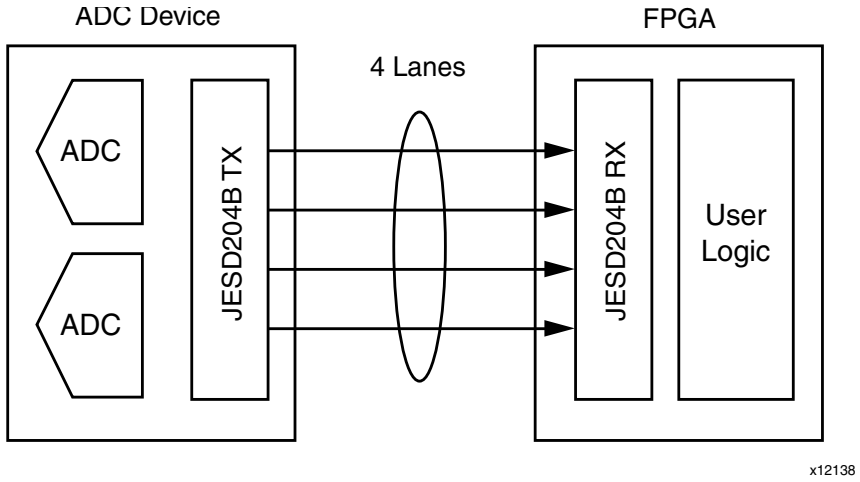

Figure 1: **ADC Application**

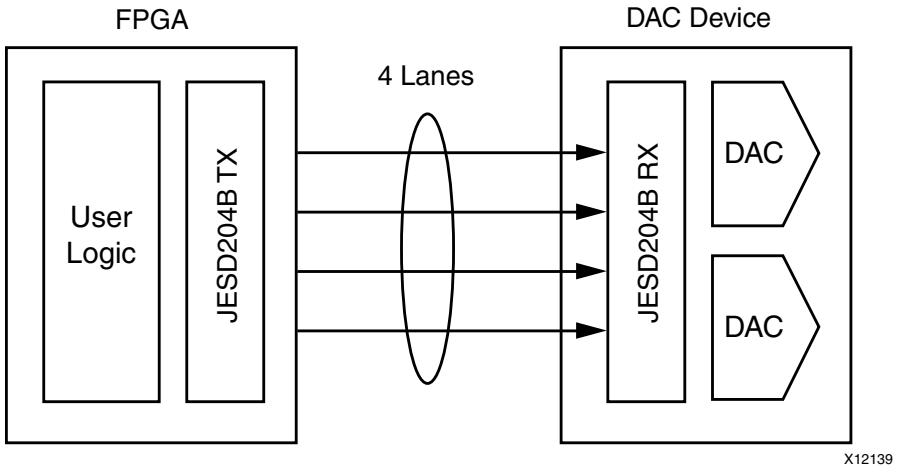

Figure 3: **DAC Application**

Additional Documentation and Supporting Materials

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/jesd204/index.htm.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the IP Release Notes Guide (XTP025) for more information on this core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Resolved Issues
- Known Issues

Licensing and Ordering Information

A free evaluation version of the core is provided with the Xilinx® Vivado Design Suite, which lets you assess the core functionality and demonstrates the various interfaces of the core in simulation. To access the evaluation version visit the JESD204 IP Evaluation page.

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the JESD204 product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/25/12	1.0	Initial Xilinx release.
12/18/12	2.0	Updated for 2012.4 • The core now supports 1, 2, 3, 4, 5, 6, 7 and 8 lane configurations in 7 series devices • Added 12.5 Gb/s line rate support • Removed JESD204A (new designs should use JESD204B subclass 0) • Removed ISE • Added three new test modes • Added software lane select

Notice of Disclaimer