LogiCORE IP JESD204 (v2.1)

DS814 April 24, 2012 **Product Specification**

Introduction

The Xilinx® LogiCORE™ IP JESD204 core implements a JESD204A or JESD204B interface supporting a line rate of up to 6.25 Gb/s on 1, 2 or 4 lanes using GTX transceivers in Virtex®-6 and a line rate of up to 10.3125 Gb/s on 1, 2, 4 or 8 lanes using GTX transceivers in Kintex™-7 and Virtex-7 FPGAs. The JESD204 core can be configured as Transmit or Receive. The core supports sharing a GTX transceiver between a transmitter and receiver.

Features

- Designed to JEDEC JESD204A [Ref 1] and JESD204B [Ref 2]
- Supports 1, 2 and 4 (and 8 in 7 series) lane configurations
- Supports Initial Lane Alignment
- Supports scrambling
- Supports 1-256 octets per frame
- Supports 1-32 frames per multi frame
- Physical and Data Link Layer functions provided
- AXI4-Lite configuration interface [Ref 3]
- AXI4-Stream data interface [Ref 3]
- Supports GTX transceiver sharing
- Delivered by CORE Generator™ tool

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-7, Kintex-7, Virtex-6				
Supported User Interfaces	AXI4-Stream, AXI4-Lite Control/Status				
	Resources				
Configuration	**Slices**	**FFs**	**LUT**	**BUFG**	**Block RAM36**
Rx 1 Lane	430	880	1300	4(2)	1
Rx 2 Lane	920	1500	2070	4(2)	2
Rx 4 Lane	1750	2750	3800	4(2)	4
Rx 8 Lane	3020	6370	7580	4(2)	8
Tx 1 Lane	410	620	950	3	0
Tx 2 Lane	520	810	1230	3	0
Tx 4 Lane	770	1180	1740	3	0
Tx 8 Lane	980	1970	2480	3	0
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	NGC Netlist				
Example Design	Verilog				
Test Bench	Verilog				
Constraints File	UCF				
Simulation Model	Verilog				
Supported S/W Driver	N/A				
Tested Design Tools (3)					
Design Entry Tools	ISE 14.1				
Simulation	ModelSim				
Synthesis Tools	XST 14.1				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. For a complete listing of supported devices, see the release notes for this core.
2. Four BUFGs required on Virtex-6 devices, two on Kintex-7 devices.
3. For the supported versions of the tools, see the ISE Design Suite 14: Release Notes Guide.

Overview

JESD204 is a high-speed serial interface designed to connect Analog-to-Digital Converter (ADCs) and Digital-to-Analog Converter (DACs) to logic devices. The JESD204 interface is specified in the *JEDEC JESD204A Specification 2008* [Ref 1]and the *JEDEC JESD204B Specification 2011* [Ref 2]. Figure 1 and Figure 2 illustrate how the JESD204 provides the interface between an ADC/DAC and user logic over an example 4 lane interface.

Applications

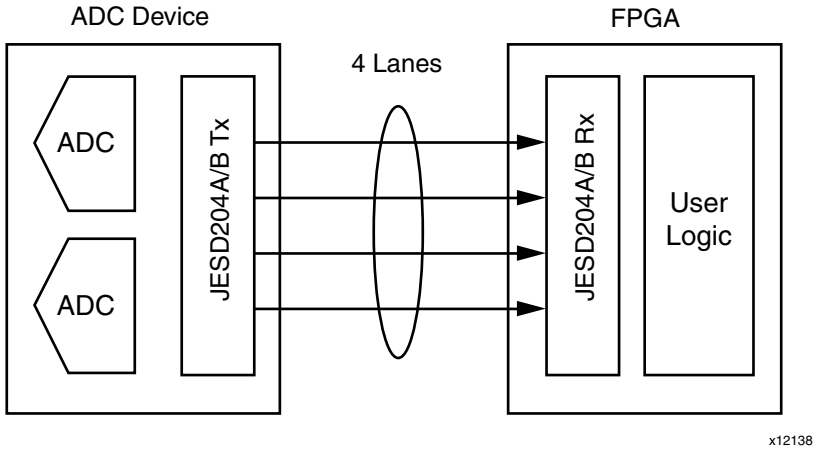

Figure 1: **ADC Application**

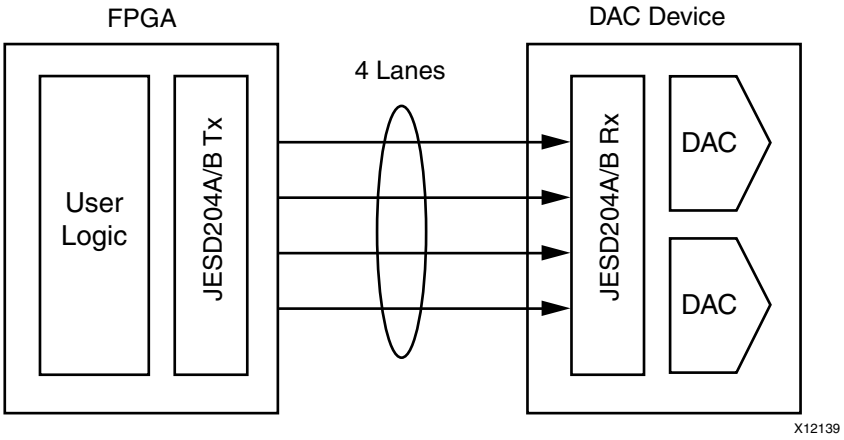

Figure 2: **DAC Application**

Functional Description

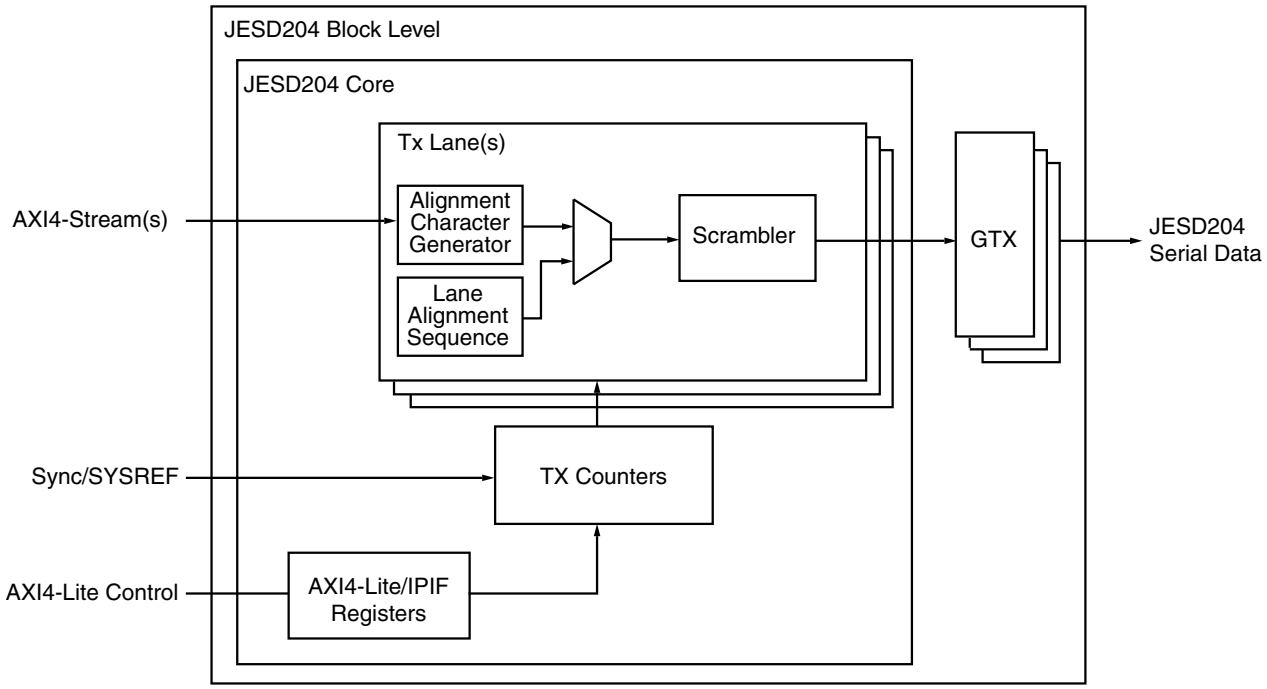

Figure 3: **Transmitter**

Transmitter

Figure 3 shows the block diagram for the transmitter of the JESD204 core. The main blocks are:

- AXI4-Stream interface for each lane
- Initial Lane Alignment (ILA) sequence generation for each lane
- Scrambling for each lane
- Alignment character insertion logic for each lane
- Control state machine and Sync interface
- Transceiver wrapper logic
- Block level wrapper

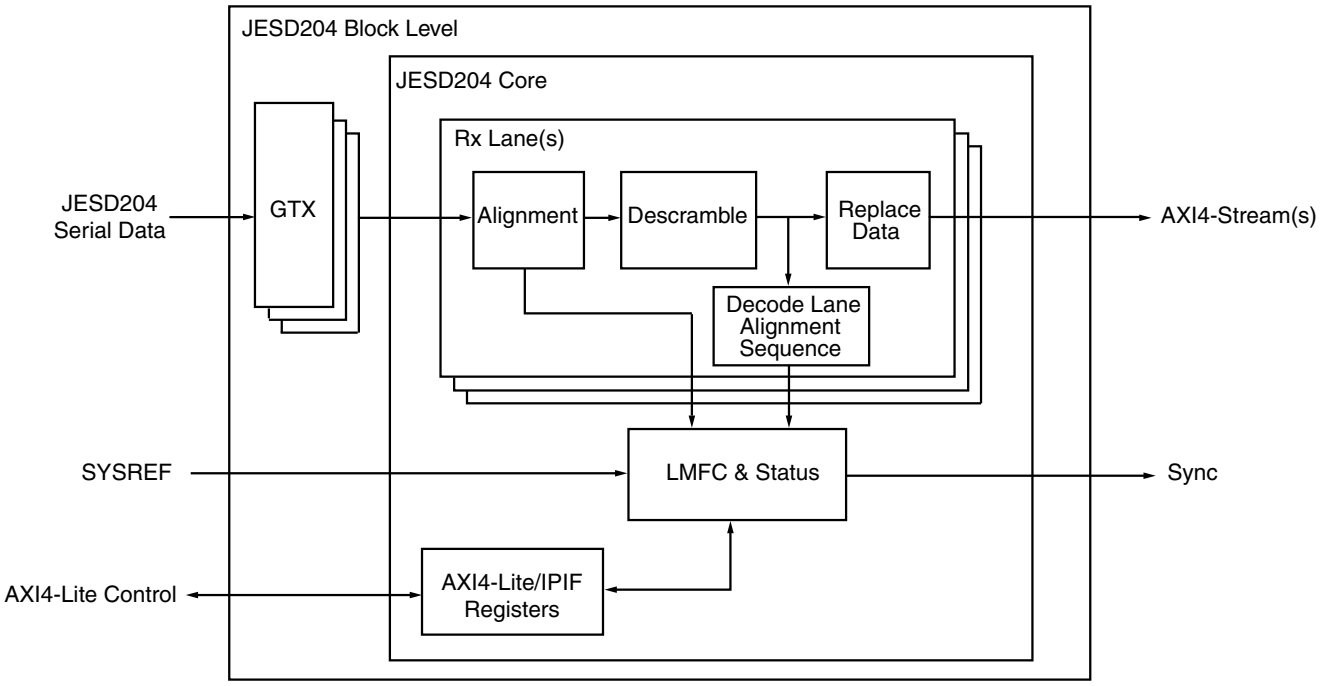

Figure 4: **Receiver**

Receiver

Figure 4 shows the block diagram for the receiver of the JESD204 core. The main blocks are:

- AXI4-Stream interface for each lane
- ILA capture for each lane
- Descrambling for each lane
- Alignment character detection and replacement logic for each lane
- Control state machine and Sync interface
- Transceiver wrapper logic
- Block level wrapper

References

To search for Xilinx documentation, go to www.xilinx.com/support.

To search for JESD204 documentation, go to www.jedec.org

For a glossary of technical terms used in Xilinx documentation, see: www.xilinx.com/company/terms.htm.

1. JEDEC JESD204A April, 2008
2. JEDEC JESD204B July, 2011
3. Xilinx AXI Reference Guide (UG761)

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

A free evaluation version of the core is provided with the Xilinx CORE Generator tool, which lets you assess the core functionality and demonstrates the various interfaces of the core in simulation. After purchase, the core can be downloaded from the Xilinx IP Center for use with CORE Generator v14.1. CORE Generator is bundled with ISE® Design Suite v14.1 at no additional charge.

Contact your Xilinx sales representative for pricing and availability about the JESD204 core or go to the JESD204 product page for additional information.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/19/11	1.0	Initial Xilinx Release
04/24/12	2.0	Version 2.1 of core. ISE Release 14.1. Add 8 lanes, transceiver sharing and increase line rate to 10.3125 Gb/s.

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