Integrated Logic Analyzer (ILA) v2.0

DS875 July 25, 2012 **Product Specification**

ILA Introduction

The customizable Integrated Logic Analyzer (ILA) IP core is a logic analyzer that can be used to monitor the internal signals of a design. The ILA core includes many advanced features of modern logic analyzers, including boolean trigger equations, and edge transition triggers. Because the ILA core is synchronous to the design being monitored, all design clock constraints that are applied to your design are also applied to the components of the ILA core.

Features

- User-selectable trigger width, data width, and data depth
- Multiple probe ports, which can be combined into a single trigger condition

For more information about the ILA core, see the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Artix™-7, Kintex™-7, Virtex®-7				
Supported User Interfaces	IEEE Standard 1149.1 - JTAG				
	Resources				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	888	1,102	0	1	591.7
Config2	937	1,196	0	1	591.7
Config3	32,106	50,610	0	228	570
Provided with Core					
Documentation	Product Specification				
Design Files	N/A				
Example Design	Not Provided				
Test Bench	VHDL Wrapper and Verilog				
Constraints File	Not Provided				
Simulation Model	Not Provided				
Supported S/W Driver	Not Provided				
Tested Design Tools					
Design Entry Tools	Vivado v2012.2				
Simulation	Not Provided				
Synthesis Tools(4)	Not Provided				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. For a complete listing of supported devices, see the release notes for this core.

Applications

The ILA core is designed to be used in any application that requires verification or debugging using the Vivado logic analyzer.

Functional Description

Signals in the FPGA design are connected to ILA core clock and probe inputs (Figure 1). These signals, attached to the probe inputs, are sampled at design speeds and stored using on-chip block RAM (BRAM). The core parameters specify the number of probes, trace sample depth, and the width for each probe input. Communication with the ILA core is conducted using an auto-instantiated debug core hub that connects to the JTAG interface of the FPGA.

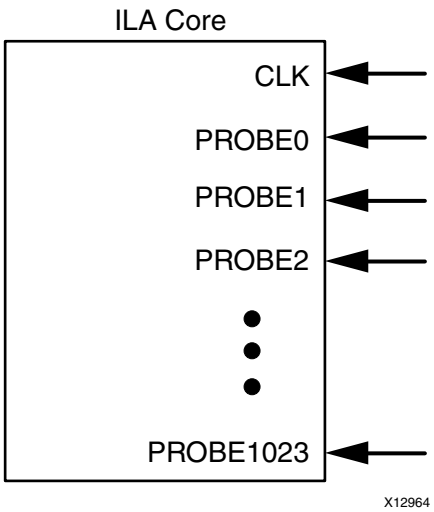

Figure 1: **ILA Core Symbol**

Note: The numerical range from Probe 2 to Probe 1023 is indicated by ellipses (...) in Figure 1.

After the design is loaded into the FPGA device on the board, use the Vivado logic analyzer software to set up a trigger event for the ILA measurement. After the trigger occurs, the sample buffer is filled and uploaded into the Vivado logic analyzer. You can display this data using the waveform window.

Regular FPGA logic is used to implement the probe sample and trigger functionality. On-chip block RAM memory stores the data until it is uploaded by the software. No user input or output is required to trigger events, capture data, or to communicate with the ILA core.

ILA Probe Trigger Comparator

Each probe input is connected to a trigger comparator that is capable of performing various operations. At run time the comparator can be set to perform = or != comparisons. This includes matching level patterns, such as X0XX101. It also includes detecting edge transitions such as rising edge (R), falling edge (F), either edge (B), or no transition (N). The trigger comparator can perform more complex comparisons, including >, <, >=, and <=.

Note that the comparator is set at runtime through the Vivado logic analyzer.

ILA Trigger Condition

The trigger condition is the result of a Boolean "AND" or "OR" calculation of each of the ILA probe trigger comparator result. Using the Vivado logic analyzer, you select whether to "AND" probe trigger comparators probes

or "OR" them. The "AND" setting causes a trigger event when all of the ILA probe comparisons are satisfied. The "OR" setting causes a trigger event when any of the ILA probe comparisons are satisfied. The trigger condition is the trigger event used for the ILA trace measurement.

ILA Ports and Parameters

Table 1 and Table 2 provide the details about the ILA ports and parameters..

Table 1: **ILA Ports**

Port Name	Direction	Description
CLK	IN	Design clock that clocks all trigger and storage logic.
PROBE<n>[<*m*>-1:0]	IN	Probe port input. The probe port number <n> will be in the range from 0 to 1023. The probe port width (denoted by <m>) is in the range of 1 to 4096. ***Note:*** You must declare this port as a vector. For a one-bit port, use PROBE<n>[0:0].

ILA Parameters

Table 2: **ILA Parameters**

Parameter Name	Allowable Values	Default Value	Description
component_name	String with A-z, 0-9, and _ (underscore)	ila_v2_0_0	Name of instantiated component
C_NUM_OF_PROBES	1–1024	1	Number of ILA probe ports
C_DATA_DEPTH	1024, 2048, 4096, 8192, 16384, 32768, 65536, 131072	1024	Probe storage buffer depth. This number represents the maximum number of samples that can be stored at run time for each probe input.
C_PROBE<n>_WIDTH	1–4096	1	Width of probe port <n>. Where <n> is the probe port having a value from 0 to 1023.

Verification

Xilinx has verified the ILA v2.0 core in a proprietary test environment, using an internally developed bus functional model.

References

More information about the Vivado logic analyzer software is available in the *Xilinx Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite software under the terms of the Xilinx End User License. The core may be accessed through the Vivado Design Suite IP catalog.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Doc Version	Description of Revisions
07/25/2012	1.0	Initial Xilinx release of the ILA core with Vivado Design Suite support. Previous version of this data sheet was DS299.

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