25G IEEE 802.3by Reed-Solomon FEC v1.0

PB035 (v1.0) April 6, 2016 **Product Brief**

Introduction

The Xilinx® LogiCORE™ 25G IEEE 802.3by Reed-Solomon Forward Error Correction IP core implements the Reed-Solomon Forward Error Correction (RS-FEC) sublayer as described in *IEEE 802.3by/D2.2 section 108* [Ref 1] and the 25G Ethernet Consortium Schedule 3 (v1.6) section 3.2.3 [Ref 2].

Additional Documentation

A product guide is available for this core. Access to this material can be requested by clicking on this registration link:
www.xilinx.com/member/25g_rs_fec.html

Features

- IEEE Std. 802.3by TX and RX co-optimized with Xilinx 25G Ethernet MAC and PCS or standalone PCS
- Run-time switchable between IEEE802.3by and 25G Ethernet Consortium Schedule 3 specification mode
- Low latency design
- Configuration and status bus
- Selectable AXI4-Lite interface for status output
- Example reference design demonstrating 25G Ethernet IP with RS-FEC
- ECC RAM option
- Transcode Bypass mode for direct access to RS encoder/decoder
- Optional feature in the 10G/25G Ethernet Subsystem (see the *10G/25G High Speed Ethernet Subsystem Product Guide* (PG210) [Ref 3])

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™ Families Virtex® UltraScale™ Architecture
Supported User Interfaces	AXI4-Lite, Configuration and Status bus
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog
Test Bench	Not Provided
Constraints File	Xilinx Constraints File
Simulation Model	Encrypted Verilog
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado® Design Suite
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The RS-FEC layers of the *IEEE Std 802.3by* [Ref 1] and 25G Ethernet Consortium Schedule 3 [Ref 2] define more than just the RS encoder/decoder. They define several stages of synchronization, alignment and transcoding which are necessary for the layer to communicate with preceding and subsequent layers. The functional block diagram of the core is shown in Figure 1.

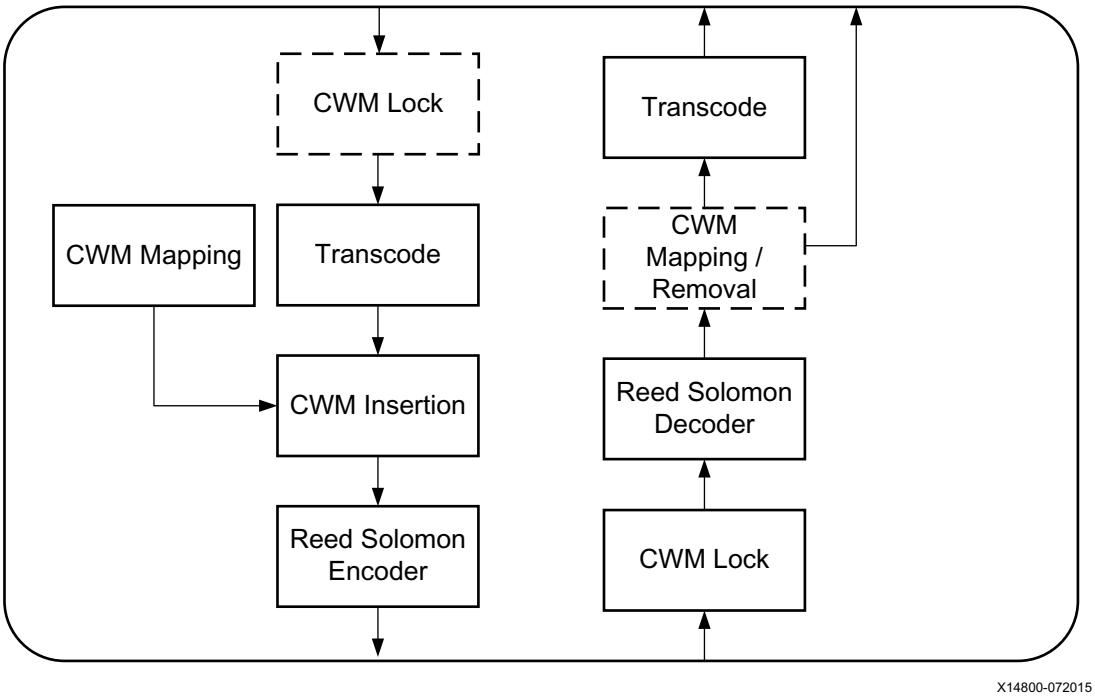

Figure 1: **Core Block Diagram**

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

Xilinx provides premier technical support for customers encountering issues that require additional assistance.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the 10G/25G Ethernet Subsystem product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Evaluation

A full system hardware evaluation license is available for this core. The evaluation version of the core operates in the same way as the full version for several hours, dependent on clock frequency (approximately 10 hours at 391 MHz). Operation is then disabled and the data output does not change. If you notice this behavior in hardware, it probably means you are using an evaluation version of the core. The Xilinx tools warn that an evaluation license is being used during netlist implementation. If a full license is installed for the core to run on hardware, delete the old files and recreate the core from new.

References

These documents provide supplemental material useful with this product brief:

1. *IEEE Std 802.3by/D2.2*, (http://standards.ieee.org/develop/project/802.3.html)
2. *25G Ethernet Consortium Schedule 3 (v1.6) specification*, (http://25gethernet.org/)
3. *10G/25G High Speed Ethernet Subsystem Product Guide* (PG210)

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/06/2016	1.0	Initial Xilnx release.

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