LogiCORE IP Ethernet Statistics v3.5

DS323 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP Ethernet Statistics core provides a user-configurable collection of statistical counters that can be used to gather network traffic statistics for the Xilinx® Ethernet Media Access Controller (MAC) products.

Features

- Example designs are provided for use with these Xilinx Ethernet MAC cores:
  - Embedded Tri-Mode Ethernet MAC
  - Tri-Mode Ethernet MAC solution comprised of the 10/100/1000 Mb/s, 1000 Mb/s, and 10/100 Mb/s IP cores
- Provides between 20 and 64 individual statistics counters
- Provides 32-bit or 64-bit counter widths
- Addressable counters that can be read through an independent microprocessor-neutral interface (which can be shared with the chosen Ethernet MAC)
- Editable HDL example design included to define the statistics counted
- Fully configurable using the Xilinx CORE Generator™ software v13.1.

LogiCORE IP Facts				
Core Specifics				
Supported Device Families[1]	Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3, Spartan-3A, Spartan-3A DSP Spartan-3E			
Supported User Interfaces	Host Interface			
Width	32-bit or 64-bit counters			
Performance	Statistical gathering at 10 Mb/s, 100 Mb/s, 1 Gb/s			
Resources				
	Slices	**LUTs**	**FFs**	**Block RAM**
LUT4 (Spartan-3, Virtex-4)[2]	450-850	300-700	500-800	1-2
LUT6 (Virtex-5 and newer)[2]	300-550	450-850	450-750	0
BUFG (All families)	2-4 (shared with Ethernet MAC)			
Provided with Core				
Documentation	Product Specification User Guide			
Design Files	NGC netlist			
Example Design	Verilog or VHDL			
Test Bench	Demonstration Test Bench Scripts			
Constraints File	User Constraints File (UCF)			
Simulation Model	Verilog or VHDL			
Tested Design Tools				
Design Entry Tools	ISE v13.1 software			
Simulation	Mentor Graphics ModelSim v6.6d Cadence Incisive Enterprise Simulator (IES) v10.2 Synopsys VCS and VCS MX 2010.06			
Synthesis Tools	XST v13.1			
Provided by Xilinx, Inc.				

1. For the complete list of supported devices, see the release notes for this core. Speed grades for devices are: -1 for Virtex-6 and Virtex-5, -10 for Virtex-4, -2 for Spartan-6, and -4 for all other supported Spartan devices. Ethernet Statistics has been merged into the Tri-Mode Ethernet MAC for v5.1 and later and the Virtex-6 FPGA Tri-Mode Ethernet MAC for v2.1 and later. When using these versions of the Tri-Mode Ethernet MAC, you do not instantiate the Ethernet Statistics separately.
2. The Ethernet Statistics core is highly configurable; resource ranges given are given as a guide.

Typical Applications

Figure 1 illustrates a typical application for the Ethernet Statistics core and its example design. In this example, the core is connected to an Ethernet MAC core. The Management Interface is shown connected to a Station Management Entity (STA), which monitors network performance. This STA can be implemented in any of the Xilinx embedded processors (MicroBlaze™ or PowerPC®), or an external processor. Each counter can be uniquely addressed and read through the Management Interface at any point.

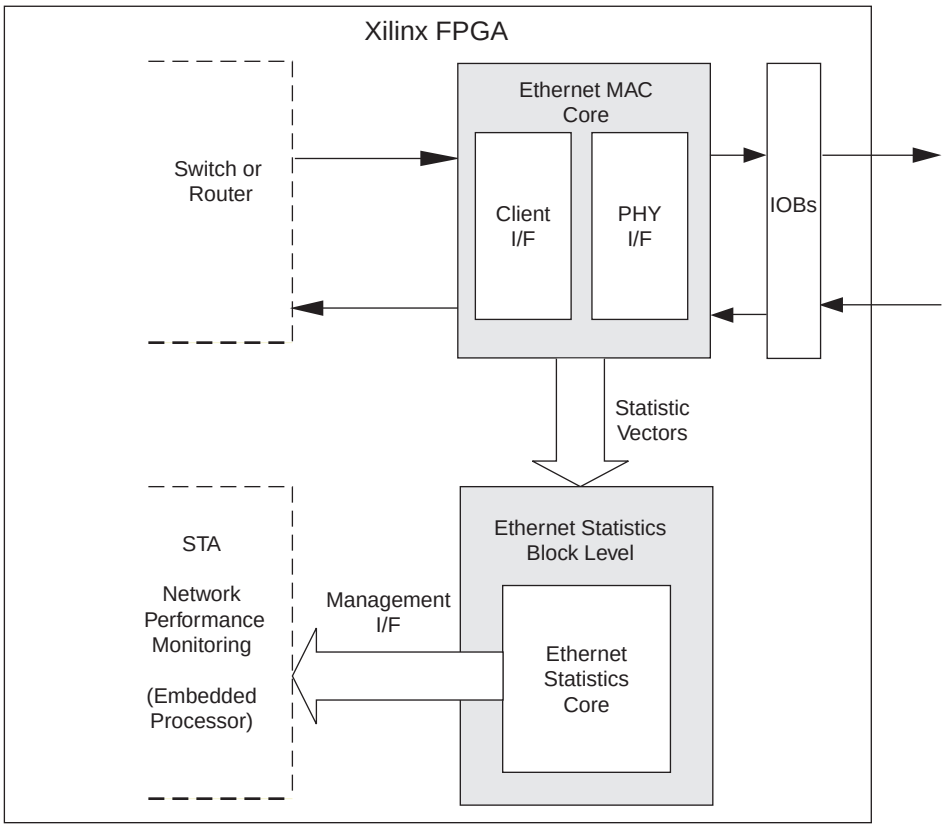

Figure 1: **Typical Application**

Overview

This document defines the Ethernet Statistics core functions as instantiated within its example design and lists the statistics counters provided by the example design. The example design delivered with the core supports the following Xilinx Ethernet Media Access Controller (MAC) cores:

- Embedded Tri-Mode Ethernet MAC
- Tri-Mode Ethernet MAC solution comprised of the 10/100/1000 Mb/s, 1000 Mb/s and 10/100 Mb/s IP cores. All of the IP cores are referred to as Tri-Mode Ethernet MAC in the rest of this document.

Functional Description

Ethernet Statistics Example Design

Figure 2 illustrates the Ethernet Statistics core instantiated within its example design, shown connected to an Ethernet MAC. Each functional block and interface displayed in Figure 2 is described in this section.

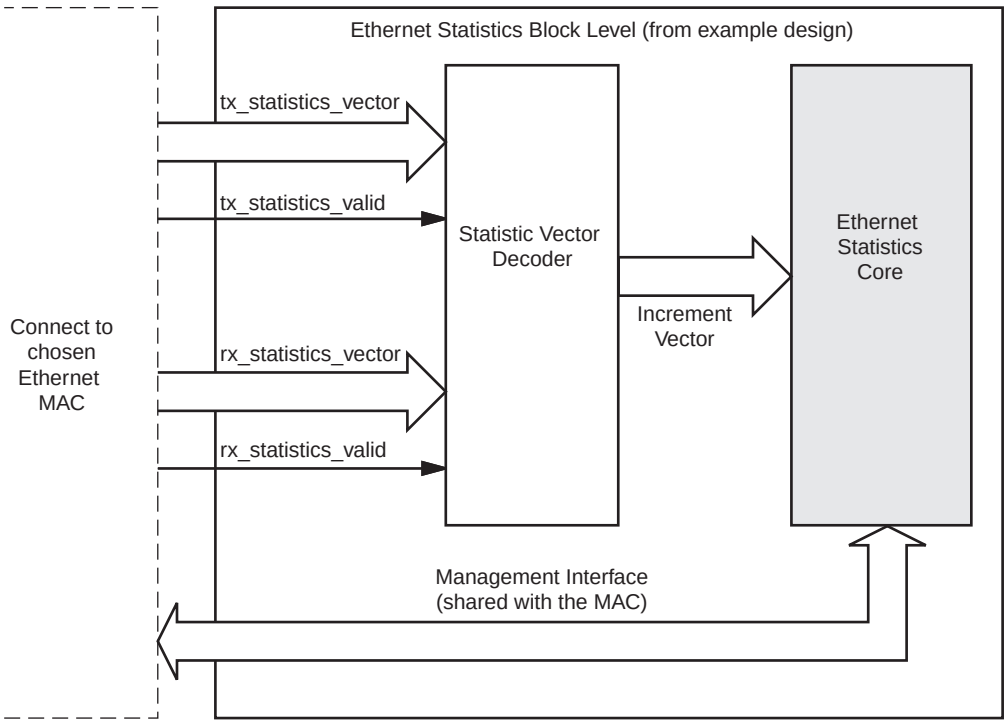

Figure 2: **Ethernet Statistics Example Design Top-level Block Diagram**

- **Statistics Vectors**. The chosen MAC outputs its statistics in the form of statistic vectors, both for transmitter and receiver functions. For a definition of these statistic vector outputs, see the associated MAC user guide.
- **Statistic Vector Decoder**. The MAC statistic vectors are routed into the Statistic Vector Decoder module. As part of the example design, this is provided in HDL. This module decodes the vectors and implements the logic to derive each of the statistics counters and can be easily modified to create statistics counters for specific applications.
- **Management Interface**. The Management Interface is always free to read the current statistics counter values from the core. Each specific counter can be individually addressed. This Management Interface can either be shared with that of the chosen MAC or used separately.

Ethernet Statistics Core

The Ethernet Statistics core is pre-synthesized and delivered as a Xilinx NGC netlist, as illustrated in the shaded area of Figure 2 (the Ethernet Statistics core block). Figure 3 illustrates an expanded version of the core netlist.

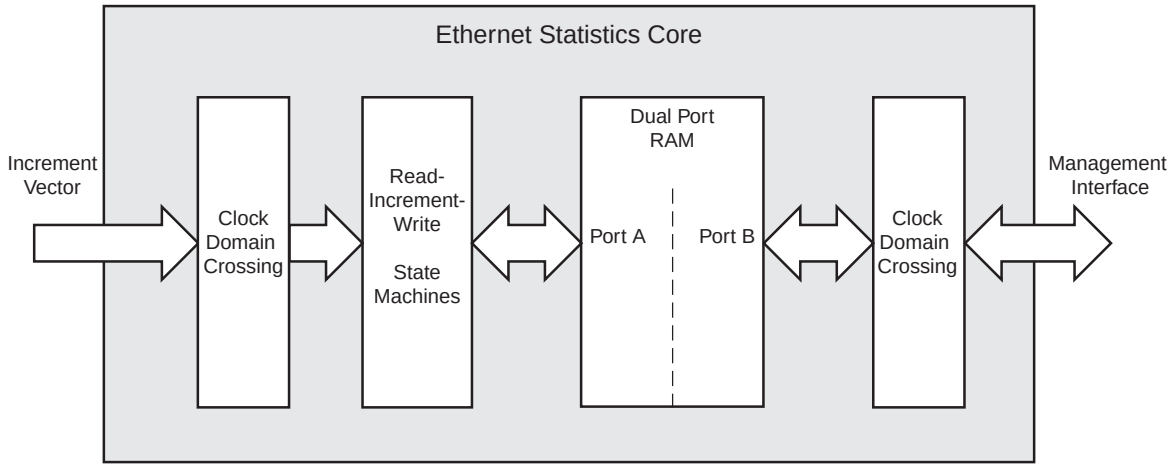

Figure 3: **Ethernet Statistics Core Netlist**

Input increment signals arrive from the Vector Decoder block (Figure 2) through an `increment_vector` bus. There is an increment bit for each counter; a toggle on a particular increment bit causes the corresponding counter to increment. For example, a toggle of the `increment_vector[17]` signal causes counter number 17 to increment. Counter 17 also corresponds to address 17 in decimal (0x11 in hexadecimal) when read from the Management Interface.

Within the core, the current counter values are stored in Dual Port RAM. In response to toggles on the `increment_vector` signals, individual counter values are read out of the RAM, incremented, and written back. This operation occurs on port A of the dual-port memory.

Port B of the dual-port memory is reserved for the Management Interface, which is free to read the current statistic values at any point in time. Each specific counter can be individually addressed. This Management Interface can either be shared with that of the chosen MAC or used separately.

For detailed information about integrating the core, see the Ethernet Statistics User Guide (UG170)

Statistics Counters

Table 1 defines the statistics counters provided by the example design. All 41 statistics counters are provided for the Embedded Ethernet MAC, and Tri-Mode Ethernet MAC. When using the Tri-Mode Ethernet MAC in its full-duplex only configuration, only the first 34 statistics counters (the non-half-duplex counters) are relevant.

You can modify the statistics counters by editing the Vector Decoder block HDL source code provided with the example design. You can control the address of each counter by connecting the logic that defines a specific counter up to a different `increment_vector` bit.

The statistics counters will wrap around when they reach their maximum value.

Table 1: **Example Design Statistics Counter Definitions**

Address	Name	Description
0	Transmitted bytes	A count of bytes of frames transmitted (destination address to frame check sequence inclusive).
1	Received bytes	A count of bytes of frames received (destination address to frame check sequence inclusive).
2	Undersize frames received	A count of the number of frames received that were fewer than 64 bytes in length but otherwise well formed.
3	Fragment frames received	A count of the number of frames received that were fewer than 64 bytes in length and had a bad frame check sequence field.
4	64 byte Frames Received OK	A count of error-free frames received 64 bytes in length.
5	65-127 byte Frames Received OK	A count of error-free frames received between 65 and 127 bytes in length.
6	128-255 byte Frames Received OK	A count of error-free frames received between 128 and 255 bytes in length.
7	256-511 byte Frames Received OK	A count of error-free frames received between 256 and 511 bytes in length.
8	512-1023 byte Frames Received OK	A count of error-free frames received between 512 and 1023 bytes in length.
9	1024-MaxFrameSize byte Frames Received OK	A count of error-free frames received between 1024 bytes and the specified *IEEE 802.3-2002* maximum legal length.
10	Oversize Frames Received OK	A count of otherwise error-free frames received that exceeded the maximum legal frame length specified in *IEEE 802.3-2002*.
11	64 byte Frames Transmitted OK	A count of error-free frames transmitted that were 64 bytes in length.
12	65-127 byte Frames Transmitted OK	A count of error-free frames transmitted between 65 and 127 bytes in length.
13	128-255 byte Frames Transmitted OK	A count of error-free frames transmitted between 128 and 255 bytes in length.
14	256-511 byte Frames Transmitted OK	A count of error-free frames transmitted between 256 and 511 bytes in length.
15	512-1023 byte Frames Transmitted OK	A count of error-free frames transmitted that were between 512 and 1023 bytes in length.
16	1024-MaxFrameSize byte Frames Transmitted OK	A count of error-free frames transmitted between 1024 and the specified *IEEE 802.3-2002* maximum legal length.
17	Oversize Frames Transmitted OK	A count of otherwise error-free frames transmitted that exceeded the maximum legal frame length specified in *IEEE 802.3-2002*.
18	Frames Received OK	A count of error-free frames received.
19	Frame Check Sequence Errors	A count of received frames that failed the CRC check and were at least 64 bytes in length.
20	Broadcast Frames Received OK	A count of frames successfully received and directed to the broadcast group address.

Table 1: **Example Design Statistics Counter Definitions *(Cont'd)***

Address	Name	Description
21	Multicast Frames Received OK	A count of frames successfully received and directed to a non-broadcast group address.
22	Control Frames Received OK	A count of error-free frames received that contained the special control frame identifier in the length/type field.
23	Length/Type Out of Range	A count of frames received that were at least 64 bytes in length where the length/type field contained a length value that did not match the number of MAC client data bytes received. The counter also increments for frames in which the length/type field indicated that the frame contained padding but where the number of MAC client data bytes received was greater than 64 bytes (minimum frame size). The exception is when the Length/Type Error Checks are disabled in the chosen MAC, in which case this counter will not increment.
24	VLAN Tagged Frames Received OK	A count of error-free VLAN frames received. This counter will only increment when the receiver is configured for VLAN operation.
25	Pause Frames Received OK	A count of error-free frames received that contained the MAC Control type identifier 88-08 in the length/type field, contained a destination address that matched either the MAC Control multicast address or the configured source address of the MAC, contained the PAUSE opcode and were acted upon by the MAC.
26	Control Frames Received with Unsupported Opcode	A count of error-free frames received that contained the MAC Control type identifier 88-08 in the Length/Type field but were received with an opcode other than the PAUSE opcode.
27	Frames Transmitted OK	A count of error-free frames transmitted.
28	Broadcast Frames Transmitted OK	A count of error-free frames that were transmitted to the broadcast address.
29	Multicast Frames Transmitted OK	A count of error-free frames that were transmitted to a group destination address other than broadcast.
30	Underrun Errors	A count of frames that would otherwise be transmitted by the core but could not be completed due to the assertion of TX_UNDERRUN during the frame transmission.
31	Control Frames Transmitted OK	A count of error-free frames transmitted that contained the MAC Control Frame type identifier 88-08 in the length/type field.
32	VLAN Tagged Frames Transmitted OK	A count of error-free VLAN frames transmitted. This counter will only increment when the transmitter is configured for VLAN operation.
33	Pause Frames Transmitted OK	A count of error-free PAUSE frames generated and transmitted by the MAC in response to an assertion of pause_req.
34	Single Collision Frames	A count of frames involved in a single collision but subsequently transmitted successfully (half-duplex mode only).
35	Multiple Collision Frames.	A count of frames involved in more than one collision but subsequently transmitted successfully (half-duplex mode only).

Table 1: **Example Design Statistics Counter Definitions *(Cont'd)***

Address	Name	Description
36	Frames with Deferred Transmissions	A count of frames whose transmission was delayed on its first attempt because the medium was busy (half-duplex mode only).
37	Late Collisions	A count of the times that a collision has been detected later than one slot Time from the start of the packet transmission. A late collision is counted twice— both as a collision and as a late Collision (half-duplex mode only).
38	Frames Aborted due to Excess collisions	A count of the frames that, due to excessive collisions, are not transmitted successfully (half-duplex mode only).
39	Frames with Excess Deferral	A count of frames that deferred transmission for an excessive period of time (half-duplex mode only).
40	Alignment Errors	Asserted for received frames of size 64-bytes and greater which contained an odd number of received nibbles and which also contained an invalid FCS field.

Verification

The Ethernet Statistics core has been verified with extensive simulation and tested in hardware in these ways:

- **Simulation**. The Ethernet Statistics core has been integrated into the test bench of the Tri-Mode Ethernet MAC. This uses highly parameterizable transaction-based test benches (not part of the core deliverables).
- **Hardware Verification**. The core and the example design have been tested in hardware in these configurations:
  - Connected to the Tri-Mode Ethernet MAC core using a Spartan®- 3ADSP FPGA (tested at 1 Gb/s)
  - Connected to the Tri-Mode Ethernet MAC core using a Virtex®-4 LX FPGA (tested at 10 Mb/s, 100 Mb/s, and 1 Gb/s)
  - Connected to the Virtex-4 Embedded Ethernet MAC in a Virtex-4 FX FPGA (tested at 10 Mb/s, 100 Mb/s, and 1 Gb/s)
  - Connected to the Virtex-5 Embedded Ethernet MAC in a Virtex-5 LXT FPGA (tested at 10 Mb/s, 100 Mb/s, and 1 Gb/s)

References

- *IEEE 802.3*
- Tri-Mode Ethernet MAC User Guide (UG138)
- Ethernet Statistics User Guide (UG170)

Support

Xilinx provides technical support for this product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Ethernet Statistics core is provided under the End User License Agreement and can be generated using the Xilinx CORE Generator system v13.1 or higher. The CORE Generator system is shipped with Xilinx ISE® Design Suite Series Development software.

In ISE v13.1 and later, a license key is not required to access the IP. To access the wrapper in ISE v12.4 software and older, a no cost full license must be obtained from Xilinx. See the Ethernet Statistics product page.

Contact your local Xilinx sales representative for pricing and availability of other Xilinx LogiCORE IP modules and software. Information on additional LogiCORE IP modules is available at the Xilinx IP Center.

List of Acronyms

Acronym	Spelled Out
CRC	Cyclic Redundancy Check
DSP	Digital Signal Processor
FCS	Frame Check Sequence
FF	flip-flop
FPGA	Field Programmable Gate Array.
Gb/s	Gigabits per second
HDL	Hardware Description Language
IES	Incisive Enterprise Simulator
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
Mb/s	Megabits per second
NGC	Native Generic Circuit
STA	Station Management Entity
UCF	User Constraints File
VLAN	Virtual LAN (Local Area Network)

Revision History

Date	Version	Revision
4/28/05	1.1	Initial Xilinx release.
1/18/06	1.2	Updated to Xilinx Tools 8.1i, speed grade change to -4 for Spartan-3 and Spartan-3E FPGAs.
7/13/06	1.3	Updated to Xilinx tools 8.2i; core version 2.1.
10/23/06	1.51	Updated to core v2.2, added support for Virtex-5 and Spartan-3A FPGA families.
2/15/07	2.0	Updated core to v2.3, Xilinx tools 9.1i.
8/8/07	2.1	Updated core to v2.4, Xilinx tools 9.2i.
3/24/08	2.2	Updated core to v2.5, Xilinx tools 10.1.
4/24/09	2.3	Updated core to v3.1, Xilinx tools 11.1. Added support for Virtex-6 and Spartan-6 families.
6/24/09	2.4	Updated core to v3.2, Xilinx tools 11.2.
4/19/10	2.5	Updated core to v3.4, Xilinx tools 12.1.
3/1/11	2.6	Updated core to v3.5, Xilinx tools 13.1.

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