Virtex-5 LogiCORE Endpoint Block for PCI Express

DS533 March 24, 2008 **Product Specification**

Introduction

The LogiCORE™ Virtex™-5 Endpoint block for PCI Express® (PCIe®) automates the generation of HDL wrapper files for the Virtex-5 integrated Endpoint block using the Xilinx CORE Generator™ tool. The integrated Endpoint block is highly configurable and this GUI-based tool provides an easy way to produce valid configuration options. This LogiCORE IP wrapper enables advanced features such as multiple virtual channels and larger maximum payload sizes up to 4096 bytes. This lightweight wrapper is suitable for experienced power users.

Verilog and VHDL design wrappers, simulation scripts, and hardware implementation scripts are provided by the tool. In addition to the wrapper files, an example reference design implementation of a memory endpoint is provided. This is a complete example reference design that can be downloaded to the Xilinx ML505 or ML555 reference boards.

Features

- Sets the attributes of the Endpoint block
- Ties off unused ports of the Endpoint block
- Customizes, instantiates, and connects the desired number of RocketIO™ GTP/GTX tiles to the Endpoint block (collectively referred to as the GT wrapper)
- Customizes, instantiates, and connects the desired number of block RAMs to the Endpoint block (collectively referred to as the block RAM wrapper)
- Customizes, instantiates, and connects a clock module to provide a complete clocking solution for the Endpoint block, GTP/GTX tile, block RAM, and user application
- Customizes, instantiates, and connects a reset module to provide the necessary Endpoint block resets

These features are contained in a single entity, the core or subsystem. The block diagram in Figure 1, page 2 shows the core generated from the CORE Generator tool.

LogiCORE IP Facts				
Core Specifics				
Supported Device Family(1)	Virtex-5 LXT/SXT/FXT			
Resources Used	BUFGs	LUTs	FFs	Block RAMs
	5	35	140 to 564	3 to 40(2)
Resources Used by Reference Design(3)	6	785	909 to 1,335	7 to 44(3)
Provided with Core				
Documentation	Product Specification User Guide			
Design File Formats	Verilog and VHDL Wrappers, Example Design Netlist, Test Bench, Scripts			
Constraints File	.ucf (user constraints file)			
Verification	Hardware: Verilog and VHDL Test Bench Software: Memory Endpoint Reference Design			
Instantiation Template	VHDL Wrapper			
Reference Designs/ Application Notes	Memory Endpoint Reference Design			
Additional Items				
Design Tool Requirements				
Xilinx Implementation Tools	ISE™ 10.1			
Verification	Mentor Graphics® ModelSim® 6.3c, Cadence® IUS 6.1, Synopsys® vcs_mxY-2006.06-SP1 ISE Simulator (ISim) 10.1			
Simulation	Mentor Graphics ModelSim 6.3c, Cadence IUS 6.1, Synopsys vcs_mxY-2006.06-SP1			
Synthesis	XST 10.1, Synplicity® Synplify Pro® 8.9			
Support				
Provided by Xilinx, Inc., www.xilinx.com/support				

1. For more information on Virtex-5 platforms, see DS100: Virtex-5 *Family Overview*.
2. The precise number depends on user configuration.
3. Includes the resources of both the Memory Endpoint Reference Design and the wrappers.

Functional Description

The integrated Endpoint block is highly complex and customizable. The wizard enables users to customize and generate a subsystem for PCIe using a simple set of menu options. The subsystem contains the Endpoint block, GTP/GTX tiles, block RAMs, and clock and reset modules that are automatically configured and connected. The options available in the wizard determine the correct attribute settings and tie off any unused ports. Selecting the desired options in the wizard generates a completely customized core.

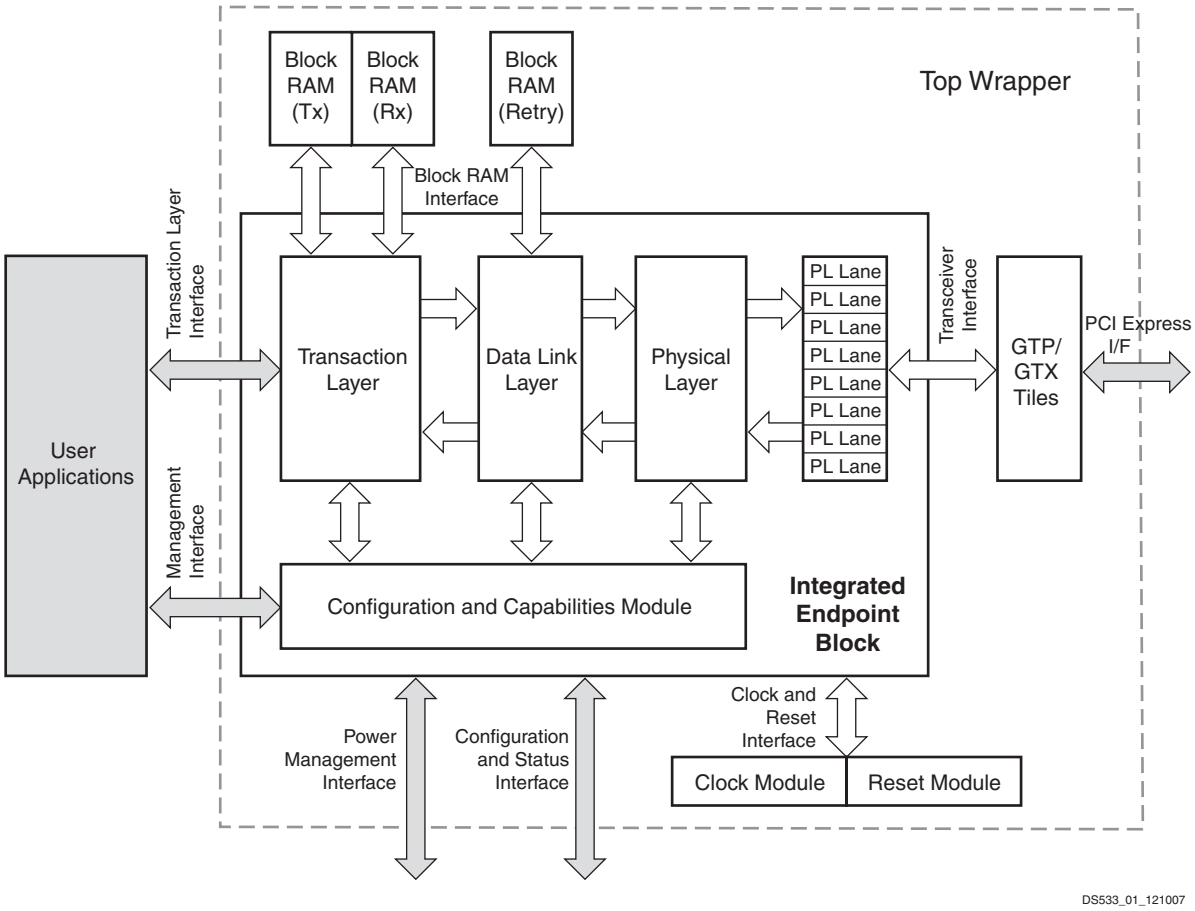

Figure 1: **Integrated Endpoint Block Top-Level Wrapper**

CORE Generator Output

The GUI generates a list of files after the user clicks the Finish button. The key component in the generated files is a set of wrappers containing the customization settings for the Endpoint block, GTP/GTX tiles, block RAM, and clock and reset modules.

The CORE Generator tool automatically generates customized wrappers to connect GTP/GTX tiles and block RAM. Appropriate clock and reset modules are embedded in the top wrapper. These modules allow the user to focus on interfacing with the application, saving valuable time. Figure 1, page 2 illustrates the benefits of using the wrappers. The effort in connecting the Endpoint block to other blocks in the device is greatly reduced with the use of the core.

Top Wrapper

The top wrapper (Figure 1, page 2) contains all the individual wrappers and modules. It serves as the top-level file. User application ports are exposed at the top level. Remaining input ports are tied off to preset values; output ports are kept open. The user is responsible for connecting the following:

- Reference clock to the clock input of the wrapper
- System-level reset signal to the reset input of the wrapper
- Serial pins of the GTP/GTX tile to the system-level serial pins
- User application to the Transaction Layer interface of the wrapper
- Management interface, configuration and status interface, and (optionally) the power management interface of the wrapper to the user application

GT Wrapper

The GT wrapper connects the transceiver interface of the integrated Endpoint block to the GTP/GTX tiles. Based on the user selection in the GUI, the wrapper instantiates the correct number of GTP/GTX tiles with the appropriate attribute settings to configure the GTP/GTX tiles in PCIe mode. Multilane designs are automatically configured for channel bonding. The serial ports of the GT wrapper connect to the serial ports of the top-level wrapper. It then connects to the user application and logic.

Block RAM Wrapper

The block RAM wrapper connects the integrated Endpoint block to the required block RAMs through the block RAM interface. The buffer sizes and block RAM requirements are calculated based on user input. The wrapper instantiates the correct number of block RAMs appropriately. The number of block RAMs is always rounded up to the nearest power of two. When multiple block RAMs are instantiated, they are connected in *gang* mode. In gang mode, the memory bus width is distributed across the multiple block RAMs. All block RAMs that constitute a buffer are enabled simultaneously with the same address bits. For example, a buffer requirement of 16 kB uses four block RAMs by configuring each in a 2k x 16 mode with 11 address pins and 16 data pins. When additional pipelining is needed in the block RAM data/control path, pipelining stages must be added and the buffer latency attributes in the top-level Endpoint block wrapper must be set appropriately.

Clock Module

The clocking requirements of the integrated Endpoint block change based on the number of lanes being used and the frequency of the user application. Based on the user selection, the clocking module is automatically configured to generate the correct clock outputs with the desired frequency.

Reset Module

The integrated Endpoint block requires reset logic in the fabric for correct operation. The required reset logic depends on the RESETMODE attribute setting and the user's reset scheme. The reset module satisfies all the reset requirements of the integrated Endpoint block.

Related Documentation

Complete and up-to-date documentation of the Virtex-5 family of FPGAs is available on the Xilinx website at http://www.xilinx.com/virtex5.

See also:

UG196, *Virtex-5 RocketIO GTP Transceiver User Guide*

UG198, *Virtex-5 RocketIO GTX Transceiver User Guide*

UG197, *Virtex-5 Integrated Endpoint Block for PCI Express Designs Users Guide*

UG350, *Virtex-5 LogiCORE Endpoint Block for PCI Express Designs User Guide*

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Endpoint Block for PCI Express core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator system v10.1 or higher. The CORE Generator system is shipped with Xilinx ISE Foundation Series Development software. This core is provided free of charge to licensed users.

A simulation evaluation license for the core is shipped with the CORE Generator system. To access the full functionality of the core, including FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, please visit the core product page.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/10/06	1.0	Initial Xilinx release.
11/30/06	1.1	Added VHDL support.
03/01/07	2.0	Updated title. Updated *LogiCORE IP Facts* table. Updated Figure 1. Minor typographical edits.
05/17/07	2.1	Added support for SXT devices. Updated resource utilization numbers. Miscellaneous typographical edits.
08/08/07	2.2	Updated design tool requirements.
10/10/07	2.3	Updated design tool requirements.
03/24/08	2.4	Updated design tool requirements and LogiCORE data sheet template.
03/24/08	2.5	Updated design tool requirements. Miscellaneous typographical edits.

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