LogiCORE IP Digital Pre-Distortion v6.0

PB006 October 16, 2012 Product Brief

Introduction

Pre-distortion negates the non-linear effects of a power amplifier (PA) generated when transmitting a wide-band signal. Pre-distortion allows a PA to achieve greater efficiency by operating at higher output power while still maintaining spectral compliance, reducing system capital and operational expenditure.

The solution is targeted for base stations used in third and fourth generation (3G/4G) mobile technologies and beyond. It is a combination of hardware and embedded software processes that between them realize pre-distortion correction along with features that make for a fully engineered, practical, robust and self-contained solution. It is configurable both in feature selection and in usage to support a variety of clocking and resource requirements.

Features

- Algorithms
  - DPD correction with up to 33 dB of ACLR improvement
  - Pre-distortion correction architecture selection for cost-performance trade-off
  - Options to support signal dynamics
  - TDD support with automatic data selection
  - Quadrature modulator correction
  - PA saturation (overdrive) detection
  - Signal capture and analysis
  - Easy integration and evaluation using the Debug Interface utility
- Physical Configuration Parameters
  - Selection of correction architectures of increasing performance/complexity
  - Selection of one, two, four or eight transmit antennas
  - Clock to sample rate ratios from 0.5 to 4
  - Optional Quadrature Modulation Correction (QMC) for either the transmitter or feedback path receiver
  - Optional hardware acceleration of coefficient estimation and signal alignment
- Feedback ADC Interface Options
  - Real IF feedback signal sampled at twice the pre-distortion sample rate with arbitrary IF frequency (optimal performance option)
  - Real IF feedback signal sampled at one times the pre-distortion sample rate with arbitrary IF frequency
  - Zero-IF complex baseband feedback signal sampled at one times the pre-distortion sample rate with integrated QMC.
  - Optional feedback path support for buffered ADC support.

Additional Documentation and Supporting Materials

A product guide and additional supporting materials (Advanced Debug Interface and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/dpd_evaluation/index.htm.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Refer to the IP Release Notes Guide (XTP025) for further information on this core. There is a link to all the DSP IP and then to each core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for each core. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the ISE® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the Digital Pre-Distortion product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/22/11	1.0	Initial Xilinx release. ISE Design Suite 13.2. Previous version of this Product Brief is XMP143.
08/15/11	1.1	Updated to include web registration information.
10/16/12	2.0	Updated for ISE Design Suite 14.3.

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