LogiCORE IP Digital Pre-Distortion v5.0

PB006 August 15, 2011 **Product Brief**

Introduction

Pre-distortion negates the non-linear effects of a power amplifier (PA) generated when transmitting a wide-band signal. Pre-distortion allows a PA to achieve greater efficiency by operating at higher output power while still maintaining spectral compliance, reducing system capital and operational expenditure.

The solution is targeted for base stations used in third and fourth generation (3G/4G) mobile technologies and beyond. It is a combination of hardware and embedded software processes that between them realize pre-distortion correction along with features that make for a fully engineered, practical, robust and self-contained solution. It is configurable both in feature selection and in usage to support a variety of clocking and resource requirements.

Features

- Algorithms
  - DPD correction with up to 33 dB of ACLR improvement
  - Pre-distortion correction architecture selection for cost-performance trade-off
  - Dynamics options
  - TDD support with automatic data selection
  - Quadrature modulator correction
  - PA saturation (overdrive) detection
  - Signal capture and analysis
  - Easy integration and evaluation using the Debug Interface utility
- Physical Configuration Parameters
  - Selection of correction architectures of increasing performance/complexity
  - Selection of polynomial order of 5 or 7
  - Selection of one, two, four or eight transmit antennas
  - Clock to sample rate ratios from one to four
  - Optional quadrature modulation correction for either the transmitter or feedback path receiver
  - Optional hardware acceleration of coefficient estimation and signal alignment
- Interface Options
  - Real IF feedback signal sampled at twice the pre-distortion sample rate with arbitrary IF frequency (optimal performance option)
  - Real IF feedback signal sampled at one times the pre-distortion sample rate with arbitrary IF frequency
  - Zero-IF complex baseband feedback signal sampled at one times the pre-distortion sample rate with integrated QMC.
  - Optional feedback path support for buffered ADC support.

Resource Requirements and Performance

Table 1 and Table 2 show the resource utilization for selected physical configuration parameters for the supported device families. Correction architecture D generally gives the highest performance.

Table 1: **Resource Utilization on Virtex-6**

TX	Architecture	Clocks/ Sample	Poly. Order	QMC	HWA	FFs	LUTs	Slices	Block RAM 36K/18K(1)	DSP48E1s
1	D	4	7	0	0	3927	3383	1752	55/0	14
1	D	4	7	1	0	4001	3375	1677	55/0	17
1	D	4	7	2	0	3884	3330	1679	55/0	14
1	D	4	7	1	1	5742	4533	2071	64/10	37
1	D	4	7	0	1	5644	4704	2072	64/10	34
1	D	4	7	0	2	6824	6097	2825	68/10	47
1	D	4	7	0	3	9162	7489	3655	68/10	78
2	D	4	7	0	3	10385	8611	3391	76/10	85

Notes:

1. In some configurations Virtex-6 cases use a number of 18K block RAMs in addition to full 36K block RAMs.

Table 2: **Resource Utilization on Kintex-7**

TX	Architecture	Clocks/ Sample	Poly. Order	QMC	HWA	FFs	LUTs	Slices	Block RAM 36K/18K(1)	DSP48E1s
1	D	4	7	0	0	3913	3400	1708	55/0	14
1	D	4	7	1	0	4047	3351	1693	55/0	17
1	D	4	7	2	0	3906	3228	1795	55/0	14
1	D	4	7	1	1	5774	4515	2263	64/10	37
1	D	4	7	0	1	5645	4571	2265	64/10	34
1	D	4	7	0	2	6843	5964	2844	68/10	47
1	D	4	7	0	3	9189	7424	3606	68/10	78
2	D	4	7	0	3	10437	8151	4190	76/10	85

Notes:

1. In some configurations Kintex-7 cases use a number of 18K block RAMs in addition to full 36K block RAMs.

Power Amplifer Correction Performance Example

The core has been tested with signals representative of various air interface standards. Testing is carried out with an industry standard radio card and power amplifier. Figure 1 shows the performance for a WCDMA test case with different correction architectures.

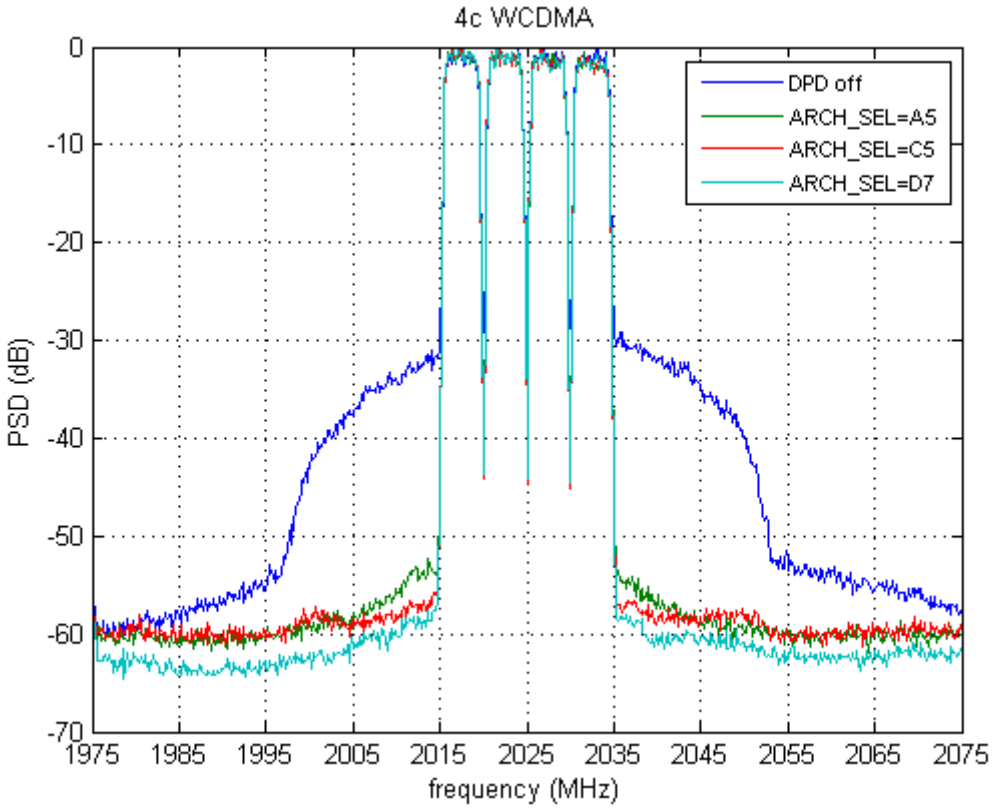

Figure 1: **Spectra for Four WCDMA Carriers before and after DPD**

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (Advanced Debug Interface and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/dpd_evaluation/index.htm.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Refer to the IP Release Notes Guide (XTP025) for further information on this core. There is a link to all the DSP IP and then to each core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for each core. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator software v13.2 and later. The Xilinx CORE Generator system is shipped with Xilinx ISE Design Suite development software.

To order Xilinx software, contact your local Xilinx sales representative.

Information on additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/22/11	1.0	Initial Xilinx release. ISE Design Suite 13.2. Previous version of this Product Brief is XMP143.
08/15/11	1.1	Updated to include web registration information.

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