LogiCORE IP DisplayPort v2.3

DS802 June 22, 2011 **Product Specification**

Introduction

The Xilinx LogiCORE™ IP DisplayPort™ interconnect protocol is designed for transmission and reception of serial-digital video at two standard rates of 1.62 Gb/s and 2.7 Gb/s for consumer and professional displays. DisplayPort is a high-speed serial interface standard supported by industry leaders in consumer HDTV, PC laptop and PC Monitors. This protocol replaces DVI and HDMI™ outside and LVDS inside the box for higher resolution, higher frame rate and color bit depth display. DisplayPort offers a smaller design, two-way interaction, improved signal integrity, and reduced EMI while providing faster speed.

The Xilinx DisplayPort solution is designed to the Video Electronics Standards Association (VESA) *DisplayPort Standard v1.1a* specification [Ref 1].

Features

- Source (TX) and Sink (RX) Controllers
- Designed to VESA *DisplayPort Standard v1.1a* and *HDCP Specification rev. 1.3.*
- Hardware tested
- One or two pixel-wide video interface supporting up to a 2560x1600 monitor resolution
- 1,2 or 4 lanes at 1.62 or 2.7 Gb/s
- RGB and YCbCr color space, up to 16 bits per color
- Auto lane rate and width negotiation
- I2C over a 1 Mb/s AUX channel

LogiCORE IP Facts				
Core Specifics				
Supported Device Family(1)	Virtex-7, Kintex-7, Virtex-6, Spartan-6			
Supported User Interfaces	AXI4-Lite			
Resources Used				
	I/O (to pins)	LUTs	FFs	Block RAMs
Sink	12	~7200	~4825	4
Source	13	~7700	~3325	12
Provided with Core				
Documentation	Product Specification User Guide			
Design File Formats	Verilog and VHDL NGC Netlist Scripts for Unix and Windows			
Constraints File	.ucf (user constraints file) Full Timing Constraints Transceiver Physical Constraints			
Verification	Verilog Test Bench			
Instantiation Template	Verilog and VHDL Wrapper			
Example Design	Simple RTL Source Policy Maker RTL Sink Policy Maker RTL EDID ROM, RTL I2C Controller Demonstration Test Bench			
Design Tool Requirements				
Xilinx Implementation Tools	ISE 13.2			
Verification(2)	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator Synopsys VCS and VCS MX			
Simulation(2)	Mentor Graphics ModelSim			
Synthesis	Xilinx XST			
Support				
Provided by Xilinx, Inc.				

1. For a complete listing of supported devices, see the release notes for this core.
2. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Functional Overview

Source Core

The Source core moves a video stream from a standardized main link through a complete DisplayPort Link Layer, and onto High-Speed Serial I/O for transport to a Sink device.

Main Link

The Main Link for the Source core interfaces to a user-driven stream of video data. Using horizontal and vertical sync signals for framing, this user interface matches the industry standard for display controllers and plugs into existing video streams. The user can specify one or two pixel-wide data through a register field. The user can also specify the number of bits per pixel as well as colorspace (RGB or YCbCr). The user must provide an accompanying video clock that operates between 13.5 and 135 MHz.

The Source core is responsible for managing the video data and preparing it for transmission over the high-speed serial I/O. It performs all of the required operations for the Link and Physical Layers of the *DisplayPort Standard v1.1a* [Ref 1]. A pre-synthesis directive includes this module, which then can be enabled and disabled through register access. HDCP is not included in the standard CORE Generator output, but can be provided on request. Contact Xilinx for more details about this feature.

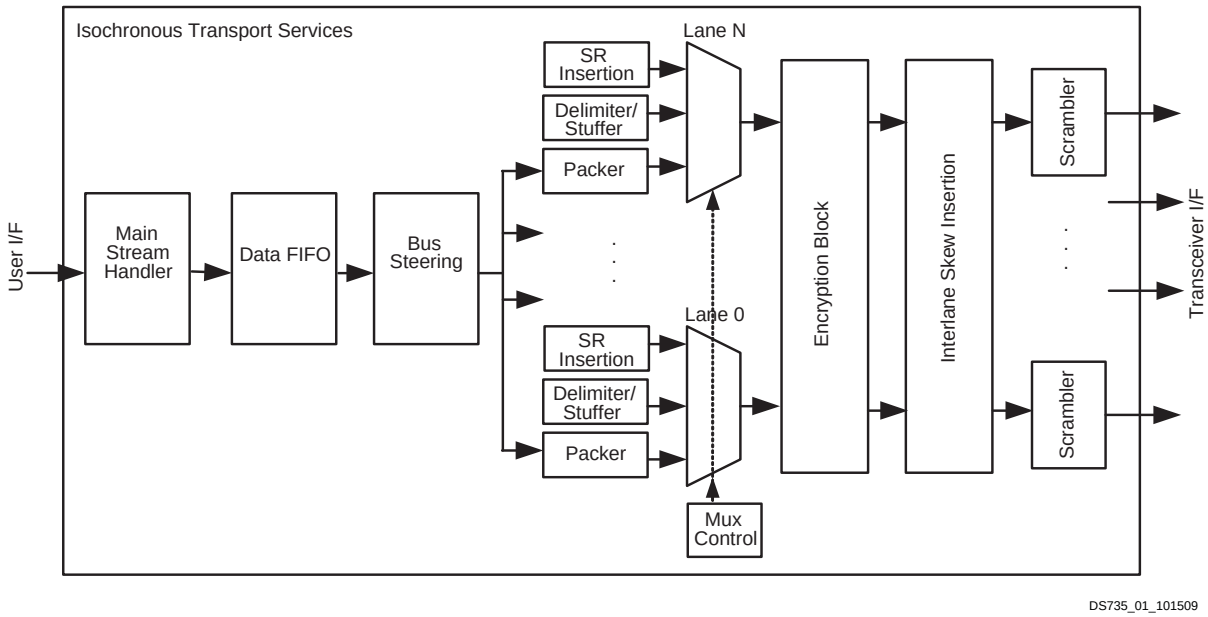

Figure 1: **Source Main Link Datapath**

Secondary Channel

The current version of the DisplayPort IP does not support the secondary Audio Channel.

Host Interface

The core can be configured through the AMBA® AXI4-Lite processor interface. The registers are mapped as packed 32-bit values from the perspective of the interface.

AUX Channel

The AUX Channel provides peer information between source and sink endpoints. The core is also designed to facilitate I2C communication over this link.

High-Speed Serial I/O

The user can specify up to four lanes through the Xilinx CORE Generator™ GUI. Though more lanes can be selected, the actual number in use is determined by a negotiation procedure between endpoints. The instantiations of the transceivers have been brought to the top and provided to the user for greater visibility.

Sink Core

The Sink device accepts incoming serial data streams from the High-Speed Serial I/O, properly reconstructs the original data to an appropriate format, and provides a video stream in a standard format on the main link. It performs all of the required operations for the Link and Physical Layers of the *DisplayPort Standard v1.1a*.

Main Link

The Main Link for the Sink Core drives a stream of video data toward the user. Using horizontal and vertical sync signals for framing, this user interface matches the industry standard for display controllers and plugs in to existing video streams with little effort. Though the core provides data and control signaling, the user is still expected to supply an appropriate clock. This clock can be generated with the use of M and N values provided by the core. Alternatively, the user might want to generate a clock by other means. The core's underflow protection allows the user to use a fast clock to transfer data into a frame buffer.

The user can specify one or two pixel-wide data through a register field. The bit width and format is determined from the Main Stream Attributes, which are provided as signals in the Main Link as well as register fields.

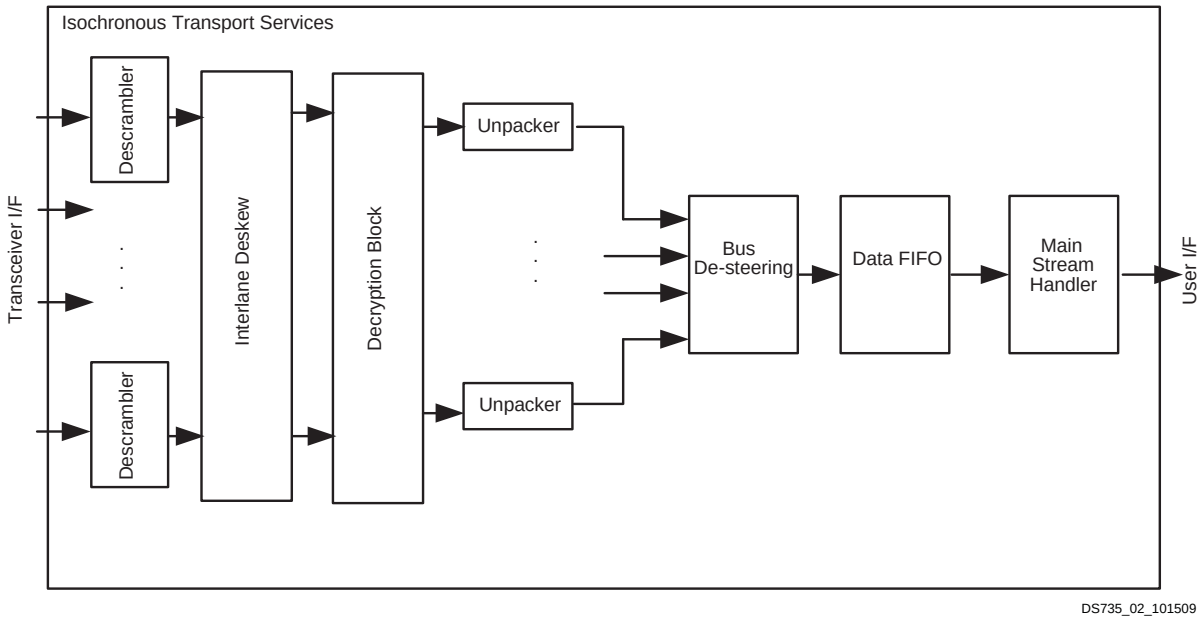

Figure 2: **Sink Main Link Datapath**

Secondary Channel

The current version of the DisplayPort IP does not support the secondary Audio Channel.

Host Interface

The core can be configured through the AMBA AXI4-Lite processor interface. The registers are mapped as packed 32-bit values from the perspective of the interface.

AUX Channel

The AUX Channel provides peer information between source and sink endpoints. The core is also designed to facilitate I2C communication over this link.

High-Speed Serial I/O

The user can specify up to four lanes through a pre-synthesis directive. Though more lanes can be selected, the actual number in use is determined by a negotiation procedure between endpoints. The instantiations of the transceivers have been brought to the top and provided to the user for greater visibility.

Policy Maker System Example Reference Design

Xilinx provides both Source and Sink DisplayPort controllers. The RTL-based Sink Policy Maker is suitable for core bring up and link maintenance. It enables the core, asserts Hot Plug Detect, and enables the Display Timing Generator. For users who desire finer tuning of the link, this Policy Maker is provided as open source.

Two Source Policy Maker options are available to the purchaser of the DisplayPort core. The first is a simple RTL-based controller. Use this version for a quick simulation or fast training against the Xilinx Sink DisplayPort core in hardware. As with the Sink version, this is provided as open source for user tuning. This version should not be used in applications that require compliance to the VESA specification.

For full compliance, Xilinx provides a second netlist-based Source Policy Maker. This version is ideal for hardware bring up and productization. It is based off of a MicroBlaze™ design running C code, which is also available to the purchaser of this core. For information about acquiring the source code, contact your local Xilinx sales office. See Ordering Information, page 9 for more details.

XAPP493, *Implementing a DisplayPort Source Policy Maker Using a MicroBlaze Embedded Processor*, describes the implementation of a DisplayPort Source Policy Maker targeted specifically for the Spartan-6 FPGA Consumer Video Kit (CVK).

I/O Signals

Table 1: **Source Core I/O Signals**

Signal Name[1]	Direction From Core	Description
reset	Input	Core global reset.
Processor Interface		
s_axi_aclk	Input	AXI Bus Clock.
s_axi_aresetn	Input	AXI Reset. Active low.
s_axi_awaddr[31:0]	Input	Write Address.
s_axi_awprot[2:0]	Input	Protection type.
s_axi_awvalid	Input	Write address valid.
s_axi_awready	Output	Write address ready.
s_axi_wdata[31:0]	Input	Write data bus.

Table 1: **Source Core I/O Signals *(Cont'd)***

Signal Name[1]	Direction From Core	Description
s_axi_wstrb[3:0]	Input	Write strobes.
s_axi_wvalid	Input	Write valid.
s_axi_wready	Output	Write ready.
s_axi_bresp[1:0]	Output	Write response.
s_axi_bvalid	Output	Write response valid.
s_axi_bready	Input	Response ready.
s_axi_araddr[31:0]	Input	Read address.
s_axi_arprot[2:0]	Input	Protection type.
s_axi_arvalid	Input	Read address valid.
s_axi_arready	Output	Read address ready.
s_axi_rdata[31:0]	Output	Read data.
s_axi_rresp[1:0]	Output	Read response.
s_axi_rvalid	Output	Read valid.
s_axi_rready	Input	Read ready.
axi_int	Output	AXI interrupt out.
User Data Interface		
vid_clk	Input	User data video clock.
vid_vsync	Input	Vertical sync pulse.
vid_hsync	Input	Horizontal sync pulse.
vid_oddeven	Input	Odd/even field select.
vid_enable	Input	User data video enable.
vid_pixel0[47:0]	Input	Video data.
vid_pixel1[47:0]	Input	Video data.
vid_rst	Input	User video reset.
Main Link Interface		
lnk_clk_p	Input	Differential clock input from pin.
lnk_clk_n	Input	Differential clock input from pin.
lnk_clk	Output	Reference clock for the FPGA fabric.
lnk_tx_lane_p[3:0]	Output	High-speed lane serial data.
lnk_tx_lane_n[3:0]	Output	High-speed lane serial data.
AUX Channel Interface		
aux_tx_in_channel_p	Input	Positive polarity of the AUX Manchester-II data.
aux_tx_in_channel_n	Input	Negative polarity of the AUX Manchester-II data.
aux_tx_out_channel_p	Output	Positive polarity of the AUX Manchester-II data.
aux_tx_out_channel_n	Output	Negative polarity of the AUX Manchester-II data.
I2C Interface		

Table 1: **Source Core I/O Signals *(Cont'd)***

Signal Name[1]	Direction From Core	Description
i2c_sda_in	Input	I2C serial data in.
i2c_sda_enable_n	Output	I2C data out enable. Active low.
i2c_scl_in	Input	I2C serial clock in.
i2c_scl_enable_n	Output	I2C serial clock output enable. Active low
HPD Interface		
hpd	Input	Hot Plug Detect.

1. Signal names beginning with s_ or m_ denote slave and master interfaces respectively.

Table 2: **Sink Core I/O Signals**

Signal Name[1]	Direction From Core	Description
reset	Input	Core global reset.
Processor Interface		
s_axi_aclk	Input	AXI Bus Clock .
s_axi_aresetn	Input	AXI Reset. Active low.
s_axi_awaddr[31:0]	Input	Write Address.
s_axi_awprot[2:0]	Input	Protection type.
s_axi_awvalid	Input	Write address valid.
s_axi_awready	Output	Write address ready.
s_axi_wdata[31:0]	Input	Write data bus.
s_axi_wstrb[3:0]	Input	Write strobes.
s_axi_wvalid	Input	Write valid.
s_axi_wready	Output	Write ready.
s_axi_bresp[1:0]	Output	Write response.
s_axi_bvalid	Output	Write response valid.
s_axi_bready	Input	Response ready.
s_axi_araddr[31:0]	Input	Read address.
s_axi_arprot[2:0]	Input	Protection type.
s_axi_arvalid	Input	Read address valid.
s_axi_arready	Output	Read address ready.
s_axi_rdata[31:0]	Output	Read data.
s_axi_rresp[1:0]	Output	Read reponse.
s_axi_rvalid	Output	Read valid.
s_axi_rready	Input	Read ready.
axi_int	Output	AXI interrupt out.
User Data Interface		
vid_clk	Input	User data video clock.

Table 2: **Sink Core I/O Signals *(Cont'd)***

Signal Name[1]	Direction From Core	Description
vid_vsync	Output	Vertical sync pulse.
vid_hsync	Output	Horizontal sync pulse.
vid_oddeven	Output	Odd/even field select.
vid_enable	Output	User data video enable.
vid_pixel0[47:0]	Output	Video data.
vid_pixel1[47:0]	Output	Video data.
vid_rst	Input	User video reset.
Main Link Interface		
lnk_clk	Output	Reference clock for the FPGA fabric.
lnk_clk_p	Input	Differential clock input from pin.
lnk_clk_n	Input	Differential clock input from pin.
lnk_rx_lane_p[3:0]	Input	High-speed lane serial data.
lnk_rx_lane_n[3:0]	Input	High-speed lane serial data.
lnk_m_vid[23:0]	Output	M-value for clock generation.
lnk_n_vid[23:0]	Output	N-value for clock generation.
lnk_m_aud[7:0]	Output	M-value for audio clock generation.
AUX Channel Interface		
aux_rx_in_channel_p	Input	Positive polarity of the AUX Manchester-II data.
aux_rx_in_channel_n	Input	Negative polarity of the AUX Manchester-II data.
aux_rx_out_channel_p	Output	Positive polarity of the AUX Manchester-II data.
aux_rx_out_channel_n	Output	Negative polarity of the AUX Manchester-II data.
I2C Interface		
i2c_sda_in	Input	I2C serial data in.
i2c_sda_enable_n	Output	I2C data out enable. Active low.
i2c_scl_in	Input	I2C serial clock in.
i2c_scl_enable_n	Output	I2C serial clock output enable. Active low.
HPD Interface		
hpd	Output	Hot Plug Detect.
Main Stream Attributes		
msa_hres[15:0]	Output	Horizontal resolution.
msa_hspol	Output	Horizontal sync polarity.
msa_hswidth[15:0]	Output	Horizontal sync width.
msa_hstart[15:0]	Output	Horizontal active data timing.
msa_htotal[15:0]	Output	Horizontal total clock count.
msa_vres[15:0]	Output	Vertical resolution.
msa_vspol	Output	Vertical sync polarity.

Table 2: **Sink Core I/O Signals *(Cont'd)***

Signal Name(1)	Direction From Core	Description
msa_vswidth[15:0]	Output	Vertical sync width.
msa_vstart[15:0]	Output	Vertical active data timing.
msa_vtotal[15:0]	Output	Vertical total line count.

1. Signal names beginning with `s_` or `m_` denote slave and master interfaces respectively.

Parameterization

Table 3: **Core Parameters**

Parameter Name	Values (Default)	Description
LANE COUNT	{1, 2, **4**}	Number of high-speed SerDes the design contains.
IEEE OUI	24-bit value	This Sink-only parameter allows the user to hardwire the OUI value within the core.
C_BASEADDR	0x8000_0000	Set base Address of slave.
C_HIGHADDR	0x8000_0FFF	Set high address of slave memory map.

Verification

The DisplayPort cores have been verified with extensive simulation and hardware validation.

Simulation

A highly-parameterizable transaction-based test bench was used to test the core. Broad protocol and implementation-specific coverage were used to fully verify the cores. The tests included the following:

- Full I2C operation over the AUX channel
- Bandwidth and performance tests
- Main link stress tests
- Processor interface register read and write accesses
- Scramble/Descramble quality checks

Hardware Validation

The DisplayPort cores have been validated using DNMEG_V5T_PCIE boards from The Dini Group and a Spartan-6 FPGA Consumer Video Kit (CVK) from TED. The hardware has been tested against Quantum Data's 882 Test Instrument for compliance to the DisplayPort standard. The cores were also tested against established, certified products for interoperability.

Family Support

The cores can operate at full speed with a Virtex-6 -1 grade part, Spartan-6 -3 grade part or XA Spartan-6 -3 grade part. The supported device families are:

- Virtex-7
- Kintex-7
- Virtex-6 LXT
- Virtex-6 SXT
- Virtex-6 HXT
- Spartan-6 LXT
- XA Spartan-6 LXT

References

1. VESA *DisplayPort Standard v1.1a*, January 11, 2008.
2. UG386, *Spartan-6 FPGA GTP Transceivers User Guide*.
3. UG371, *Virtex-6 FPGA GTH Transceivers User Guide*.
4. UG366, *Virtex-6 FPGA GTX Transceivers Advance Product Specification*.
5. Spartan-6 FPGA Consumer Video Kit
6. XAPP493, *Implementing a DisplayPort Source Policy Maker Using a MicroBlaze Embedded Processor.*
7. High-bandwidth Digital Content Protection System v1.3 Amendment for DisplayPort, v1.0
8. AMBA AXI Protocol, v2.0
9. UG476, *7 Series FPGAs GTX Transceivers User Guide*

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License. The core is generated using the CORE Generator software provided with the Xilinx ISE® Design Suite.

To evaluate this core at no charge, refer to the evaluation instructions on the DisplayPort product page, located at www.xilinx.com/products/ipcenter/EF-DI-DISPLAYPORT.htm. To access the full core functionality in simulation and in hardware, you must purchase and install a full license for the core.

Contact your local Xilinx sales representative for information on pricing and availability of this and other Xilinx LogiCORE IP modules. Information about additional modules can be found at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
9/21/10	1.0	Initial Xilinx release.
3/1/2011	2.0	Updated core to v2.2 and ISE Design Suite to v13.1.
6/22/2011	3.0	Updated core to v2.3 and ISE Design Suite to v13.2. Added support for Virtex-7 and Kintex-7 devices. Removed support for Virtex-5 devices. Amended HDCP support.

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