Virtex-5 FPGA CRC Wizard v1.3

DS589 March 24, 2008 **Product Specification**

Introduction

The LogiCORE™ IP Cyclic Redundancy Check (CRC) Wizard provides a LocalLink wrapper for the CRC integrated block available in the Virtex™-5 LXT, SXT, and FXT platforms. The CRC Wizard can be customized to suit a wide variety of requirements.

CRC is an error checking mechanism for a block of data, such as a frame of network traffic. CRCs are popular because they are simple to implement in digital hardware, are easy to analyze mathematically, and are particularly good at detecting common errors caused by noise in transmission channels.

Features

- LocalLink wrapper for simple user interface
- Instantiates CRC blocks on the Virtex-5 LXT/SXT/FXT platforms
- Uses CRC32 polynomial
- Two 32-bit input CRC blocks (CRC32) can be combined into one 64-bit input CRC block (CRC64)
- Easy-to-use framing user interface
- Supports variable REM feature
- Options to complement/transpose user data or CRC

LogiCORE IP Facts	
Core Specifics	
Supported Device Family (1)	Virtex-5 LXT/SXT/FXT
Provided with Core	
Documentation	Product Specification User Guide
Design File Formats	Verilog and VHDL
Constraints File	.ucf (user constraints file)
Verification	Example Design and Test Bench
Instantiation Template	Verilog or VHDL Wrapper
Design Tool Requirements	
Xilinx Implementation Tools	ISE™ 10.1 (2)
Verification	Mentor Graphics® ModelSim® 6.3c
Simulation	Mentor Graphics ModelSim 6.3c
Synthesis	XST 10.1
Support	
Provided by Xilinx, Inc. at www.xilinx.com/support	

1. For more information on the Virtex-5 devices, see DS100 *Virtex-5 Family Overview*
2. ISE Service Packs can be downloaded at http://www.xilinx.com/support/download.htm.

Functional Overview

The CRC is an error checking mechanism for a block of data, such as a frame of network traffic. The CRC Wizard allows the user to configure and use the CRC block in the Virtex-5 LXT/SXT/FXT device using the LocalLink interface (Figure 1).

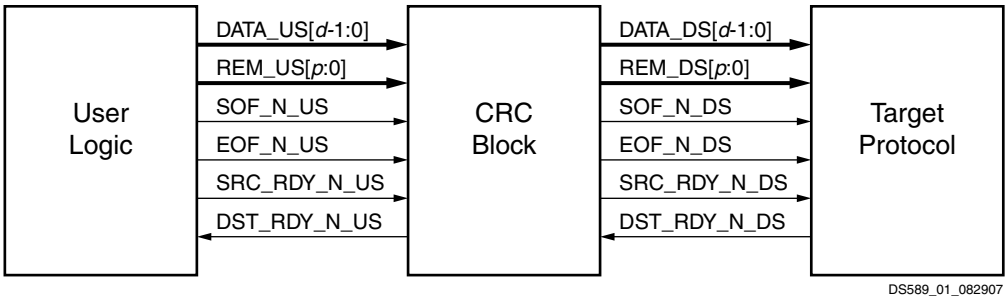

Figure 1: **CRC Block Example**

Application

The CRC Wizard calculates the CRC for packets of data from the user interface. The input of the CRC Wizard can be 32-bits or 64-bits of data.

Functional Description

In Virtex-5 devices, each transceiver tile is paired with two CRC blocks. The CRC blocks can operate independently as two 32-bit input CRC modules (CRC32), or can be combined into a single 64-bit input CRC module (CRC64). The CRC modules use the standard 32-bit Ethernet polynomial for CRC calculation. The CRC blocks are independent of the transceiver blocks.

The CRC Wizard generates two LocalLink compatible CRC modules, TX_CRC and RX_CRC, each instantiating the Virtex-5 CRC block resource (see Figure 2, page 3.) The TX_CRC and RX_CRC modules both have two LocalLink interfaces, upstream and downstream, allowing them to be inserted into the transmit (TX_CRC) or receive (RX_CRC) path of the application design.

The TX_CRC module, Figure 3, page 3, generates a CRC value from data input on the upstream interface. The module inserts the CRC byte(s) at the end of the frame on the downstream interface.

The RX_CRC module, Figure 4, page 3, calculates CRC on the incoming data from the upstream interface while passing the data through to its downstream interface. The downstream interface includes extra signals to indicate whether the incoming frame contains a valid CRC. CRC_PASS_FAIL_N is generated by comparing the CRC calculated at the receive end with the CRC obtained from the transmit end along with data.

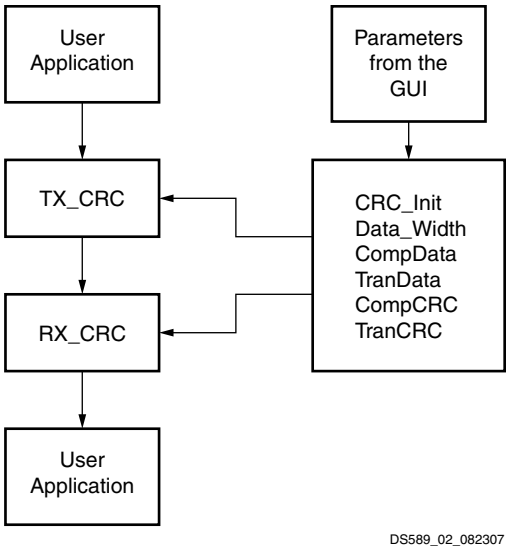

Figure 2: **CRC Wizard Modules**

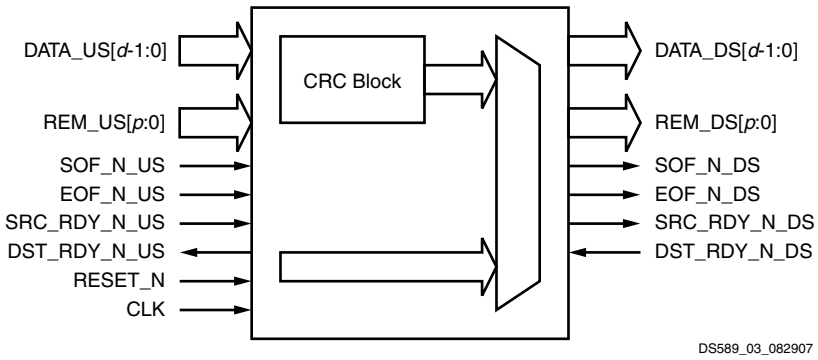

Figure 3: **TX_CRC Module**

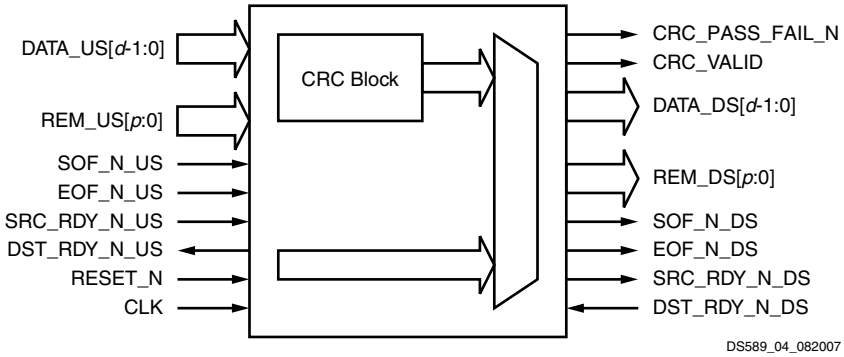

Figure 4: **RX_CRC Module**

Core Parameters

Table 1 shows the core parameters, description, and CRC Wizard value.

Table 1: **Core Parameters**

Parameter	Description	CRC Wizard Value
CRC_Init	The initial value to be loaded to the internal CRC registers for CRC calculation.	32-bit value field
Data_Width	Input data width from the user interface to CRC interface.	32-bit/64-bit
CompData	Some protocols specify that each data byte should be complemented before passing through the CRC calculator. This option permits implementation of this feature.	TRUE/FALSE
TranData	When selected, each RX/TX_DATA byte is transposed before it is passed through the CRC calculator.	TRUE/FALSE
CompCRC	Protocols such as Ethernet and Fibre Channel require a final complementing of each of the CRC bytes. This option permits implementation of this feature.	TRUE/FALSE
TranCRC	When selected, each byte output from the CRC generator is transposed.	TRUE/FALSE

Core Interface

The interface includes all ports required to read and write framed data to and from the CRC integrated block. LocalLink ports with a framing interface are provided. The interface consists of a simple set of data ports with source and destination ready ports. The generated core instantiates two CRC blocks depending on the width selected and includes LocalLink ports for both instances.

Resource Utilization

The number of look-up tables (LUTs) and flip-flops (FFs) used in selected CRC designs are shown in Table 2 (for VHDL) and Table 3 (for Verilog). The CRC design core is also available in configurations not shown in the tables; the estimated cost for these modules can be extrapolated from the tables. The implementation shown uses the example design and is for illustration purposes only.

Table 2: **Virtex-5 VHDL Implementation Resource Utilization**

Design Configuration	CRC Width	Resources Used	
		LUTs	FFs
CRC with variable REM support	32	266	406
	64	492	674
CRC with variable REM support + Transpose CRC Data + Complement CRC Data	32	330	406
	64	637	674

Table 3: **Virtex-5 Verilog Implementation Resource Utilization**

Design Configuration	CRC Width	Resource Used	
		LUTs	FFs
CRC with variable REM support	32	265	406
	64	489	674
CRC with variable REM support + Transpose CRC Data + Complement CRC Data	32	329	406
	64	634	674

Verification

The CRC Wizard was verified using a simulation test bench with a frame-based traffic generator and checker to verify the integrity of the data transmitted with that received. The designs generated through CRC Wizard were tested on hardware for functionality, performance, and reliability using the Xilinx ML523 RocketIO™ characterization platform.

References

1. SP006: *LocalLink Interface Specification*
2. UG189: *Virtex-5 FPGA CRC Wizard v1.3 User Guide*
3. UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*
4. DS100: *Virtex-5 Family Overview*

Revision History

Date	Version	Revision
11/30/06	1.1	Initial Xilinx release.
05/17/07	1.2	LogiCORE CRC Wizard v1.1 release. Updated Table 1, Table 2 and Table 3.
10/10/07	1.3	LogiCORE CRC Wizard 1.2 release. Corrected core parameters in Figure 2 and Table 1. Removed *TX* and *RX* from port names in Figure 3 and Figure 4. Updated LUT and FF resources used in Table 2 and Table 3.
03/24/08	1.4	LogiCORE CRC Wizard v1.3 release. Added FXT device. Updated utilization numbers in Table 2 and Table 3.
03/24/08	1.4.1	Minor non-technical edits.

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