LogiCORE IP CPRI v4.1

DS611 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP CPRI™ core is a high-performance, low-cost flexible solution that implements the Common Packet Radio Interface (CPRI). This core uses state-of-the-art Virtex®-5 FPGA RocketIO™ GTP and GTX transceivers, Virtex-6 FPGA GTXE1 transceivers, Virtex-7 and Kintex™-7 FPGA GTXE2 transceivers or Spartan®-6 FPGA GTPA1 transceivers to implement the Physical Layer, and a compact and customizable Data Link Layer is implemented in the FPGA logic.

Features

- Designs implemented on Virtex-5 LXT/SXT and Spartan-6 LXT devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTP and GTPA1 transceivers.
- Designs implemented on Virtex-5 FXT/TXT devices operate at line rates of 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTX transceivers.
- Designs implemented on Virtex-6 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTXE1 transceivers. Optionally line rates of 4915.2 Mb/s and 6144 Mb/s are supported in these devices.
- Designs implemented on Virtex-7 and Kintex-7 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTXE2 transceivers. Optionally line rates of 4915.2 Mb/s, 6144 Mb/s and 9830.4 Mb/s are supported in these devices.
- Suitable for use in both Radio Equipment Controllers (RECs) and Radio Equipment (RE), including multi-hop systems
- Supports 1 to 32 Antenna-Carriers per core
- Automatic speed negotiation
- Can be configured as master or slave at generation time
- Easy-to-use interface for I/Q data and synchronization
- Supports vendor-specific data transport
- Delay measurement capability meets CPRI Requirement 21 per *CPRI Specification v4.2* [Ref 1]
- Supports both Fast (Ethernet) and Slow (HDLC) Control and Management (C&M) Channels and Management (C&M) Channels per *CPRI Specification v4.2* [Ref 1]
- Designed to *CPRI Specification v4.2*

LogiCORE IP Facts				
Core Specifics				
Supported Device Family[1]	Virtex-7, Kintex-7[2] Virtex-6[3] Spartan-6 Virtex-5 LXT[4]/SXT/FXT/TXT			
Supported User Interfaces	Generic data, status, configuration and management interfaces. AXI4-Lite management interface			
	Resources			
(3072.0 Mb/s default configuration)	**Slices**	**LUTs**	**FFs**	**Block RAMs**
	910	1460	1930	6
(6144.0 Mb/s default configuration)	1120	2050	2720	6
(9830.4 Mb/s default configuration)[5]	1110	2340	3030	6
Provided with Core				
Documentation	Product Specification User Guide			
Design Files	NGC Netlist			
Example Design	VHDL			
Test Bench	VHDL			
Constraints File	.ucf (user constraints file)			
Simulation Models	VHDL, Verilog			
Tested Design Tools				
Design Entry Tools	Xilinx ISE v13.1 software			
Simulation[6]	Mentor Graphics ModelSim v6.6d			
Synthesis Tools	XST			
Support				
Provided by Xilinx, Inc.				

1. For the complete list of supported devices, see the release notes for this core.
2. 6144 Mb/s is only supported on -1 speed grades in FFG type packages and -2 and -3 speed grades in all packages for Virtex-7 and Kintex-7 devices. 9830 Mb/s is only supported on -2 and -3 speed grades in FFG packages.
3. 6144 Mb/s is only supported on -2 and -3 speed grades for Virtex-6 devices.
4. Excludes Virtex-5 LX20T FPGA.
5. Operation at 9.8 Gb/s is supported using a direct connection to a XFP using the XFI electrical specification or SFP+ optical module using SFI electrical specification.
6. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Overview

The CPRI core implements Layer 1 and Layer 2 of the CPRI specification in Xilinx Virtex-7, Kintex-7, Virtex-6, Spartan-6 and Virtex-5 LXT/SXT/FXT devices. The CPRI core provides these client-side interfaces.

- **I/Q Interface.** Consists of a stream of radio data (I/Q samples) that is synchronized to the Universal Mobile Telecommunications System (UMTS) radio frame pulse.
- **Synchronization Interface.** Provides the means for the client logic to synchronize to the network time by transmitting the UMTS radio frame pulse and clock frequency.
- **High-Level Data Link Control (HDLC) Interface.** Transports management information between master and slave. The HDLC interface is serialized and synchronous.
- **Ethernet Interface.** When configured to support speeds of up to 3072 Mb/s or 4915.2 Mb/s, the Ethernet interface is presented as a Media Independent Interface (MII), this allows a 100 Mbit Ethernet Media Access Controller (MAC) to be attached to the core to provide a high-speed channel for management information. When speeds of up to 6144 Mb/s or 9830.4 Mb/s are supported a Gigabit Media Independent Interface (GMII) option is available, this allows a 1 Gbit Ethernet MAC to be attached to the core. The core includes an Ethernet frame buffer in both transmit and receive directions.
- **Vendor-Specific Data Interface.** Provides client logic access to the vendor-specific sub-channels in the CPRI stream.
- **Management Interface.** Provides control and status registers that allow management of the entire design from a supervisory processor.

The architecture of the core is shown in Figure 1. In addition to the interfaces described previously, the core contains these blocks:

- **Status/Alarm Block.** Reflects the internal state of the core and the state of the link.
- **Start-up Sequencer.** Performs line-rate negotiation and Control and Management (C&M) parameter negotiation at link start-up. This block continuously monitors the state of the link and sends the status to the alarm block.
- **UMTS Terrestrial Radio Access - Frequency Division Duplexing (UTRA FDD) I/Q Module:** A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in UTRA FDD systems (shown in Figure 1).
- **Legacy raw I/Q Module**: A pluggable I/Q Module for backward compatibility with the raw interfacing timing for v1.x CPRI cores (not shown in Figure 1).

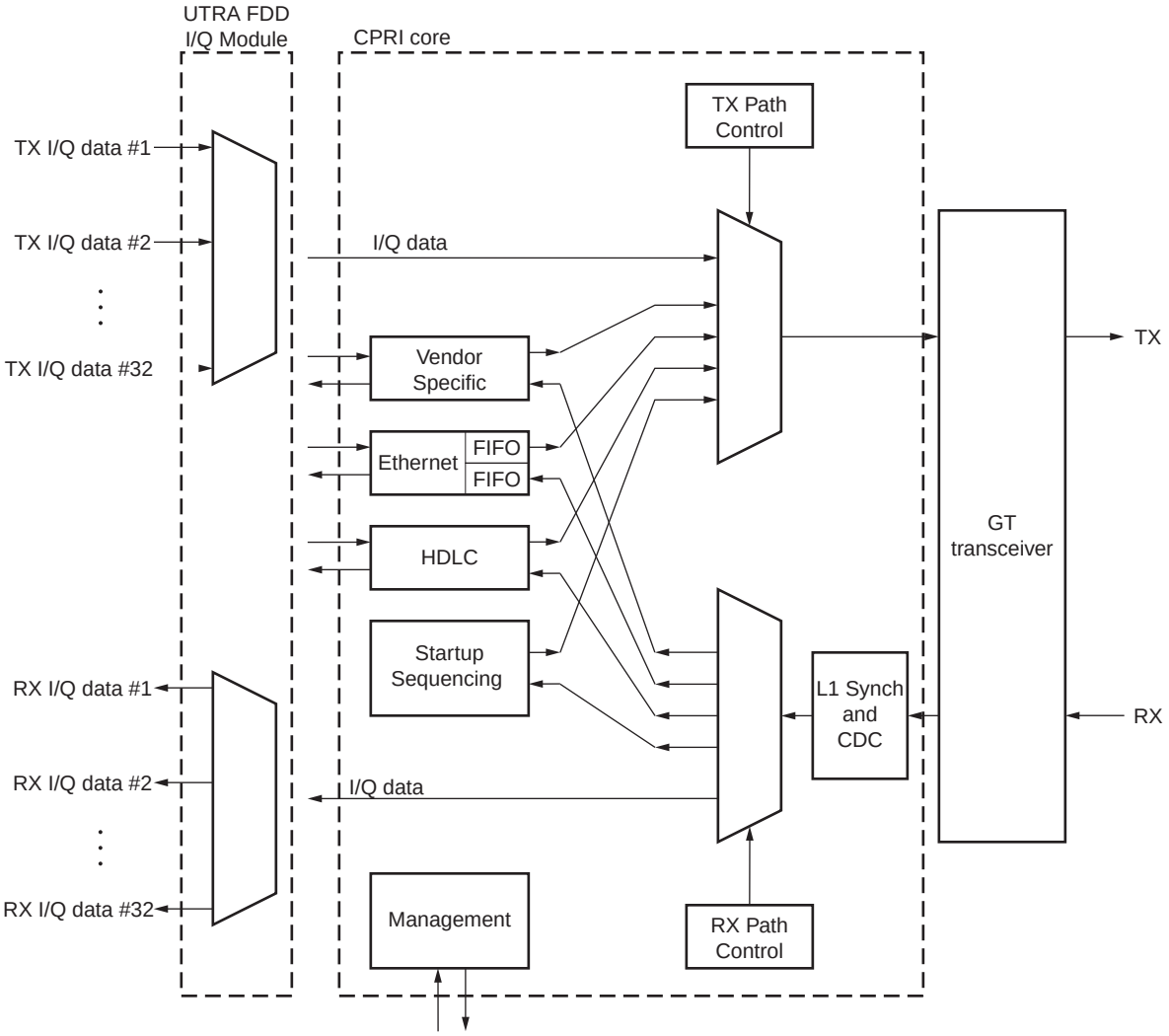

Figure 1: **CPRI Top-Level Block Diagram**

Applications

CPRI is an emerging standard for communication between a Radio Equipment Controller (REC) or Base Station and one or more Radio Equipment (RE) units in a 3G cellular network. The concept is to foster an independent technology evolution for cellular equipment products by defining a publicly available specification for the key internal interface between these units. Figure 2 shows the position of the interface in a cellular system.

The goal of the CPRI interface is to use one physical connection for the radio data (I/Q data), radio unit management (Automatic Gain Control, alarms, etc.) and synchronization (clock frequency control, frame synchronization). Table 1 shows the data rates supported by each Xilinx device. Data is transferred over a single serial link. This link is defined to be electrically compliant with existing high speed serial link standards such as the Gigabit Ethernet and 10 Gigabit Attachment Unit Interface (XAUI) standards.

Table 1: **Supported Data Rates**

	614.4 Mb/s	1228.8 Mb/s	2457.6 Mb/s	3072.0 Mb/s	4915.2 Mb/s	6144.0 Mb/s	9830.4 Mb/s
Virtex-5							
LXT/SXT	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
FXT/TXT	Not supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Virtex-6							
LXT/SXT (-1/-1L speed grade)	Supported	Supported	Supported	Supported	Supported	Not supported	Not supported
LXT/SXT (-2/-3 speed grade)	Supported	Supported	Supported	Supported	Supported	Supported	Not supported
CXT	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Spartan-6	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Virtex-7, Kintex-7							
Non FFG packages (-1 speed grade)	Supported	Supported	Supported	Supported	Supported	Not supported	Not supported
Non FFG packages (-2/-3 speed grade)	Supported	Supported	Supported	Supported	Supported	Supported	Not supported
FFG packages (-1 speed grade)	Supported	Supported	Supported	Supported	Supported	Supported	Not supported
FFG packages (-2/-3 speed grade)	Supported	Supported	Supported	Supported	Supported	Supported	Supported

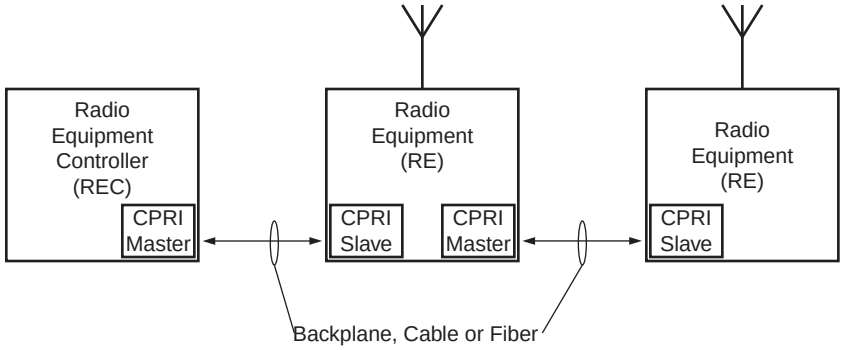

Figure 2: **Location of CPRI in a Cellular System**

Device Utilization

Virtex-5 Devices

Table 2 provides approximate device utilization figures for example configurations of the core in Virtex-5 devices. The values include the GTP/GTX control logic and the clock control logic

Table 2: **Virtex-5 Core Device Utilization[1]**

Parameter Values				Device Resources					
Device	**Ethernet**	**R21**	**Master or Slave**	**LUTs**	**FFs**	**Block RAMs**	**PLLs**	**BUFRs**	**BUFGs**
LXT/SXT	Yes	No	Slave	1370	1780	5	1	1	3
LXT/SXT	Yes	Yes	Slave	1510	1940	5	1	1	3
LXT/SXT	No	No	Slave	970	1190	1	1	1	3
LXT/SXT	No	Yes	Slave	1100	1350	1	1	1	3
LXT/SXT	No	No	Master	950	1170	2	1	1	3
LXT/SXT	No	Yes	Master	1110	1340	2	1	1	3
LXT/SXT	Yes	No	Master	1350	1760	6	1	1	3
LXT/SXT	Yes	Yes	Master	1510	1930	6	1	1	3
FXT	No	No	Slave	980	1160	1	1	1	2
FXT	No	Yes	Slave	1090	1320	1	1	1	2
FXT	Yes	No	Slave	1390	1750	5	1	1	2
FXT	Yes	Yes	Slave	1490	1910	5	1	1	2
FXT	No	No	Master	970	1140	2	1	1	2
FXT	No	Yes	Master	1120	1310	2	1	1	2
FXT	Yes	No	Master	1380	1730	6	1	1	2
FXT	Yes	Yes	Master	1530	1900	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 2 and are external to the core which allows them to be shared.

Virtex-6 Devices (Supporting Speeds of up to 3072.0 Mb/s)

Table 3 provides approximate device utilization figures for example configurations of the 3072.0 Mb/s core in Virtex-6 devices. The values include the GTXE1 control logic and the clock control logic.

Table 3: **Virtex-6 Core Device Utilization (Speeds of up to 3072.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1330	1780	5	1	1	1
Yes	Yes	Slave	1450	1940	5	1	1	1
No	No	Slave	1000	1200	1	1	1	1
No	Yes	Slave	1110	1360	1	1	1	1
No	No	Master	980	1174	2	1	1	1
No	Yes	Master	1120	1350	2	1	1	1
Yes	No	Master	1320	1760	6	1	1	1
Yes	Yes	Master	1460	1930	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 3 and are external to the core which allows them to be shared.

Virtex-6 Devices (Supporting Speeds of up to 4915.2/6144.0 Mb/s)

Table 4 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mb/s core in Virtex-6 devices. The values include the GTXE1 control logic and the clock control logic.

Table 4: **Virtex-6 Core Device Utilization (Speeds of up to 4915.2/6144.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1940	2570	5	1	1	1
Yes	Yes	Slave	2030	2730	5	1	1	1
No	No	Slave	1600	1990	1	1	1	1
No	Yes	Slave	1680	2150	1	1	1	1
No	No	Master	1580	1970	2	1	1	1
No	Yes	Master	1720	2140	2	1	1	1
Yes	No	Master	1920	2550	6	1	1	1
Yes	Yes	Master	2050	2720	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 4 and are external to the core which allows them to be shared.

Spartan-6 Devices

Table 5 provides approximate device utilization figures for example configurations of the core in Spartan-6 devices. The values include the GTPA1 control logic and the clock control logic.

Table 5: **Spartan-6 Core Device Utilization[1]**

Parameter Values				Device Resources				
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	PLLs	DCMs	BUFGs
Yes	No	Slave	1330	1740	7	1	1	4
Yes	Yes	Slave	1450	1900	7	1	1	4
No	No	Slave	980	1140	1	1	1	4
No	Yes	Slave	1100	1310	1	1	1	4
No	No	Master	960	1130	2	1	1	4
No	Yes	Master	1080	1300	2	1	1	4
Yes	No	Master	1310	1720	8	1	1	4
Yes	Yes	Master	1430	1890	8	1	1	4

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 5 and are external to the core which allows them to be shared.

Virtex-7 Devices (Supporting Speeds of up to 3072.0 Mb/s)

Table 6 provides approximate device utilization figures for example configurations of the 3072.0 Mb/s core in Virtex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 6: **Virtex-7 Core Device Utilization (Speeds up to 3072.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1180	1650	5	1	1	1
Yes	Yes	Slave	1280	1810	5	1	1	1
No	No	Slave	850	1070	1	1	1	1
No	Yes	Slave	950	1230	1	1	1	1
No	No	Master	830	1050	2	1	1	1
No	Yes	Master	960	1220	2	1	1	1
Yes	No	Master	1170	1630	6	1	1	1
Yes	Yes	Master	1300	1800	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 6 and are external to the core which allows them to be shared.

Virtex-7 Devices (Supporting Speeds of up to 4915.2/6144.0 Mb/s)

Table 7 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mb/s core in Virtex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 7: **Virtex-7 Core Device Utilization (Speeds of up to 4915.2/6144.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1820	2440	5	1	1	1
Yes	Yes	Slave	1910	2600	5	1	1	1
No	No	Slave	1480	1860	1	1	1	1
No	Yes	Slave	1560	2020	1	1	1	1
No	No	Master	1460	1840	2	1	1	1
No	Yes	Master	1580	2010	2	1	1	1
Yes	No	Master	1800	2420	6	1	1	1
Yes	Yes	Master	1920	2590	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), hires_clk (if R21 is selected) and `aux_clk`. These are not included in Table 7 and are external to the core which allows them to be shared.

Virtex-7 Devices (Supporting Speeds of up to 9830.4 Mb/s)

Table 8 provides approximate device utilization figures for example configurations of the 9830.4 Mb/s core in Virtex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 8: **Virtex-7 Core Device Utilization[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	2250	2910	5	1	1	1
Yes	Yes	Slave	2350	3070	5	1	1	1
No	No	Slave	1870	2330	1	1	1	1
No	Yes	Slave	1960	2490	1	1	1	1
No	No	Master	1830	2280	2	1	1	1
No	Yes	Master	1960	2450	2	1	1	1
Yes	No	Master	2210	2860	6	1	1	1
Yes	Yes	Master	2340	3030	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), hires_clk (if R21 is selected) and `aux_clk`. These are not included in Table 8 and are external to the core which allows them to be shared.

Kintex-7 Devices (Supporting Speeds of up to 3072.0 Mb/s)

Table 9 provides approximate device utilization figures for example configurations of the 3072.0 Mb/s core in Kintex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 9: **Kintex-7 Core Device Utilization (Speeds of up to 3072.0 Mb/s)[1]**

Parameter Values				Device Resources			
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFGs
Yes	No	Slave	1180	1710	5	1	3
Yes	Yes	Slave	1280	1870	5	1	3
No	No	Slave	850	1130	1	1	3
No	Yes	Slave	950	1290	1	1	3
No	No	Master	830	1110	2	1	3
No	Yes	Master	960	1280	2	1	3
Yes	No	Master	1170	1690	6	1	3
Yes	Yes	Master	1300	1860	6	1	3

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 9 and are external to the core which allows them to be shared.

Kintex-7 Devices (Supporting Speeds of up to 4915.2/6144.0 Mb/s)

Table 10 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mb/s core in Kintex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 10: **Kintex-7 Core Device Utilization (Speeds of up to 4915.2/6144.0 Mb/s)[1]**

Parameter Values				Device Resources			
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFGs
Yes	No	Slave	1800	2500	5	1	3
Yes	Yes	Slave	1880	2660	5	1	3
No	No	Slave	1450	1920	1	1	3
No	Yes	Slave	1540	2080	1	1	3
No	No	Master	1440	1900	2	1	3
No	Yes	Master	1550	2070	2	1	3
Yes	No	Master	1780	2480	6	1	3
Yes	Yes	Master	1900	2650	6	1	3

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 10 and are external to the core which allows them to be shared.

Kintex-7 Devices (Supporting Speeds of up to 9830.4 Mb/s)

Table 11 provides approximate device utilization figures for example configurations of the 9830.4 Mb/s core in Kintex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 11: **Kintex-7 Core Device Utilization (Speeds of up to 9830.4 Mb/s)[1]**

Parameter Values				Device Resources			
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFGs
Yes	No	Slave	2250	2970	5	1	3
Yes	Yes	Slave	2350	3130	5	1	3
No	No	Slave	1870	2390	1	1	3
No	Yes	Slave	1960	2550	1	1	3
No	No	Master	1830	2340	2	1	3
No	Yes	Master	1960	2510	2	1	3
Yes	No	Master	2210	2920	6	1	3
Yes	Yes	Master	2350	3090	6	1	3

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 11 and are external to the core which allows them to be shared.

References

1. *CPRI Specification v4.2*, September 29, 2010 (www.cpri.info)
2. *IEEE Standard 802.3-2005* (standards.ieee.org/getieee802)
3. *Xilinx AXI Reference Guide* (UG761)

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed in the documentation, or if customized beyond that allowed in the product documentation, or if any changes are made to the sections marked DO NOT MODIFY.

Ordering Information

The CPRI core can be generated using the Xilinx CORE Generator™ system v13.1 or higher with the applicable service pack. The CORE Generator system is shipped with Xilinx ISE® Design Suite Series Development software.

Related Information

Xilinx products are not intended for use in life-support appliances, devices, or systems. Use of a Xilinx product in such application without the written consent of the appropriate Xilinx officer is prohibited.

List of Acronyms

Acronym	Spelled Out
AXI	Advanced eXtensible Interface
C&M	Control and Management
CPRI	Common Packet Radio Interface
FDD	Frequency Division Duplexing
FF	Flip-Flop
FPGA	Field Programmable Gate Array
GMII	Gigabit Media Independent Interface
HDLC	High-Level Data Link Control
I/Q	in-phase (I) and quadrature-phase (Q) data
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
NGC	Native Generic Circuit
PLL	Phase-Locked Loop
RAM	Random Access Memory
RE	Radio Equipment
REC	Radio Equipment Controller
UCF	User Constraints File
UMTS	Universal Mobile Telecommunications System
UTRA FDD	UMTS Terrestrial Radio Access - Frequency Division Duplexing
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
XAUI	eXtended Attachment Unit Interface
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
08/08/07	1.0	Initial Xilinx release.
3/24/08	1.5	Updated supported tools and performance numbers.
9/05/08	2.1	Early access release.
10/31/08	2.2	Early access release 2.
4/24/09	3.0	Updated to support ISE v11.1.
6/24/09	4.0	Updated to support ISE v11.2.
09/16/09	5.0	Updated to support ISE v11.3.
10/15/09	6.0	Early access release.
4/19/10	7.0	Updated to support ISE v12.1.
7/23/10	8.0	Updated to support ISE v12.2.
3/01/11	9.0	Updated to support ISE v13.1. Supports new Virtex-7 and Kintex-7 devices and AXI4-Lite interconnect.

Notice of Disclaimer