AXI Timebase Watchdog Timer v2.0

LogiCORE IP Product Guide

Vivado Design Suite

PG128 November 18, 2015

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Table of Contents

Introduction

The Xilinx® LogiCORE™ IP AXI4-Lite Timebase Watchdog Timer (WDT) is a 32-bit peripheral that provides a 32-bit free-running timebase and watchdog timer.

Features

- Connects as a 32-bit slave on a AXI4-Lite interface
- Watchdog timer with selectable timeout period and interrupt
- Configurable WDT enable: enable-once or enable-repeatedly
- One 32-bit free-running timebase counter with rollover interrupt-dual control register

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™ Families, UltraScale™ Architecture, Zynq®-7000 All Programmable SoC, 7 Series
Supported User Interfaces	AXI4-Lite
Resources	See Table 2-2.
Provided with Core	
Design Files	VHDL
Example Design	VHDL
Test Bench	VHDL
Constraints File	Delivered with IP generation.
Simulation Model	Not Provided
Supported S/W Driver	Standalone
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite Vivado
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported derivative devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Functional Description

The top-level block diagram for the AXI Timebase Watchdog Timer (WDT) is shown in Figure 1-1.

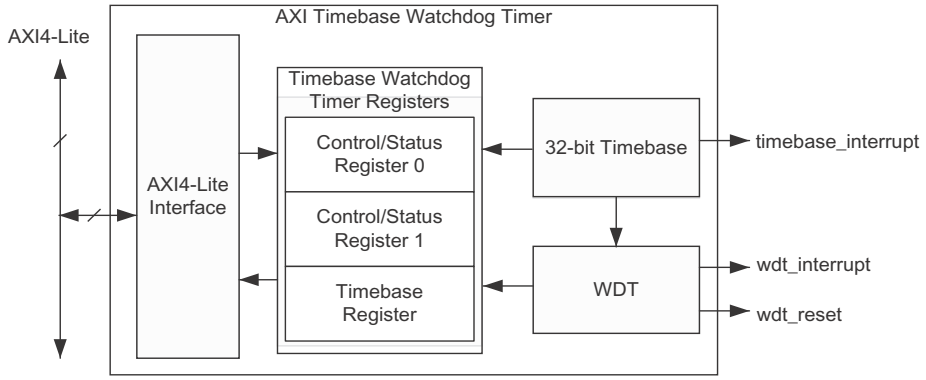

Figure 1-1: **AXI Timebase Watchdog Timer Block Diagram**

- **AXI4-Lite Interface** – AXI4-Lite Interface module implements AXI4-Lite slave interface for accessing memory mapped Timebase WDT registers. For additional information about the AXI4-Lite slave interface, see the specification usage section of the *LogiCORE IP AXI4-Lite IPIF Product Guide* (PG155) [Ref 1].
- **Timebase Watchdog Timer Registers** – Timebase Watchdog Timer register module includes all memory-mapped registers (as shown in Figure 1-1). It consists of a 32-bit Control/Status register 0, a 32-bit Control/Status register 1 and a 32-bit Timebase register (TBR).
- **32-bit Timebase** – 32-bit timebase consists of a free-running 32-bit timebase counter.
- **WDT** – WDT block provides watchdog functionality and generates reset and/or interrupt.
    - WDT uses a dual-expiration architecture. After one expiration of the timeout interval, an interrupt is generated and the WDT state bit is set to one in the status register. If the state bit is not cleared (by writing a one to the state bit) before the next expiration of the timeout interval, a WDT reset is generated.

- When WDT reset is generated, the WDT reset status bit in Status register is set. This bit is used to determine if the last system reset was due to WDT reset or not.
- WDT can only be disabled by writing two distinct addresses, reducing the possibility of inadvertently disabling the WDT in application code. After WDT expires, it can be restarted only by asserting the `s_axi_aresetn` pin.

Operation Overview

Timebase Operation

The timebase is a 32-bit counter that is incremented by one on the rising edge of the input clock. The counter is reset to zero when the reset is asserted or when the WDT is enabled. The Timebase register (TBR) contains the full timebase count value of 32 bits.

The Control/Status register 0 (TWCSR0) contains the most-significant 28 bits of the timebase count, as well as the WDT enable and status bits. The timing resolution from the upper 28 bits of the timebase count is $T_{clk} \times 16$ (T_{clk} is the period of the input clock). As a result, a single access can be used to read the state of the watchdog timer, as well as a reduced resolution version of the timebase.

An interrupt signal (Timebase Interrupt) is provided that pulses High for one clock period as the counter rolls over from 0xFFFFFFFF to 0x00000000. This interrupt can be used by the software to keep track of how many timebase rollovers have occurred.

WDT Operation

The WDT timeout interval is configured by a parameter to be $2^{\text{Width of WDT}}$ clock cycles, where width of WDT parameter is any integer from 8 to 31. The WDT interval is set at core generation time and cannot be modified dynamically through a Control register. Figure 1-2 shows the WDT state diagram.

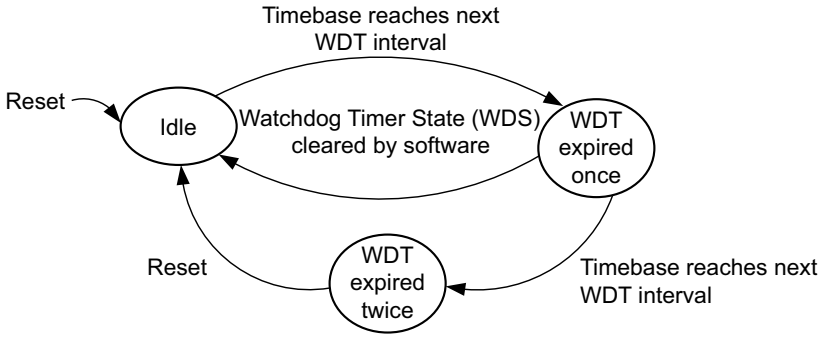

Figure 1-2: **Timebase Watchdog Timer State Diagram**

Feature Summary

- 32-bit slave device on a AXI4-Lite interface
- Watchdog timer with configurable timeout period and interrupt
- Configurable WDT enable: enable-once or enable-repeatedly
- One 32-bit free-running timebase counter with rollover interrupt
- WDT with dual-expiration architecture, where WDT reset is generated if WDT timeout occurs before previous WDT timeout interrupt is cleared by software
- Disabled only with two distinct writes, reducing the possibility of inadvertently disabling

Licensing and Ordering Information

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Performance

Performance characterization of this core was performed using margin system methodology, described in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 2].

Note: System performance numbers for UltraScale™ architecture and Zynq®-7000 AP SoC devices are expected to be similar to 7 series device numbers.

Table 2-1: **AXI Timebase Watchdog Timer System Performance**

FPGA	Speed Grade	F_{Max} (MHz)
		AXI4-Lite
Virtex-7	–1	180
Kintex-7		180
Artix-7		120
Virtex-7	–2	200
Kintex-7		200
Artix-7		140
Virtex-7	–3	220
Kintex-7		220
Artix-7		160

Resource Utilization

Resource requirements for the AXI Timebase Watchdog Timer core have been estimated for 7 series and Zynq-7000 devices (Table 2-2). These values were generated using the Vivado® Design Suite.

Note: Resources numbers for UltraScale architecture and Zynq-7000 devices are expected to be similar to 7 series device numbers.

Table 2-2: **Device Utilization – 7 Series and Zynq-7000 Devices**

Parameter Values		Device Resources		
WDT Width	**WDT Enable Behavior**	**Flip-Flops**	**Slices**	**LUTs**
8	Enable repeatedly	94	39	105
30	Enable only once	94	39	105
31	Enable only once	94	40	106

Port Descriptions

The AXI Timebase Watchdog Timer I/O signals are listed and described in Table 2-3.

Table 2-3: **AXI Timebase WDT I/O Signals**

Signal Name	Interface	I/O	Initial State	Description
s_axi_aclk	Clock	I	–	AXI Clock
s_axi_aresetn	Reset	I	–	AXI Reset, active-Low
s_axi_*	S_AXI	–	–	AXI4-Lite Slave Interface signals. See Appendix A of the *Vivado AXI Reference Guide* (UG1037) [Ref 3] for AXI4, AXI4-Lite and AXI Stream Signals.
wdt_reset		O	0	WDT Reset Status signal (active-High). Asserts on second expiration of the WDT timeout interval.
timebase_interrupt		O	0	Timebase Interrupt (active-High). Asserts for 1 clock pulse upon timebase rollover (0xFFFFFFFF to 0x00000000).
wdt_interrupt		O	0	WDT Interrupt (active-High). Asserts High until WDS bit is cleared in TWCSR0 register.
freeze		I	–	Active-High. Stalls the WDT counters.

Register Space

Table 2-4 shows all the AXI Timebase Watchdog Timer registers and their addresses.

Table 2-4: **AXI Timebase WDT Register Map**

Base Address + Offset	Register Name	Access Type	Default Value (Hex)	Description
BASEADDR + 0x00	TWCSR0	R/W	0x00000000	Control/Status Register 0
BASEADDR + 0x04	TWCSR1	W(1)	0x00000000	Control/Status Register 1, state is mirrored in TWCSR0 for read.
BASEADDR + 0x08	TBR	R(2)	0x00000000	Timebase Register

Notes:

1. Reading of this register returns undefined valued.
2. Writing into this register has no effect.

Control/Status Register 0 (TWCSR0)

Control/Status register 0 contains the watchdog timer reset status, watchdog timer state, and watchdog timer enables. The TWCSR0 bit definitions are explained in Table 2-5.

Table 2-5: **Control/Status Register 0 (0x00)**

Bits	Name	Reset Value	Access Type	Description
31:4	TBR	0	R	Timebase Register (Most significant 28 bits) This read-only field contains the most significant 28 bits of the timebase register. The timebase register is mirrored here so that a single read can be used to obtain the count value and the watchdog timer state if the upper 28 bits of the timebase provide sufficient timing resolution.
3	WRS	0	R/W	Watchdog Reset Status Indicates the WDT reset signal was asserted. This bit is not cleared by a system reset so that it can be read after a system reset to determine if the reset was caused by a watchdog timeout. This bit can be cleared by applying reset to the IP (asserting the `s_axi_aresetn`) followed by writing 1 to this bit. Writing a 0 to this bit has no effect. 0 = WDT reset has not occurred 1 = WDT reset has occurred
2	WDS	0	R/W	Watchdog Timer State Indicates the WDT period has expired. The `wdt_reset` signal is asserted if the WDT period expires again before this bit is cleared by software. Writing a 1 to this bit clears the watchdog timer state. Writing a 0 to this bit has no effect. 0 = WDT period has not expired 1 = WDT period has expired, reset occurs on next expiration

Table 2-5: **Control/Status Register 0 (0x00) *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
1	EWDT1	0	R/W	Enable Watchdog Timer (Enable 1) This bit must be used in conjunction with the EWDT2 bit in the TWCSR1 register. Both bits must be 0 to disable the WDT. 0 = Disable WDT function if EWDT2 also equals 0 1 = Enable WDT function
0	EWDT2	0	R	Enable Watchdog Timer (Enable 2) This bit is read-only and is the only place to read back a value written to Bit[0] of TWCSR1.

Control/Status Register 1 (TWCSR1)

Control/Status register 1 contains the second WDT enable bit. The WDT enable must be cleared in both TWCSR0 and TWCSR1 to disable the WDT. If the WDT is configured as enable-once, then the WDT cannot be disabled after it has been enabled. The TWCSR1 bit definitions are explained in Table 2-6.

Table 2-6: **Control/Status Register 1 (0x04)**

Bits	Name	Reset Value	Access Type	Description
31:1	Reserved	N/A	N/A	Reserved
0	EWDT2	0	W(1)	Enable Watchdog Timer (Enable 2) This bit must be used in conjunction with the EWDT1 bit in the TWCSR0 register to disable the WDT. Both bits must be 0 to disable the WDT. The value of EWDT2 can be read back only in TWCSR0. 0 = Disable WDT function if EWDT1 also equals 0 1 = Enable WDT function

1. Reading of this register returns undefined value.

Timebase Register (TBR)

The Timebase register is the output of a free-running incrementing counter that clocks at the input clock rate (no prescaling of the clock is done for this counter). This register is read-only and is reset by the following:

- A system reset
- Enabling the WDT after power on reset
- Enabling the WDT after the WDT has been disabled. EWDT1 and EWDT2 must both be zero to disable the WDT. The WDT is enabled when either EWDT1 or EWDT2 are set to one. Note that when the WDT mode is enable-once, the TBR can only be reset when the WDT is first enabled.

Table 2-7: **Timebase Register (0x08)**

Bits	Name	Reset Value	Access Type	Description
31:0	TBR	0	R(1)	Timebase Register This register indicates the free-running incrementing counter value.

1. Writing into this register has no effect.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Clocking

The `axi_timebase_wdt` operates on the `s_axi_aclk` clock.

Resets

AXI Timebase WDT resets on `s_axi_aresetn`, which is active-Low and synchronous to `s_axi_aclk`.

Programming Sequence

The following is the programming sequence to reset the AXI Timebase WDT.

1. Set EWDT1 in TWSCR0 register to enable Timebase WDT.
2. With WDT period expired, writing a one to WDS bit clears the WDT timer expiry status.
3. With WDT reset state, Writing a one to WRS bit clears the watchdog reset status bit. Writing a zero to this bit has no effect.
4. Clear both EWDT1 in TWCSR0 register and EWDT2 in TWCSR1 register to disable the Timebase WDT.

Protocol Description

Timing Diagrams

Figure 3-1 shows the operation performed where WDS bit is cleared by the software before the second expiration occurs. Figure 3-2 shows the operation performed where WDS bit is not cleared and WDT expired twice state is reached.

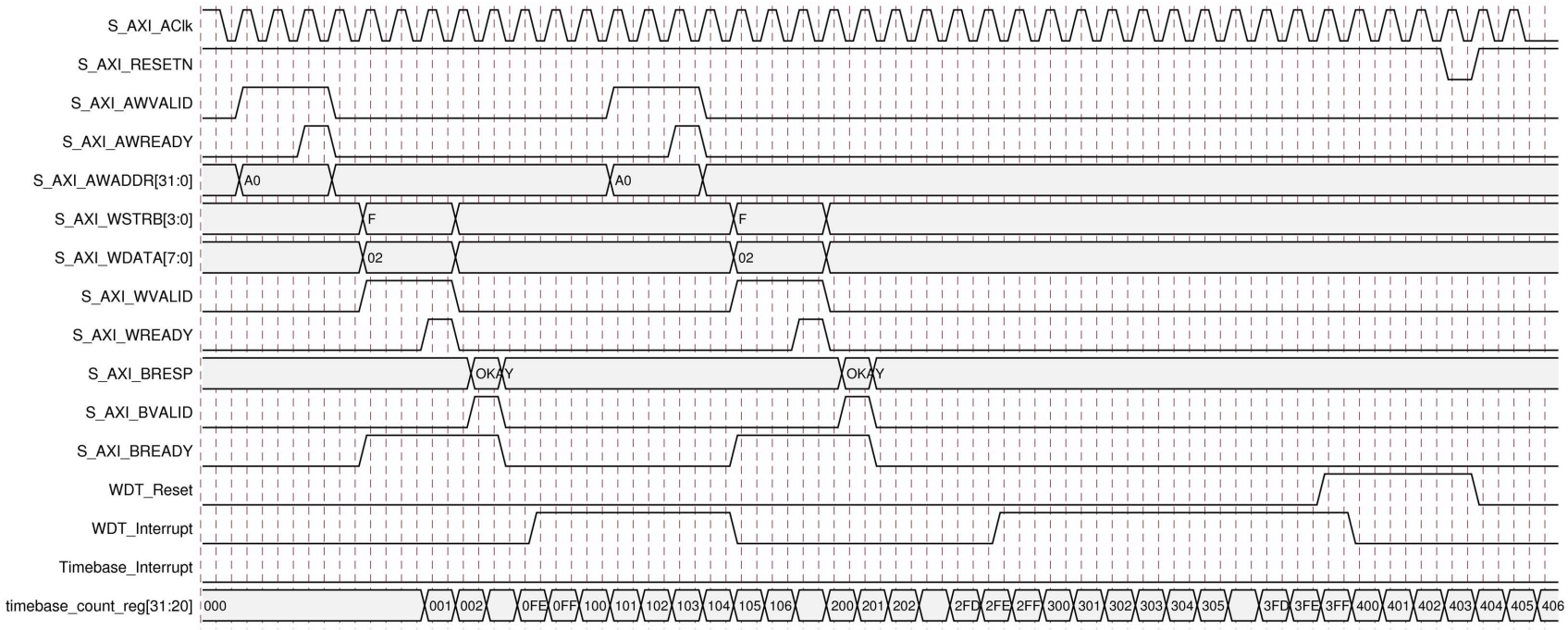

Figure 3-1: **WDT Expired Once Operation Waveform**

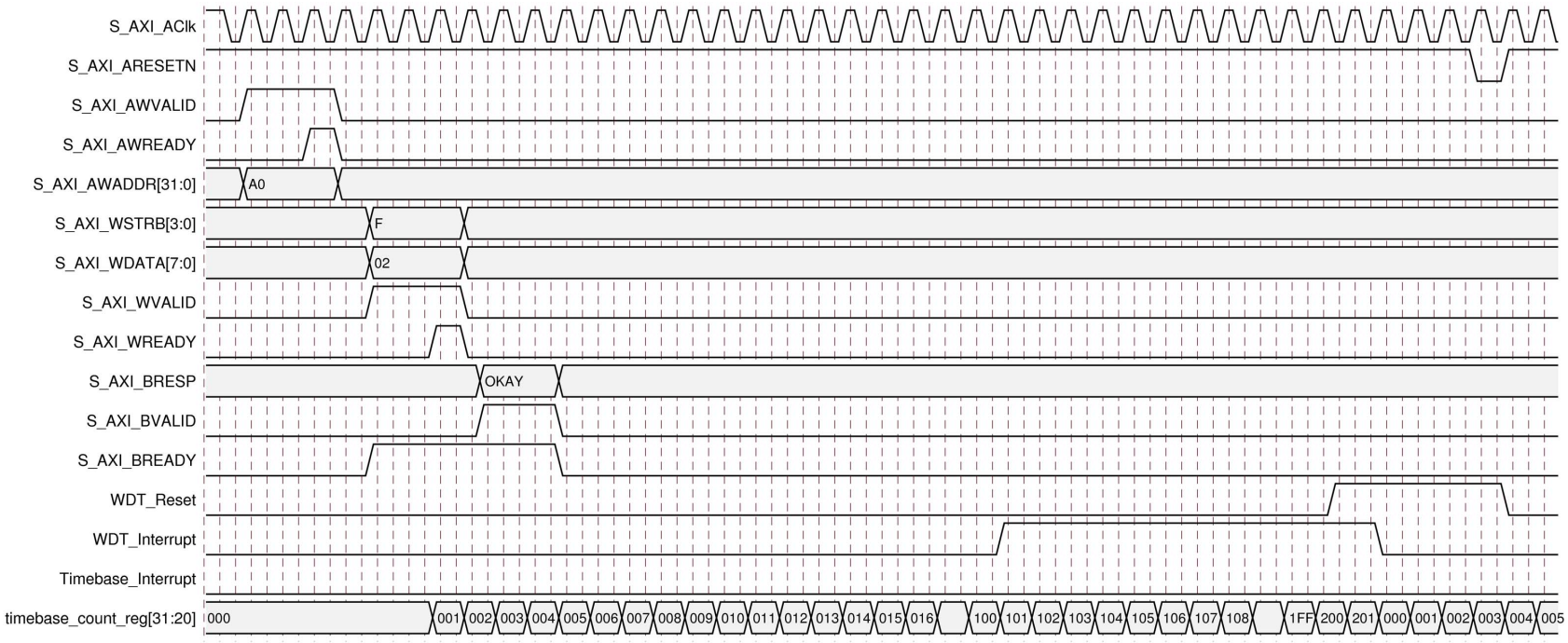

Figure 3-2: **WDT Expired Twice Operation Waveform**

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 2]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6]

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

Vivado Integrated Design Environment

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 2] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5].

Note: Figure in this chapter is an illustration of the Vivado IDE. This layout might vary from the current version.

Figure 4-1 shows the Customize IP window settings for AXI Timebase WDT IP core.

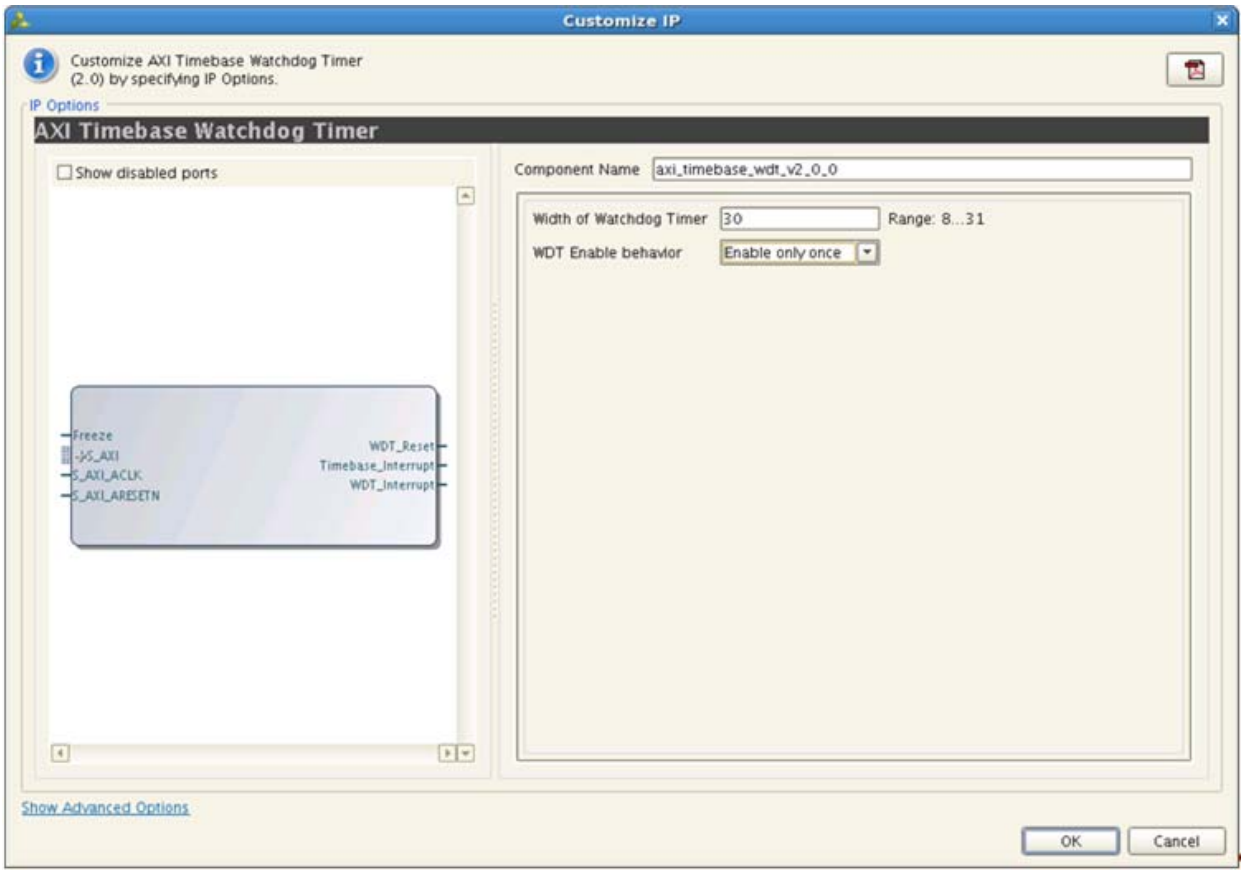

Figure 4-1: **Vivado Customize IP Dialog Box**

The AXI Timebase WDT Customize IP dialog box includes the following options:

- **Width of Watchdog Timer** – This indicates exponent for setting the length of the WDT interval. WDT interval = $2^{C\_WDT\_INTERVAL} \times T_{clk}$. Values for this selection can be in range from 8 to 31. Default values is 30.
- **WDT Enable behavior** – Enable only once = WDT can be enabled only once after reset, cannot disable it. Enable Repeatedly = WDT can be enabled/disabled by software. Default value is "Enable only once."

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 2].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This section contains information about simulating IP in the Vivado Design Suite. For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6].

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 2].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

The top module instantiates all components of the core and example design that are needed to implement the design in hardware, as shown in Figure 5-1. This includes the clock generator (MMCME2), register configuration, data generator, and data checker modules.

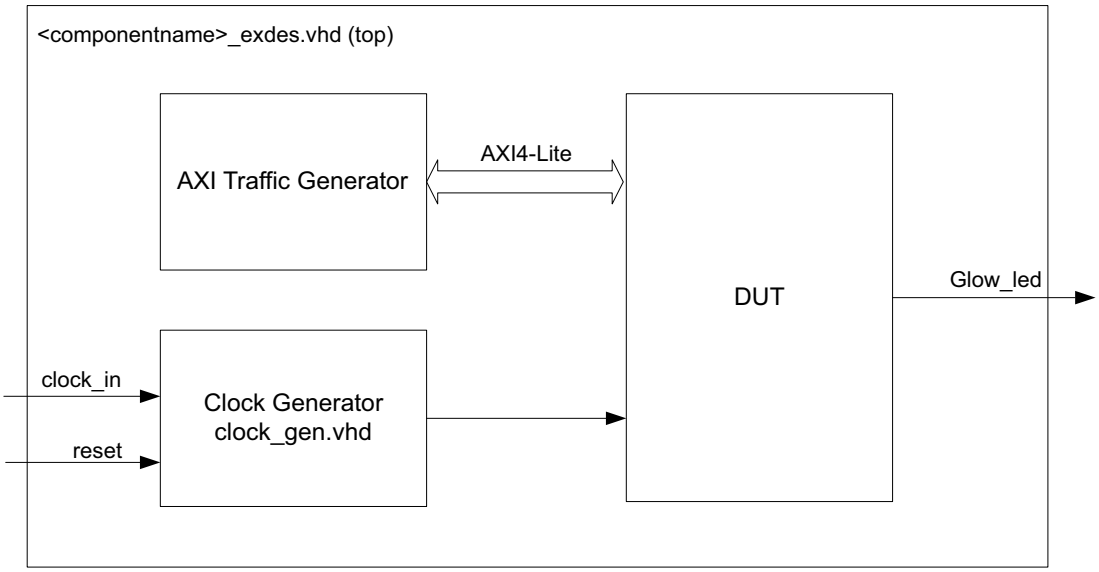

Figure 5-1: **AXI Timebase WDT Example Design Block Diagram**

- **Clock Generator** – MMCME2 generates the clocks for the example design. MMCME2 generates 100 MHz clock for `s_axi_aclk`. DUT and other modules of the example design are kept under reset until MMCME2 is locked.
- **AXI Traffic Generator (ATG)** – This module (IP) is configured in System Test Mode. All of the `AXI_TIMEBASE_WDT` related AXI4-Lite transactions are stored in the `coe/mif` file. For more information on AXI Traffic Generator, see *LogiCORE IP AXI Traffic Generator* (PG125) [Ref 8]. The ATG automatically starts the AXI4-Lite transaction after coming out of reset.

Implementing the Example Design

After following the steps described in Customizing and Generating the Core, page 16 to generate the core, implement the example design as follows:

1. Right-click the core in the Hierarchy window, and select **Open IP Example Design**.
2. A new window pops up, asking you to specify a directory for the example design. Select a new directory or keep the default directory.
3. A new project is automatically created in the selected directory and it is opened in a new Vivado window.
4. In the Flow Navigator (left-side pane), click **Run Implementation** and follow the directions.

ATG writes value "2" to x"00 register and this starts the WDT timer. When timer value has reached a certain count, `Glow_led` output drives to 1.

The `Glow_led` outputs of the WDT example design is connected to the `GPIO_LED_7` LED of the KC705 board for the example design status. On successful completion of ATG write transactions to WDT registers and counters initiation, the `GPIO_LED_7` LED of KC705 would glow. In case of a failure, the `GPIO_LED_7` LED of KC705 would not glow.

Example Design Directory Structure

In the current project directory, a new project with name `<component_name>_example` is created and the files are generated in `<component_name>_example/<component_name>_example.srcs/` directory. This directory and its subdirectories contain all the source files that are required to create the AXI Timebase WDT example design.

Table 5-1 shows the files delivered in this `<component_name>_example/<component_name>_example.srcs/sources_1/imports/example_design/` directory.

Table 5-1: **Example Design Directory**

Name	Description
<component_name>_exdes.vhd	Top-level HDL file for the example design.
clock_gen.vhd	Clock generation module for example design.
atg_addr.coe	COE file of address. This file contains the axi_timebase_wdt register address.
atg_data.coe	COE file of data. This file contains the data to be written/read from the axi_timebase_wdt registers.

Table 5-1: **Example Design Directory *(Cont'd)***

Name	Description
atg_mask.coe	COE file to mask certain reads.
atg_ctrl.coe	COE file that contains control information of ATG.

Table 5-2 shows the files delivered in this `<component_name>_example/<component_name>_example.srcs/sources_1/sim_1/imports/simulation/` directory.

Table 5-2: **Simulation Directory**

Name	Description
<component_name>_exdes_tb.vhd	Test bench for the example design.

Table 5-3 shows the files delivered in this `<component_name>_example/<component_name>_example.srcs/sources_1/constrs_1/imports/example_design/` directory.

Table 5-3: **Constraints Directory**

Name	Description
<component_name>_exdes.xdc	Top-level constraints file for the example design.

The XDC has all the necessary constraints needed to run the example design on the KC705 board. All I/O constraints are commented in the XDC file.

IMPORTANT: *Uncomment before implementing the design for KC705 board.*

Simulating the Example Design

Using the AXI Timebase WDT example design (delivered as part of the AXI Timebase WDT), you can quickly simulate and observe the behavior of the AXI Timebase WDT.

Setting Up the Simulation

The Xilinx® simulation libraries must be mapped into the simulator. If the libraries are not set for your environment, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6] for assistance compiling Xilinx simulation models and setting up the simulator environment. To switch simulators, click **Simulation Settings** in the Flow Navigator (left pane). In the Simulation options list, change **Target Simulator**.

Simulation Results

The simulation script compiles the AXI Timebase WDT example design and supporting simulation files. It then runs the simulation and checks to ensure that it completed successfully.

If the test passes, then the following message is displayed:

```
Test Completed Successfully
```

If the test fails or does not complete, then the following message is displayed:

```
Test Failed!! Test Timed Out.
```

Test Bench

This chapter contains information about the test bench provided in the Vivado® Design Suite.

Figure 6-1 shows the test bench for AXI Timebase WDT example design. The top-level test bench generates 200 MHz clock and drives initial reset to the example design.

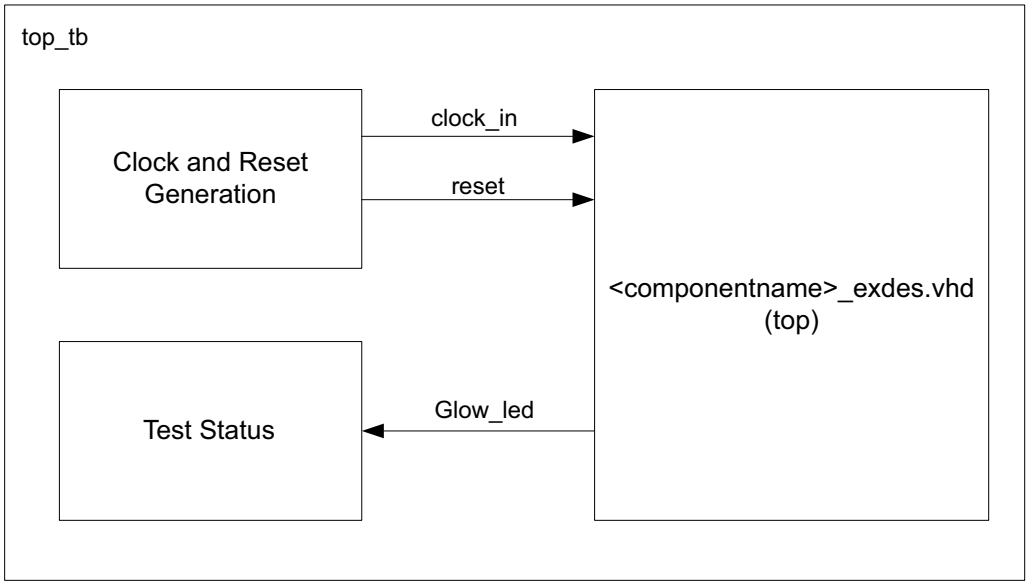

Figure 6-1: **AXI Timebase WDT Example Design Test Bench**

Migrating and Upgrading

This appendix contains information about migrating a design from ISE® to the Vivado® Design Suite, and for upgrading to a more recent version of the IP core. For customers upgrading in the Vivado Design Suite, important details (where applicable) about any port changes and other impact to user logic are included.

Migrating to the Vivado Design Suite

For information on migrating to the Vivado Design Suite, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 7].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when you upgrade to a more current version of this IP core in the Vivado Design Suite.

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the AXI Timebase WDT, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the AXI Timebase WDT. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the AXI Timebase WDT

AR: 54444

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address AXI Timebase WDT design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 9].

Interface Debug

AXI4-Lite Interfaces

Read from a register that does not have all 0s as a default to verify that the interface is functional. See Figure 3-1 for a read timing diagram. Output `s_axi_arready` asserts when the read address is valid, and output `s_axi_rvalid` asserts when the read data/response is valid. If the interface is unresponsive, ensure that the following conditions are met:

- The `s_axi_aclk` input is connected and toggling.
- The interface is not being held in reset, and `s_axi_aresetn` is an active-Low reset.
- The main core clocks are toggling and that the enables are also asserted.
- If the simulation has been run, verify in simulation and/or Vivado lab tools capture that the waveform is correct for accessing the AXI4-Lite interface.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *LogiCORE™ IP AXI4-Lite IPIF Product Guide* (PG155)
2. *Vivado® Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado AXI Reference Guide* (UG1037)
4. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994)
5. *Vivado Design Suite User Guide: Getting Started* (UG910)
6. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
7. *ISE® to Vivado Design Suite Migration Guide* (UG911)
8. *LogiCORE IP AXI Traffic Generator Product Guide* (PG125)
9. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
10. *ARM® AMBA® AXI4 Protocol Version: 2.0 Specification*
    http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/18/2015	2.0	Added support for UltraScale+ families.
04/02/2014	2.0	• Updated AXI Timebase Watchdog Timer Block Diagram. • Added PG155 reference in Overview section. • Updated 32-bit Timebase and WDT descriptions in Functional Description section. • Updated description in Timebase Operation section. • Updated Bit[0] description in Control/Status Register 0. • Updated descriptions in Clocking and Resets sections.
12/18/2013	2.0	Added UltraScale support.
10/02/2013	2.0	• Revision number advanced to 2.0 to align with core version number 2.0. • Added IP Integrator. • Updated Functional Description. • Updated Table 2-1 AXI Timebase Watchdog Timer System Performance. • Updated Performance and Resource Utilization sections. • Updated Table 2-7 Control/Status Register 0 Bit[3] description. • Updated Resets section. • Updated Timing Diagrams section. • Added Simulation, Synthesis, Example Design, and Test Bench chapters. • Updated Migrating Appendix.
03/20/2013	1.0	Initial Xilinx release of the product guide and replaces DS763. • Updated Table 2-1 AXI Timebase Watchdog Timer System Performance. • Updated Table 2-2 to 2-4 Resource Estimates. • Updated Table 2-5 AXI Timebase WDT I/O Signals.

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