AXI Thin Film Transistor Controller v2.0

LogiCORE IP Product Guide

Vivado Design Suite

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Introduction

The Xilinx® LogiCORE™ IP AXI Thin Film Transistor (TFT) controller is a hardware display controller IP core capable of displaying 256k colors. The AXI TFT Controller connects as a master on the AXI4 and reads the video pixel data from the attached video memory. This core also connects as a slave to the AXI4 bus for the register access. This core is capable of configuring Chrontel CH-7301 DVI Transmitter Chip through I2C interface.

Features

- Connects as master on the AXI4 bus of 32, 64, or 128 bits data width
- Connects as a slave on the AXI4-Lite bus
- Parameterizable TFT interface for 18-bit VGA or 24-bit DVI
- Supports 25 MHz TFT clock for display resolution of 640 × 480 pixels at 60Hz refresh rate
- Optionally supports configuration of external Chrontel DVI Transmitter Chip through the I2C interface
- Supports a separate clock domain for AXI4 interface and TFT interface
- Supports `VSYNC` Interrupt and Status

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[(1)]	UltraScale+™ Families, UltraScale™ Architecture, Zynq®-7000 All Programmable SoC, 7 Series
Supported User Interfaces	AXI4, AXI4-Lite
Resources	See Table 2-2 and Table 2-3.
Provided with Core	
Design Files	RTL
Example Design	Verilog and VHDL
Test Bench	Verilog
Constraints File	XDC
Simulation Model	Not Provided
Supported S/W Driver[(2)]	Standalone and Linux
Tested Design Flows[(3)]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

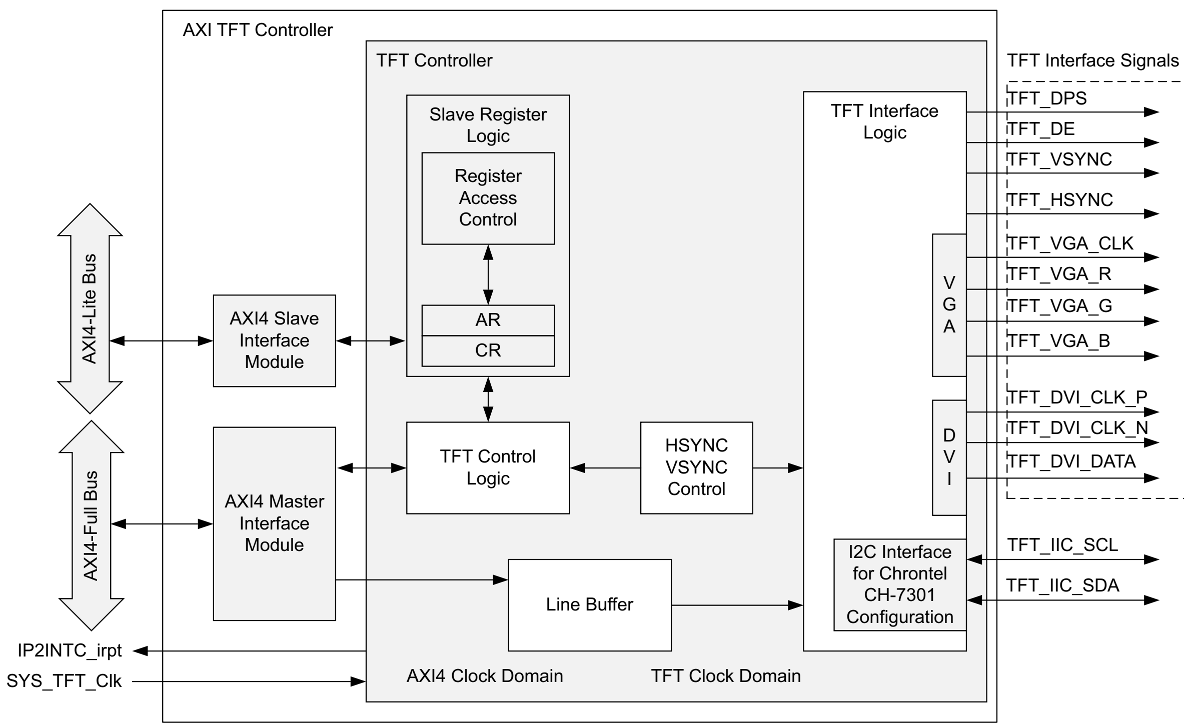
1. For a complete list of supported derivative devices, see the Vivado IP catalog.
2. Standalone driver details can be found in the SDK directory (<*install_directory*>/doc/usenglish/xilinx_drivers.htm). Linux OS and driver support information is available from the Xilinx Wiki page.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Functional Description

The AXI TFT Controller core IP is a hardware display controller for a 640 × 480 resolution display screen. This core is capable of displaying up to 256K colors through the VGA or DVI interface. The design contains an AXI4 master interface that reads video data from an attached memory device and displays the data onto the TFT screen. The design also contains an AXI4 slave interface for register access.

This controller also provides an I2C interface to configure the Chrontel CH-7301 video encoder chip when the DVI interface is selected. Figure 1-1 shows the AXI TFT Controller block diagram.



Notes:
1. DVI Interface is included in the design if the parameter TFT Interface = DVI.
2. VGA Interface is included in the design if the parameter TFT Interface = VGA.
3. I2C Interface logic is included in the design if Enable I2C Interface = 1.

Figure 1-1: **AXI TFT Controller Block Diagram**

The major modules of AXI TFT Controller are described in the following sections. These modules include:

- AXI4 Master Interface Module
- AXI4 Slave Interface Module
- Slave Register Logic
- TFT Control Logic
- Line Buffer
- HSYNC/VSYNC Control
- TFT Interface Logic

AXI4 Master Interface Module

The AXI4 Master Interface module provides a master interface between the AXI TFT Controller and the AXI4 bus. The AXI TFT Controller reads pixel data from an external AXI4 memory device through the AXI4 Master Interface module. The master interface supports 32, 64, and 128-bit data widths. Also, the interface supports 32-bit and 64-bit address widths.

AXI4 Slave Interface Module

The AXI4 Slave Interface module provides an interface between Slave register logic and AXI4-Lite bus. The AXI TFT Controller registers can be accessed through AXI4 using this interface. This module generates signals that are required for the AXI4-Lite interface and IPIF interface on the TFT side.

Slave Register Logic

The Slave Register Logic module consists of the Address register (AR), Control register (CR), and logic that provide the access to these registers using the AXI4 interface. The Address register allows you to change the base address of video memory to be read from. This allows video frames to be fetched from other memory locations without being seen on the display. You can change the video memory base address to display a different frame when it is ready. The Control register allows the display to be rotated by 180° or to be turned off by configuring the control bits.

TFT Control Logic

The TFT Control Logic module generates a read request to AXI4 Master Interface module to get pixel data from an external AXI4 memory device. This module synchronizes the signals crossing the different clock domains. The TFT control logic generates a master read request, address for the video memory, and reads the pixel data for each display line using a series of burst transactions. The pixel data is stored in an internal line buffer and then sent out to the TFT display with the necessary timing to correctly display the image. This process repeats continuously over every line and frame to be displayed on the 640 × 480 TFT screen.

Figure 1-2 shows the data flow diagram from the AXI4 clock domain to the TFT clock domain. The display is turned off by clearing the display enable bit in the Control register. The TFT controller then issues a reset to all the counters. It stops requesting data from the video memory by applying reset to the Master Interface module. In the reset state, the controller sets the `HSYNC` and `VSYNC` to their default value (see Table 2-4, page 13) causing the display to enter in sleep mode.

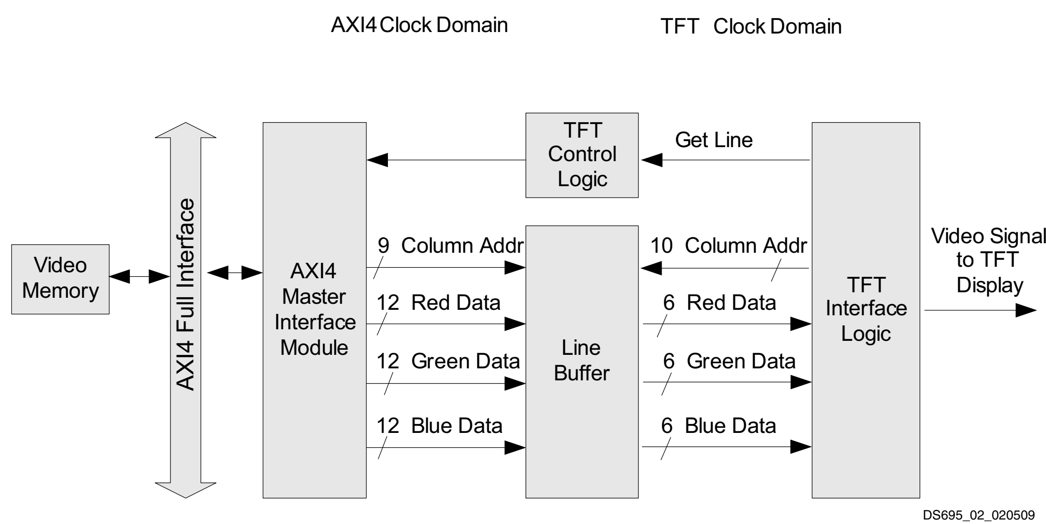


Figure 1-2: **Data Flow Diagram**

Line Buffer

The AXI TFT Controller allows the AXI4 clock and TFT video clock to be asynchronous to each other. The line buffer module includes synchronization logic to allow the passing of control signals between asynchronous AXI4 and TFT clock domains. This module consists of a 640 × 18-bit asynchronous FIFO which is used as the line buffer to pass video data between the two clock domains. Out of the 64-bit AXI4 data, the 36-bit of RGB data is written to the asynchronous FIFO.

HSYNC/VSYNC Control

This module generates the timing necessary for the video synchronization signals including back porch and front porch timing for HSYNC and VSYNC. For more information, see Chapter 3, Video Timing.

TFT Interface Logic

The TFT interface logic driving the TFT display operates in the same clock domain as the video clock. It reads out the pixel data from the dual port line buffer and transmits it to the TFT. This module consists of logic to transmit the pixel data in either VGA or DVI format based on the parameter TFT Interface and the logic to configure the Chrontel CH-7301 video encoder chip. The HSYNC, VSYNC, and DE signals are common for both the interfaces. The VGA, DVI, and Chrontel I2C interfaces are described in the following sections.

VGA Interface

The VGA interface logic is included in the design if the parameter TFT Interface is set to VGA. The 18-bit RGB pixel data is transmitted to the VGA ports and logic 0 is transmitted to all DVI ports.

DVI Interface

The DVI interface logic is included in the design if the parameter TFT Interface is set to DVI. The 18-bit RGB data is converted into 24-bit pixel data by padding zeroes in between the RGB data. This 24-bit pixel data is transmitted to the 12-bit DVI data port by clocking the data on both edges using the double data rate registers shown in Figure 1-3. The 18-bit RGB pixel data translation to 24-bit DVI data is shown in Table 1-1.

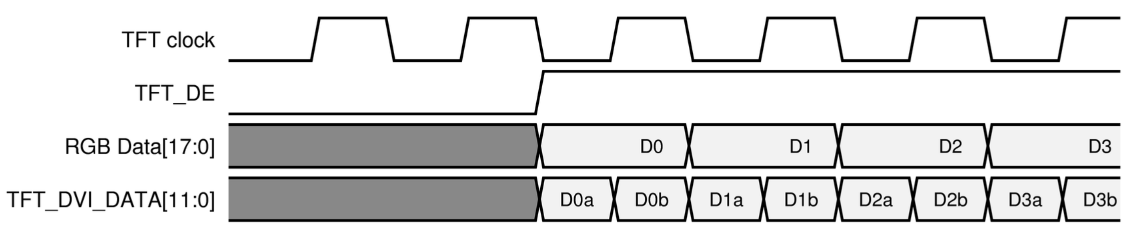


Figure 1-3: **RGB to DVI Data**

Table 1-1: **RGB to DVI Data Conversion**

DVI Data	Data A	Data B
TFT_DVI_DATA[0]	0	G[2]
TFT_DVI_DATA[1]	0	G[3]
TFT_DVI_DATA[2]	B[0]	G[4]
TFT_DVI_DATA[3]	B[1]	G[5]

Table 1-1: **RGB to DVI Data Conversion *(Cont'd)***

DVI Data	Data A	Data B
TFT_DVI_DATA[4]	B[2]	0
TFT_DVI_DATA[5]	B[3]	0
TFT_DVI_DATA[6]	B[4]	R[0]
TFT_DVI_DATA[7]	B[5]	R[1]
TFT_DVI_DATA[8]	0	R[2]
TFT_DVI_DATA[9]	0	R[3]
TFT_DVI_DATA[10]	G[0]	R[4]
TFT_DVI_DATA[11]	G[1]	R[5]

Chrontel I2C Interface

The Chrontel I2C interface logic is included in the design if the parameter Enable I2C interface is set to 1 and the TFT interface is set to DVI. This module consists of logic to configure the Chrontel CH-7301 video encoder chip. The configuration sequence logic is hard coded in this module and the data is sent over the I2C interface. This core configures only the basic registers of the CH-7301 chip for the DVI interface. The AXI TFT Controller remains in the reset state until the controller completes configuration of the Chrontel chip.

The description of these register addresses and the configuration data is shown in Table 1-2. If you want a different configuration for the Chrontel chip, you can configure the device using the Chrontel Chip Configuration register (CCR). For more information on the Chrontel DVI transmitter, see the *Chrontel CH-7301 DVI Transmitter Device Specification*.

Table 1-2: **Chrontel CH-7301 Configuration Register Descriptions**

Register Address	Register Name	Configuration Data	Access	Description
0x49	PM	0xC0	Write	Power Management Register
0x21	DC	0x09	Write	DAC Control Register
0x33	TPCP	0x08	Write	PLL Charge Pump Control Register
0x34	TPD	0x16	Write	PLL Divider Register
0x36	TPF	0x60	Write	PLL Filter Register

Applications

This core is used for VGA or DVI LCD panel applications. This core supports 640 × 480 resolution display screen.

Unsupported Features

The AXI TFT Controller is configured to the Chrontel CH-7301 chip only. If the system has a video encoder chip other than Chrontel CH-7301, you are responsible for chip configuration as needed.

Licensing and Ordering Information

This Xilinx® LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite tool under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards

The AXI TFT Controller IP core is AXI4 and AXI4-Lite compliant.

Performance

The AXI TFT is characterized as per the benchmarking methodology described in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 1]. Table 2-1 shows the results of the characterization runs for 7 series devices.

Note: Maximum frequencies for UltraScale™ and Zynq®-7000 devices are expected to be similar to Kintex®-7 and Artix®-7 device numbers.

Table 2-1: **Maximum Frequencies**

Family	Speed Grade	F_{Max} (MHz)		
		AXI4	AXI4-Stream	AXI4-Lite
Virtex-7	–1	200	200	180
Kintex-7		200	200	180
Artix-7		150	150	120
Virtex-7	–2	240	240	200
Kintex-7		240	240	200
Artix-7		180	180	140
Virtex-7	–3	280	280	220
Kintex-7		280	280	220
Artix-7		200	200	160

Resource Utilization

Note: UltraScale architecture results are expected to be similar to 7 series device results.

Virtex-7 FPGAs

Table 2-2 provides approximate resource counts for the various core options using Virtex®-7 FPGAs.

Table 2-2: **Device Utilization – Virtex-7 FPGAs**

Parameter Values		Device Resources		
AXI Data Width	**TFT Interfaces**	**Slices**	**Slice Flip-Flops**	**LUTs**
32	VGA	295	699	476
32	DVI	314	763	547
64	VGA	271	718	499
64	DVI	287	782	571
128	VGA	261	719	536
128	DVI	305	783	608

Kintex-7, Artix-7, and Zynq-7000 Devices

Table 2-3 provides approximate resource counts for the various core options using Kintex-7, Artix-7, and Zynq-7000 devices.

Table 2-3: **Device Utilization – Kintex-7, Artix-7, and Zynq-7000 Devices**

Parameter Values		Device Resources		
AXI Data Width	**TFT Interfaces**	**Slices**	**Slice Flip-Flops**	**LUTs**
32	VGA	260	699	728
32	DVI	290	763	843
64	VGA	260	718	751
64	DVI	304	782	872
128	VGA	255	719	759
128	DVI	307	783	864

Port Descriptions

The AXI TFT Controller I/O signals are described in Table 2-4.

Table 2-4: **AXI TFT Controller I/O Signal Description**

Signal Name	Interface	I/O	Initial State	Description
System Signals				
s_axi_aclk	Clock	I	–	AXI clock
s_axi_aresetn	Reset	I	–	AXI reset. Active-Low.
m_axi_aclk	Clock	I	–	AXI4 Master Clock
m_axi_aresetn	Reset	I	–	AXI4 Master Reset
md_error	System	O	0	Master Error Detection Indicator (Active-High)
ip2intc_irpt	Interrupt	O	0	VSYNC Pulse Interrupt
AXI4 Master Interface Signals				
m_axi_*	M_AXI	–	–	AXI4-Lite Slave Interface signals. See Appendix A of the *Vivado AXI Reference Guide* (UG1037) [Ref 2] for AXI4, AXI4-Lite and AXI Stream Signals.
AXI4 Slave Interface Signals				
s_axi_*	S_AXI	–	–	AXI4-Lite Slave Interface signals. See Appendix A of the *Vivado AXI Reference Guide* (UG1037) [Ref 2] for AXI4, AXI4-Lite and AXI Stream Signals.
TFT Interface Signals				
sys_tft_clk	TFT	I	–	TFT Clock Input
tft_hsync	TFT	O	1	Horizontal Sync (Active-Low)
tft_vsync	TFT	O	1	Vertical Sync (Active-Low)
tft_de	TFT	O	0	Data Enable
tft_dps	TFT	O	0	TFT Display Scan
tft_vga_clk	TFT-VGA	O	0	TFT VGA Clock(1)
tft_vga_r[5:0]	TFT-VGA	O	0	TFT VGA Red Pixel Data(1)
tft_vga_g[5:0]	TFT-VGA	O	0	TFT VGA Green Pixel Data(1)
tft_vga_b[5:0]	TFT-VGA	O	0	TFT VGA Blue Pixel Data(1)
tft_dvi_clk_p	TFT-DVI	O	0	Differential TFT DVI Clock(2)
tft_dvi_clk_n	TFT-DVI	O	0	Differential TFT DVI Clock(2)
tft_dvi_data[11:0]	TFT-DVI	O	0	TFT DVI Data(2)
tft_iic_scl_o	I2C	O	0	I2C Output Clock to Chrontel Chip(3)
tft_iic_scl_i	I2C	I	–	I2C input Clock from Chrontel Chip(3)
tft_iic_scl_t	I2C	O	1	3-State Control for I2C Clock(3)

Table 2-4: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Signal Name	Interface	I/O	Initial State	Description
tft_iic_sda_o	I2C	O	0	I2C Output Data to Chrontel Chip[3]
tft_iic_sda_i	I2C	I	–	I2C Input Data from Chrontel Chip[3]
tft_iic_sda_t	I2C	O	1	3-State Control for I2C Data[3]

Notes:

1. VGA interface signals.
2. DVI interface signals.
3. I2C signals are used to configure Chrontel Video Encoder chip. These ports are active when the DVI interface is selected and Enable I2C interface is set to 1.

Register Space

There are four internal registers available in the AXI TFT Controller. The internal registers of the AXI TFT Controller are at a fixed offset from the base address on a 32-bit boundary. Writing into the reserved register bits has no effect. Reading from the reserved registers returns 0.

All registers are defined for 32-bit access only. Any partial word write access (byte, half-word) has no effect on the registers and any partial word read access (byte, half-word) returns 0. All partial access to the core register returns bus error. The AXI TFT Controller internal registers and their offsets are listed in Table 2-5. The BASEADDR and HIGHADDR values for the IP are defined by the Vivado tool address mapping.

IMPORTANT: *The BASEADDR and HIGHADDR are not parameters.*

Table 2-5: **AXI TFT Controller Internal Register Map**

Address Offset	Register Name	Description
00h	AR	TFT Address register which specifies the base address of the video memory from which the controller fetches the data.
04h	CR	TFT Control Register
08h	IESR	VSYNC Interrupt Enable and Status Register
0Ch	CCR	Chrontel Configuration Register
10h[1]	AR	TFT Address register which specifies lower 32 bits of base address of the video memory from which the controller fetches the data.
14h[1]	AR	TFT Address register which specifies higher 32 bits of base address of the video memory from which the controller fetches the data.

Notes:

1. Applicable only when more than 32-bit address configuration is selected.

Address Register (AR)

The TFT Base Address register specifies the upper 11 bits of the base address of the video memory. This is the address of the AXI4 accessible memory device that acts as a video memory. This address must be aligned on a 2 MB boundary (that is, only the upper 11 bits are writable, the remaining address bits are always 0) as shown in Figure 2-1 and described in Table 2-6.

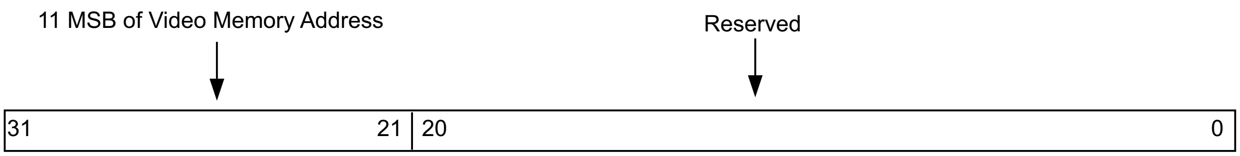


Figure 2-1: **Address Register**

Table 2-6: **Address Register Description**

Bits	Name	Reset Value	Access Type	Description
31:21	TFT Base Address	Default TFT Base Address Parameter from Vivado IDE	R/W	Specifies the base address of the video memory from which the controller fetches the data.
20:0	Reserved	N/A	N/A	Reserved

Control Register (CR)

The TFT Control register contains the control bits to configure the controller for TFT scanning mode and TFT display on/off. Writing a 0 in the TFT display enable bit resets the TFT controller. In the reset state, the controller stops requesting data from the video memory by applying a reset to the Master Interface module and sets the `HSYNC` and `VSYNC` to their default value causing the display to enter in sleep mode. The bit assignment in the TFT Control register is shown in Figure 2-2 and described in Table 2-7.

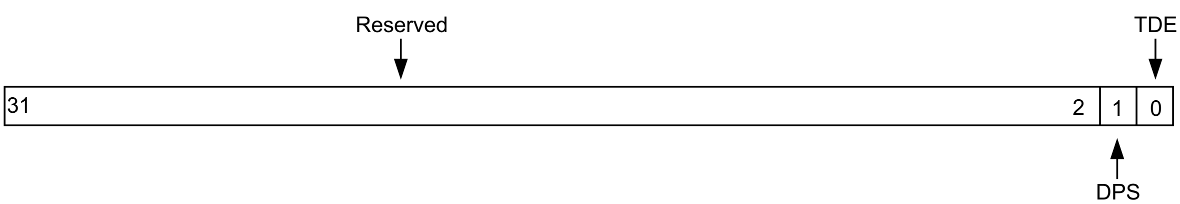


Figure 2-2: **Control Register**

Table 2-7: **Control Register Description**

Bits	Name	Reset Value	Access Type	Description
31:2	Reserved	N/A	N/A	Reserved
1	DPS	0	R/W	Display Scan Control Bit 0 = Set DPS output bit to 0. This sets the display to use normal scan direction. 1 = Set DPS output bit to 1. This sets the display to use reverse scan direction (rotates screen 180°).
0	TDE	1	R/W	TFT Display Enable Bit 0 = Disable TFT display. This resets the TFT controller and stops VSYNC/HSYNC signals causing the display to go in sleep mode. 1 = Enable TFT display. This causes the TFT controller to operate normally.

Interrupt Enable and Status Register (IESR)

The TFT Interrupt Enable and Status register is a 32-bit read/write register. This register contains the `VSYNC` interrupt enable bit and the status bit. If the `VSYNC` interrupt is enabled, the core generates an interrupt for the `VSYNC` pulse of every frame. For every rising edge of the `VSYNC` pulse, the core sets status bit to indicate that the core has displayed the current frame completely and accepted the new address from the AR. This status bit gets cleared for every write access to the AR. The bit assignment in the IESR is shown in Figure 2-3 and described in Table 2-8.

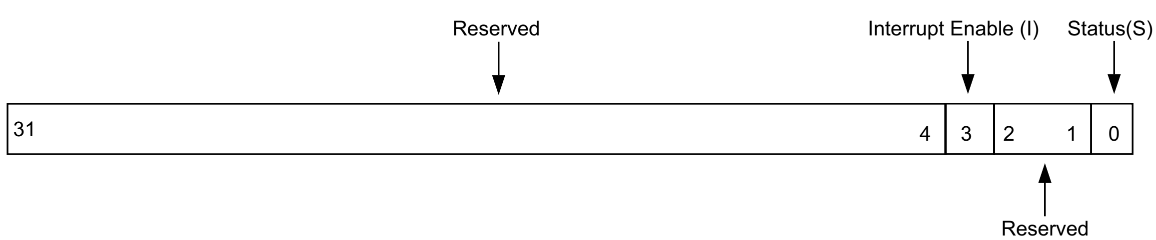


Figure 2-3: **Interrupt Enable and Status Register**

Table 2-8: **Interrupt Enable and Status Register Description**

Bits	Name	Reset Value	Access Type	Description
31:4	Reserved	N/A	N/A	Reserved
3	Interrupt Enable	0	R/W	VSYNC Interrupt Enable 0 = Disable VSYNC pulse interrupt 1 = Enable VSYNC pulse interrupt

Table 2-8: **Interrupt Enable and Status Register Description *(Cont'd)***

Bits	Name	Reset Value	Access Type	Description
2:1	Reserved	N/A	N/A	Reserved
0	Status	0	R/W	VSYNC and Address Latch Status Bit 0 = Core is displaying current frame. 1 = VSYNC pulse is active. Also indicates that the previous frame is displayed completely and the core has accepted the new address from the AR.

Chrontel Chip Configuration Register (CCR)

The Chrontel Chip Configuration register is a 32-bit read/write register. This register contains the IIC transmission start bit, Chrontel chip register address and Chrontel chip register data. This register enables you to configure the Chrontel chip register on-the-fly. Setting Bit[31] of this register initiates the IIC transmission to the Chrontel chip. When you set this bit, you need to poll this bit to know the status of the current I2C transaction. This bit is cleared when the IIC transmission is complete. The bit assignment in the CCR is shown in Figure 2-4 and described in Table 2-9.

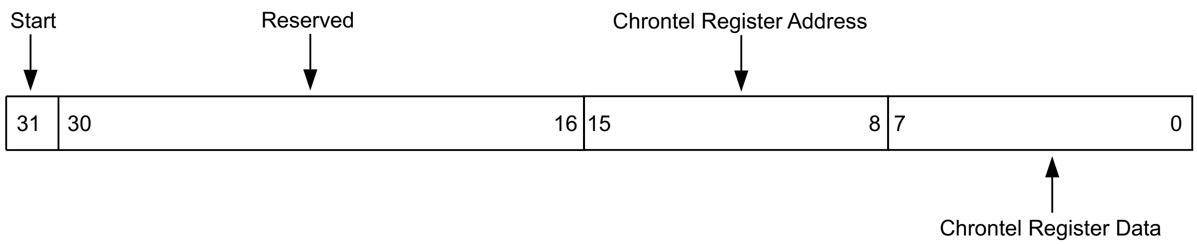


Figure 2-4: **Chrontel Chip Configuration Register**

Table 2-9: **Chrontel Chip Configuration Register Description**

Bits	Name	Reset Value	Access Type	Description
31	Start	0	R/W	Setting this bit starts IIC data transmission to the Chrontel chip.
30:16	Reserved	N/A	N/A	Reserved
15:8	ADDR	0	R/W	8-bit Chrontel Chip Register Address
7:0	DATA	0	R/W	8-bit Chrontel Chip Register Data

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Clocking

The AXI TFT Controller has three clock domains each for AXI slave interface, AXI master interface, and TFT clock domain. The following clocks are provided as input to the core.

- **s_axi_aclk** – Associates with the AXI4-Lite slave interface
- **m_axi_aclk** – Relates to the AXI4 master interface
- **sys_tft_clk** – Applies with the TFT side interface (that is, VGA or DVI)

The AXI slave or master clocks can be operated up to the maximum frequencies provided in Table 2-1. The TFT clock is a slow operating clock with a constant frequency of 25 MHz.

Resets

The AXI TFT Controller has two external reset signals each associated with the AXI slave and AXI master interface. The reset signal s_axi_aresetn is a synchronous reset input that resets the AXI slave interface and the register logic. The m_axi_aresetn signal is used to reset the AXI master interface, internal buffers, and TFT interface logic.

Protocol Description

Video Timing

The signal timings for a 640 × 480 display using a 25 MHz pixel clock are shown in Table 3-1. The AXI TFT Controller takes 16.8 ms to display each 640 × 480 display frame at 60Hz refresh rate on the TFT. To display the complete frame on the TFT, do not update the video memory start Address (AR) before this time frame.

Table 3-1: **640 × 480 Mode Display Timing**

Symbol	Parameter	Vertical Sync			Horizontal Sync	
		Time	Clocks	Lines	Time	Clocks
T_{PULSE}	Sync pulse time	16.8 ms	420,000	525	32 µs	800
T_{Disp}	Display time	15.4 ms	384,000	480	25.6 µs	640
T_{PW}	Pulse width time	64 µs	1,600	2	3.84 µs	96
T_{BP}	Back porch time	992 µs	24,800	31	1.92 µs	48
T_{FP}	Front porch time	384 µs	9,600	12	640 ns	16

HSYNC Timing

The `HSYNC` is an active-Low signal and the complete time period of the `HSYNC` is 800 TFT clocks. Out of the 800 TFT clock period, the active pixel data qualified by the active-High `DE` signal is 640 TFT clocks. The `HSYNC` pulse period is 96 TFT clocks. The time period between the `HSYNC` pulse and start of the active data is called a back porch which is 48 TFT clocks. The time period between the end of active data and start of the new `HSYNC` pulse is called a front porch which is 16 TFT clocks. The `HSYNC` timing with respect to the TFT clock is shown in Figure 3-1.

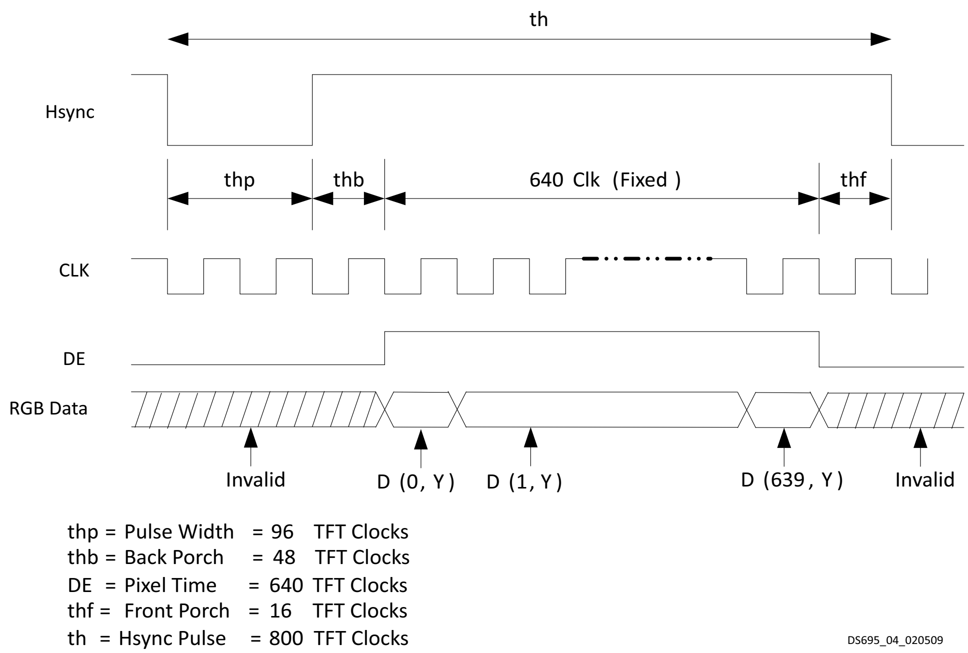


Figure 3-1: **Horizontal Data**

VSYNC Timing

The `VSYNC` is an active-Low signal and the complete time period of the `VSYNC` is 525 h_syncs. Out of the 525 h_syncs, the `VSYNC` pulse period is 2 h_syncs and the active display period is 480 h_syncs. The back porch period is 31 h_syncs and the front porch period is 12 h_syncs. The `VSYNC` timing with respect to the `HSYNC` is shown in Figure 3-2.

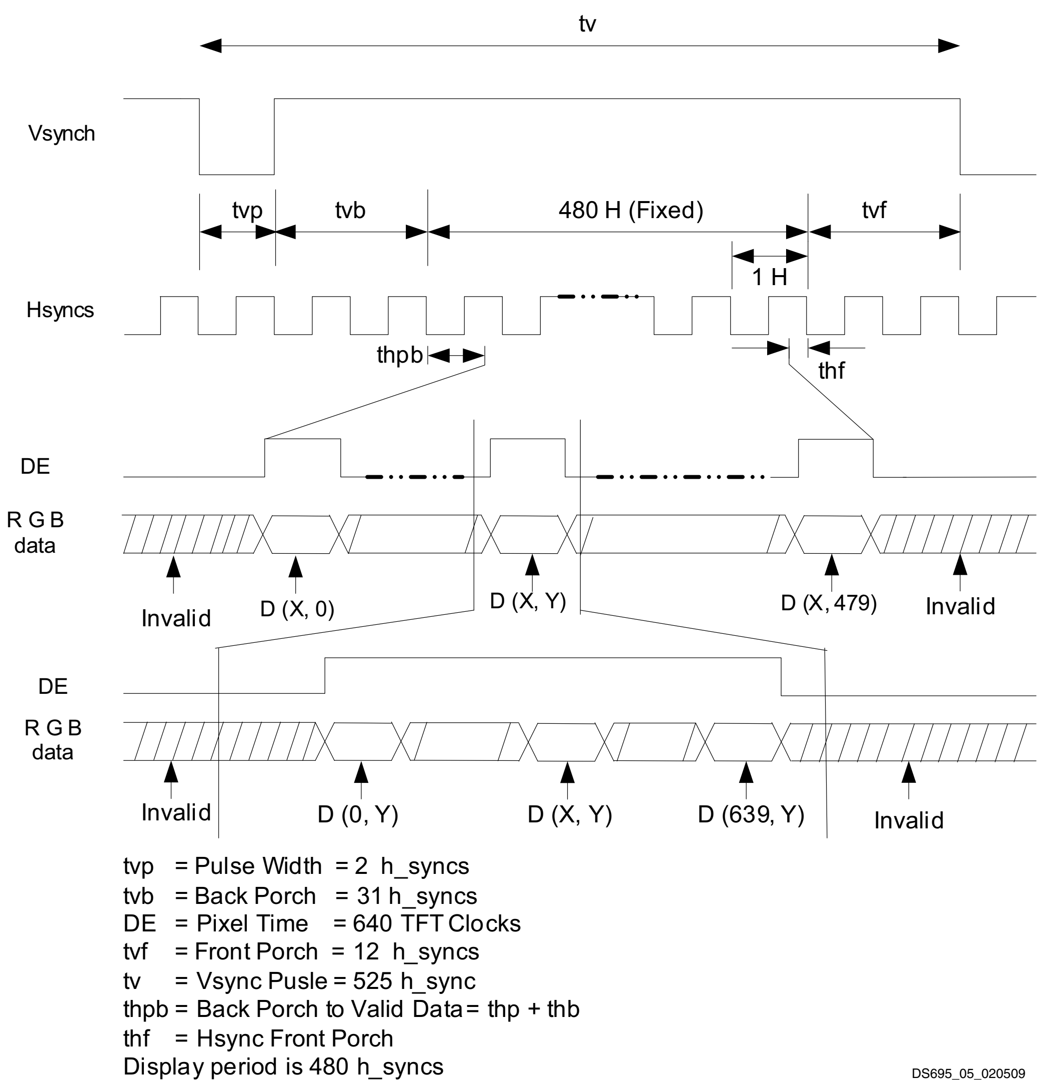


Figure 3-2: **Vertical Data**

Video Memory

IMPORTANT: *Design the system with sufficient bandwidth available between the AXI TFT Controller and the video memory device to meet the TFT video bandwidth requirements.*

There must be enough bandwidth made available for the rest of the system. If the system bandwidth requirement is increased, the TFT clock frequency can be reduced. However, reducing the TFT clock frequency also lowers the refresh rate of the screen. This can lead to a noticeable flicker on the screen if the TFT clock is too slow.

The AXI4 master interface logic can skip reading a line of data if it fails to finish reading data from a previous line because of shortage of AXI4 bandwidth. This prevents the AXI TFT Controller losing synchronization between the AXI4 and the TFT interface logic.

CAUTION! *Extreme shortage of available bandwidth for the AXI TFT Controller can cause the screen to appear unstable as stale lines of video data are displayed on the screen.*

The video memory is expected to be arranged such that each RGB pixel is represented by a 32-bit word in memory. The video memory should be stored in a 2 MB region of memory consisting of 1,024 data words (1 word = 32 bits) per line by 512 lines per frame. Out of this 1,024 × 512 memory space, only the first 640 columns and 480 rows are displayed on the screen.

For a given row (0 to 479) and column (0 to 639), the pixel color information is encoded as shown in Table 3-2.

Table 3-2: **Pixel Color Encoding**

<table>
<tr><th>Pixel Address</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="7">TFT Base Address + (4,096 × row) + (4 × column)</td><td>31:24</td><td>Undefined</td></tr>
<tr><td>23:18</td><td>Red Pixel Data:
000000 = darkest → 111111 = brightest</td></tr>
<tr><td>17:16</td><td>Undefined</td></tr>
<tr><td>15:10</td><td>Green Pixel Data:
000000 = darkest → 111111 = brightest</td></tr>
<tr><td>9:8</td><td>Undefined</td></tr>
<tr><td>7:2</td><td>Blue Pixel Data:
000000 = darkest → 111111 = brightest</td></tr>
<tr><td>1:0</td><td>Undefined</td></tr>
</table>

AXI TFT Controller Timing Diagrams

AXI TFT Master Burst Read on AXI4 Attached Memory

The AXI TFT burst read transaction on AXI4 is shown in Figure 3-3.

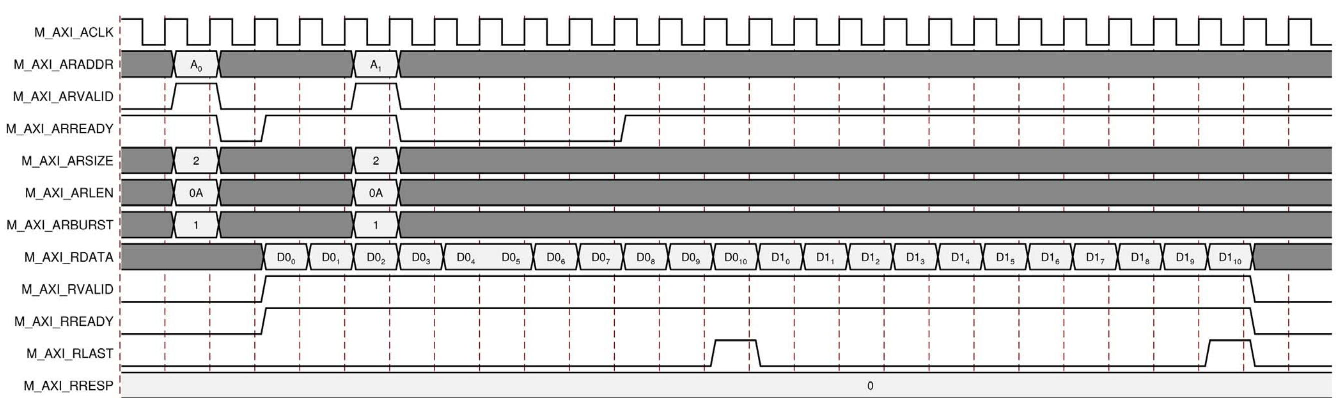


Figure 3-3: **AXI TFT Burst Read Transaction on AXI4 Master**

AXI TFT Register Read/Write through AXI4 Slave Interface

Figure 3-4 shows the AXI TFT Controller register access through AXI4 slave interface.

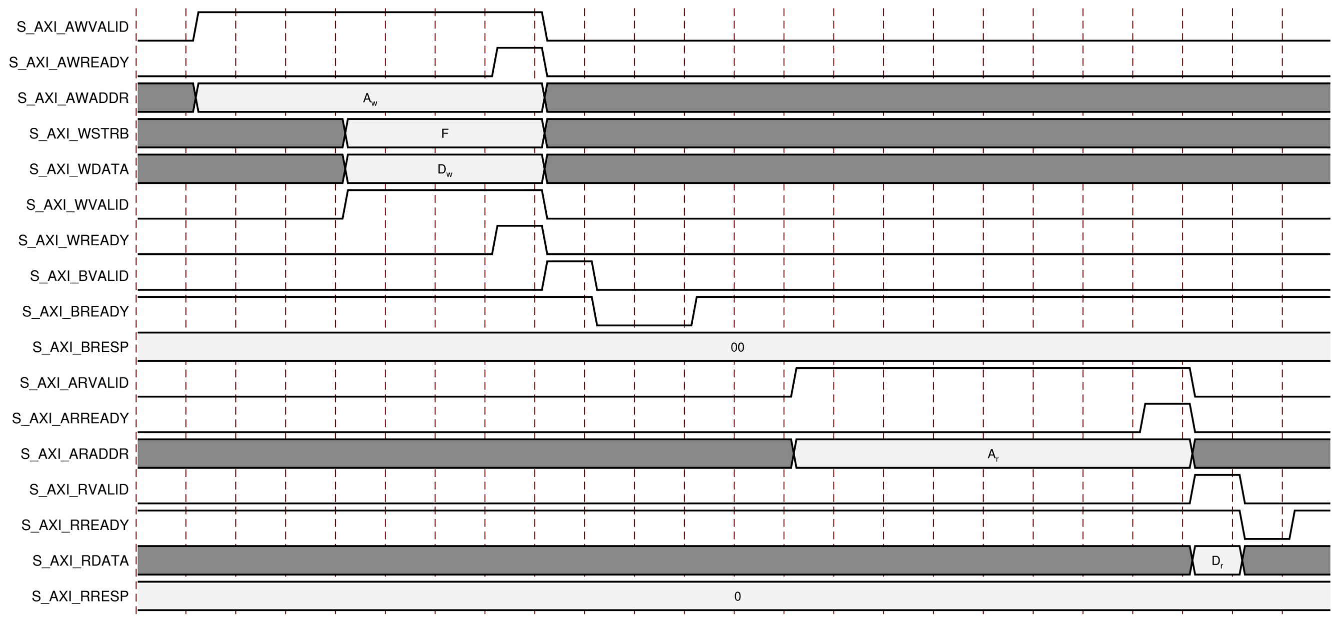


Figure 3-4: **AXI TFT Register Read/Write through AXI4 Slave Interface**

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 1]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5]

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 1] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4].

Note: Figures in this chapter are illustrations of the Vivado IDE. This layout might vary from the current version.

Figure 4-1 shows the AXI TFT Customize IP dialog box with information about customizing parameters.

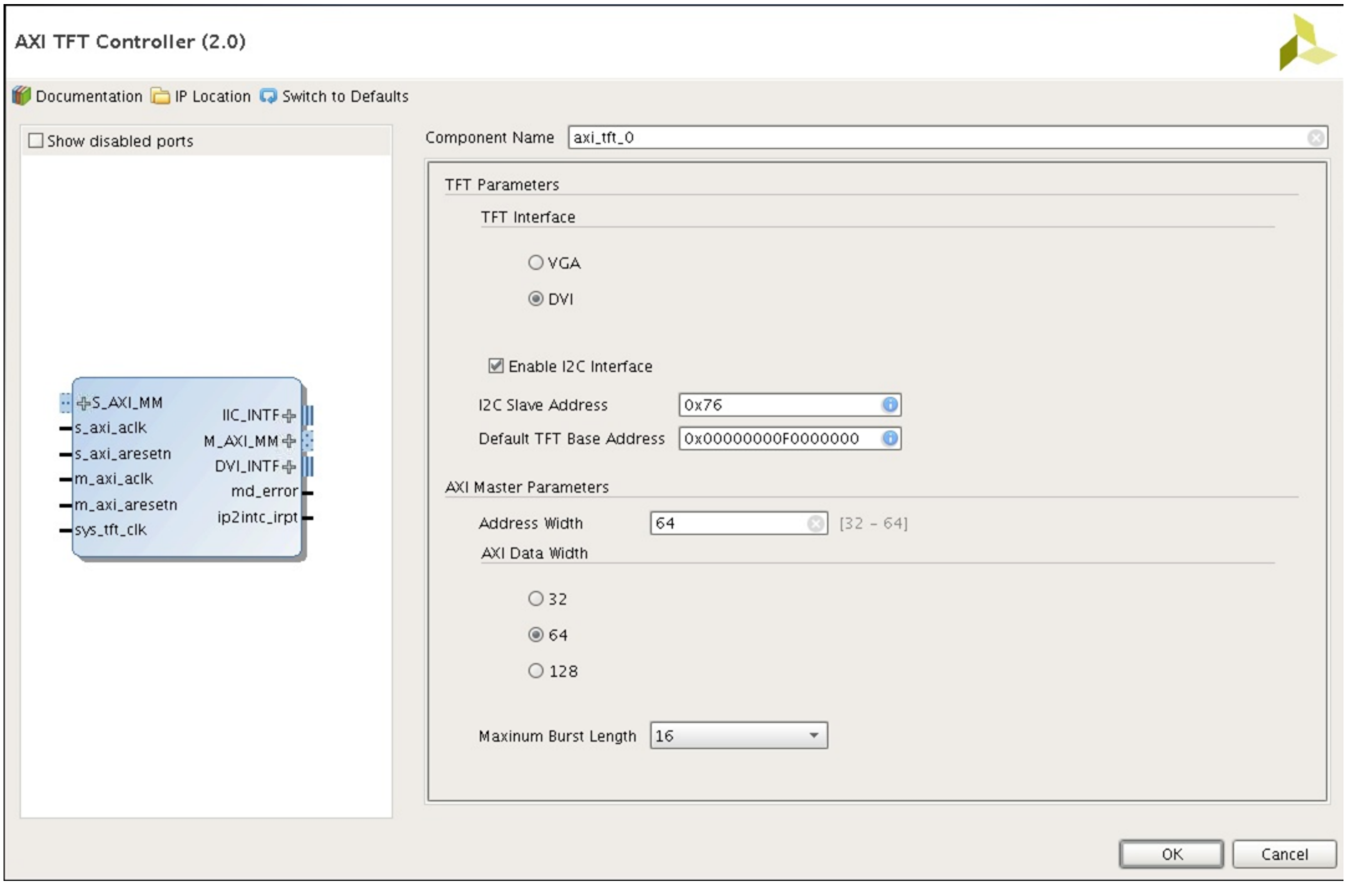


Figure 4-1: **Vivado Customize IP Dialog Box**

Figure 4-2 shows the AXI TFT Customize IP dialog box with IP integrator.

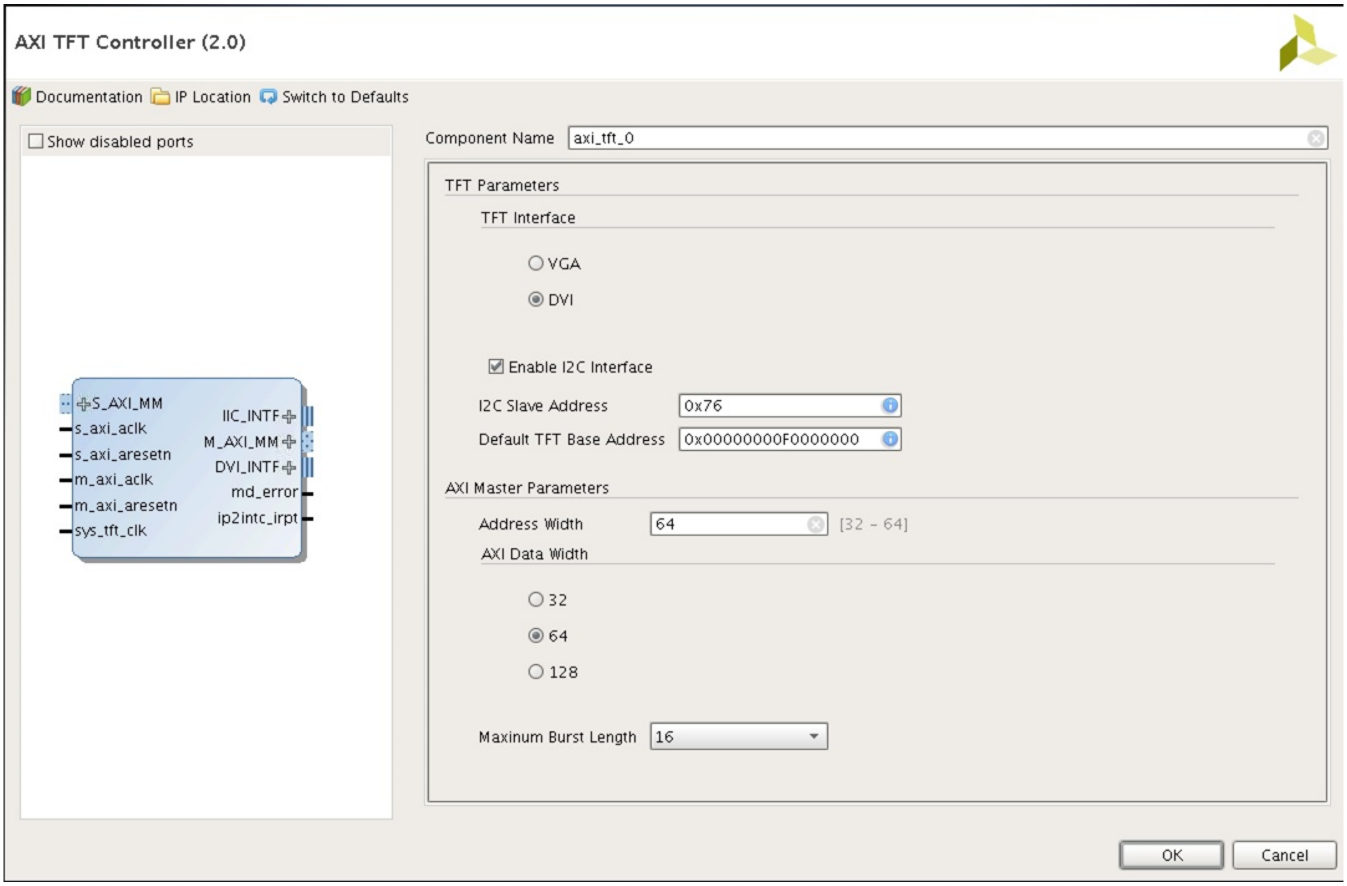


Figure 4-2: **Vivado IP Integrator Customize IP Dialog Box**

The Component Name field is the base name of the output files generated for the core. Names must begin with a letter and can be composed of any of the following characters: a to z, 0 to 9, and "_".

User Parameters

Table 4-1 shows the TFT and AXI Master Interface parameters.

Table 4-1: **AXI TFT Controller Parameter Descriptions**

Vivado IDE Parameter	Default Value	Allowed Values	Description
TFT Interface Parameters			
TFT Interface	DVI	VGA, DVI	Indicates the TFT interface supported.
Enable I2C Interface	1	0, 1	Enables I2C interface for Chrontel chip configuration. This parameter is valid only when DVI mode is selected.
I2C Slave Address	0x76	Any 7-bit hexadecimal value	Indicates the I2C slave address of the Video chip.

Table 4-1: **AXI TFT Controller Parameter Descriptions *(Cont'd)***

Vivado IDE Parameter	Default Value	Allowed Values	Description
Default TFT Base Address	0xF0000000	Address location in hexadecimal	Indicates the initial value of the address register. Lower 21 bits are not valid.
AXI Master Interface Parameters			
AXI Data Width	64	32, 64, 128	Data width of the AXI master interface.
Address Width	32	Integer values from 32 to 64	Indicates address width of AXI master interface.
Maximum Burst Length	16	16, 32, 64, 128, 256	Maximum burst length that can be issued by the AXI master interface.

Allowable Parameter Combinations

The address specified by C_DEFAULT_TFT_BASE_ADDR must be aligned on a 2 MB boundary. Only 11 MSB bits should have valid addresses, the remaining address bits must always be 0.

Optimal System Settings

RECOMMENDED: *Xilinx recommends having separate buses for the video memory access from the core and the rest of the system, to make sure sufficient bandwidth is available between the AXI TFT Controller and AXI4 memory device.*

The native data width of the AXI TFT Controller is fixed to 64 bits. Optimal performance is achieved when the video memory interface width is ≥ to native data width of AXI4 master interface.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 1].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

The IP generates the following false path constraints with respect to the clock domains. For IP level XDC commands, see the file in the project directory:

```
<project_name>.srcs/sources_1/ip/<instance_name>/
<instance_name>_clocks.xdc
```

All clock inputs need to be defined at the top-level in the system using `create_clock` command.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5].

IMPORTANT: *For cores targeting 7 series or Zynq-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.*

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 1].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

The top module instantiates all components of the core and example design that are needed to implement the design in hardware, as shown in Figure 5-1. This includes the clock and reset generation modules and AXI slave interface.

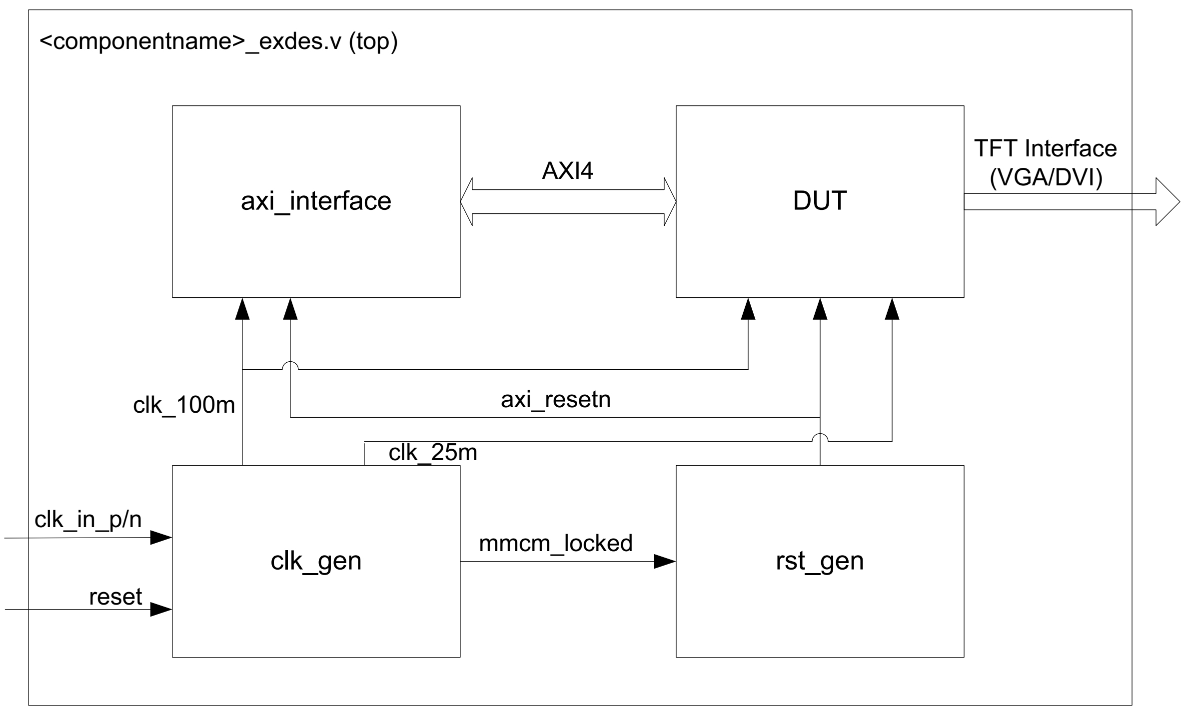


Figure 5-1: **AXI TFT Example Design Block Diagram**

This example design demonstrates the datapath of the DUT. After reset removal, DUT is in an enabled state by default and starts reading from the video memory from AXI master interface.

- **AXI Interface** – AXI interface implements the logic of the AXI-based video memory. After removal of reset, DUT triggers the burst transactions to read video data from the memory. AXI slave interface implements a counter to generate data. For each read transaction from the DUT, this block sends data depending on length and size signals provided by the DUT. The data sent includes red, green, and blue pixel values. The red, green, and blue pixel values are generated using a 6-bit counter.

- **DUT** – You generate and instantiate the AXI TFT controller instance as DUT. You select the DUT instance changes according to the parameters from the Vivado IDE.
- **clk_gen** – Clock generator module instantiates MMCM to generate 100 MHz clock and 25 MHz clock. The input frequency is 200 MHz differential clock from the board. 100 MHz clock is provided to the AXI slave interface logic and DUT as AXI clock. 25 MHz clock is provided to `sys_tft_clk` pin of the DUT.
- **rst_gen** – Reset generation logic uses locked signal from the MMCM to release the reset to the example design. The reset signal is generated synchronous to 100 MHz clock.

Implementing the Example Design

After following the steps described in Customizing and Generating the Core, page 24 to generate the core, implement the example design as follows:

1. Right-click the core in the Hierarchy window, and select **Open IP Example Design**.
2. A new window pops up, asking you to specify a directory for the example design. Select a new directory or keep the default directory.
3. A new project is automatically created in the selected directory and it is opened in a new Vivado window.
4. Provide the location constraints as per the board.
5. In the Flow Navigator (left-side pane), click **Run Implementation** and follow the directions.

To observe the results on the board, tap the pins assigned using logic analyzer and observe the red, green, and blue data signals incrementing by 1 for every valid clock cycle.

Example Design Directory Structure

In the current project directory, a new project with name `<component_name>_example` is created and the files are generated in `<component_name>_example.src/sources_1/imports/<component_name>/` directory. This directory and its subdirectories contain all the source files that are required to create the AXI TFT controller example design. They also include the reference design clocking module, reset module, example user design, and user constraints file.

```
<component_name>/example_design
```

This directory contains the generated example design top files. Table 5-1 shows the files delivered in this directory.

Table 5-1: **Example Design Directory**

Name	Description
axi_tft_example_top.xdc	Top-level constraints file for the example design.
<component_name>_exdes.v	Top-level HDL file for the AXI TFT controller example design.
axi_intf.v	AXI slave interface logic.
clk_gen.v	Clock generation modules.
tft_checker.v	TFT transaction checker logic.

Simulating the Example Design

Using the AXI TFT controller example design (delivered as part of the AXI TFT controller), you can quickly simulate and observe the behavior of the AXI TFT controller.

For more information on simulation, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5].

Setting Up the Simulation

The Xilinx® simulation libraries must be mapped into the simulator. If the libraries are not set for your environment, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5] for assistance compiling Xilinx simulation models and setting up the simulator environment. To switch simulators, click **Simulation Settings** in the Flow Navigator (left pane). In the Simulation options list, change **Target Simulator**.

Simulation Results

The simulation script compiles the AXI TFT example design and supporting simulation files. It then runs the simulation and checks to ensure that it completed successfully.

If the test fails due to data mismatch, the following error is displayed:

```
*****************************************************************
******************** ERROR: TEST FAILED ************************
********************** Data mismatch ***********************
*****************************************************************
```

If the test fails due to HSYNC/VSYNC timing mismatch, the following error is displayed:

```
*****************************************************************
******************** ERROR: TEST FAILED ************************
**************** HSYNC/VSYNC TIMING FAILED *********************
*****************************************************************
```

If no failures, the following error is displayed:

```
*****************************************************************
******************** INFO: TEST PASSED *************************
*****************************************************************
```

Test Bench

This chapter contains information about the test bench provided in the Vivado® Design Suite.

Figure 6-1 shows the test bench for the AXI TFT controller example design. The top-level test bench generates a top-level 200 MHz clock and drives initial reset to the example design.

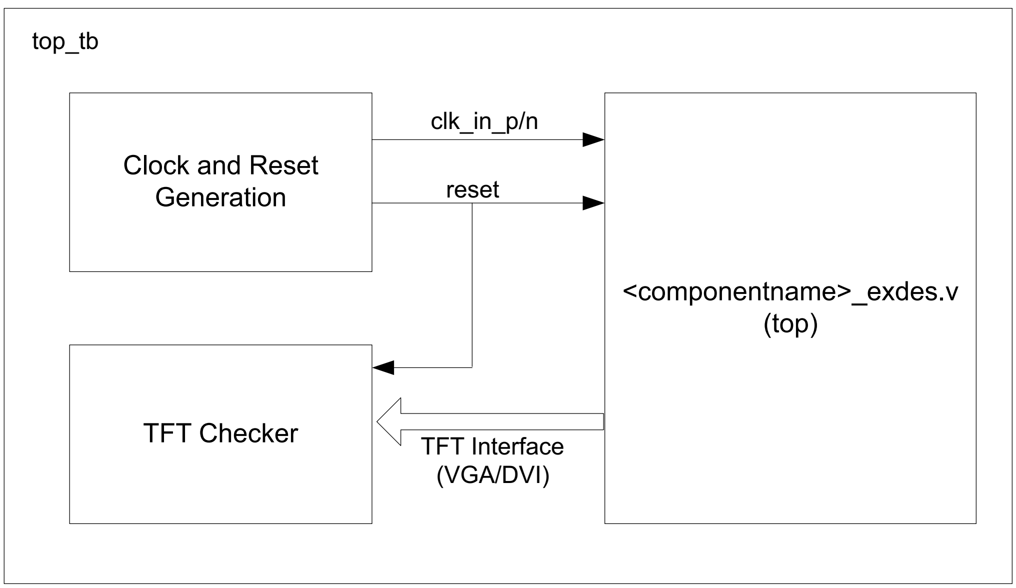


Figure 6-1: **AXI TFT Example Design Test Bench**

- **TFT Checker** – TFT checker logic implements logic to check the `HSYNC` and `VSYNC` timing and data integrity sent by the DUT, The `test_pass` signal indicates the status of the test with following values.

Table 6-1: **Status Signal Encoding**

Value	Description
00	Test passed.
01	Test failed with VSYNC/HSYNC timing.
10	Test failed with data mismatch.
11	Test failed with both timing and data mismatch.

Migrating and Upgrading

This appendix contains information about upgrading to a more recent version of the IP core.

Migrating to the Vivado Design Suite

For information on migrating to the Vivado Design Suite, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 6].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations between core versions.

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the AXI TFT Controller, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the AXI TFT Controller. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the AXI TFT Controller

AR: 54412

Known Issues

The IP supports AXI master data width of 32, 64, and 128. In 128-bit mode, master interface uses narrow burst transactions of 64 bits (that is, maximum bandwidth on AXI interface is not used in 128-bit mode).

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address AXI TFT Controller design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The Vivado Design Suite debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 7].

Hardware Debug

Hardware issues can range from initial bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado Design Suite debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the Vivado Design Suite debug feature for debugging the specific problems.

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation. The following are general checks.

1. Check if all the location constraints are given correctly.
2. Check if "I2C Slave Address" and "Default TFT Base Address" parameters are set properly.
3. Check if the internal registers are accessible from the processor.
4. If internal registers are accessible, AXI slave interface is working fine.
5. Check if the TDE bit in the Control register is set to enable transactions on VGA/DVI interface.
6. To debug further, you will need to add the Vivado Design Suite debug feature to monitor the AXI master interface.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *Vivado Design Suite User Guide: Designing with IP* (UG896)
2. *Vivado AXI Reference Guide* (UG1037)
3. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)
5. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
6. *ISE to Vivado Design Suite Migration Guide* (UG911)
7. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
8. *LogiCORE IP AXI4-Lite IPIF Product Guide* (PG155)
9. *LogiCORE IP AXI Master Burst Product Guide* (PG162)
10. *Chrontel CH-7301 DVI Transmitter Specification*, version 1.32
11. *I2C Bus Specification*, version 2.1
12. *ARM AMBA AXI Protocol v2.0 Specification* (ARM IHI 0022C)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/18/2015	2.0	Added support for UltraScale+ families.
09/30/2015	2.0	• Added 64-bit in AXI4 Master Interface Module section. • Added 0x10 and 0x14 to Table 2-5: AXI TFT Controller Internal Register Map. • Updated Figure 4-1: Vivado Customize IP Dialog Box. • Updated and added Address Width Table 4-1: AXI TFT Controller Parameter Descriptions.
04/02/2014	2.0	• Updated description in Features section of IP Facts. • Updated Supported S/W Driver in IP Facts table. • Updated description in AXI4 Master Interface Module section. • Updated burst description in TFT Control Logic section. • Added UltraScale support note in Performance section. • Updated system signal interface in I/O Port Description table. • Added link to I/O Port Description table in TFT Control Logic section. • Updated Bits[31:21] Reset Value description for Address register. • Updated I2C Slave Address bit to 7 in AXI TFT Controller Parameter Descriptions table. • Updated `s_axi_aclk` to AXI4-Lite in Clocking section.
12/18/2013	2.0	• Added UltraScale support. • Added Enable I2C interface in Overview and Product Specification chapter. • Updated figures and Enable I2C parameter in Customizing and Generating the Core chapter.
10/02/2013	2.0	• Added IP Integrator. • Updated Fig. 1-3. • Updated Table 2-1 Maximum Frequency table. • Updated Resource Utilization description section. • Added description to Chrontel Chip Configuration Register section. • Updated description in Clocking section. • Updated Required Constraints section. • Added Simulation, Synthesis, Example Design, and Test Bench chapters. • Updated Migrating Appendix. • Added Known Issues and Hardware Debug sections in Debug Appendix.

Date	Version	Revision
06/19/2013	2.0	• Revision number advanced to 2.0 to align with core version number. • Updated Fig. 1-1 AXI TFT Controller Block Diagram. • Added Performance section. • Updated Port Descriptions table. • Removed the Design Parameters table. • Updated Fig. 3-3 AXI TFT Burst Read Transaction on AXI4 Master • Updated Chapter 4 Customizing and Generating the Core section. • Updated Fig. 4-1 Vivado Customize IP Dialog Box. • Converted parameter list to Table 4-1. • Updated Master AR in Debug Appendix.
12/18/2012	1.0	Initial Xilinx release.

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