LogiCORE IP AXI Chip2Chip v1.00.a

Product Guide

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Introduction

The LogiCORE™ IP AXI Chip2Chip is a soft Xilinx IP core for use with the Xilinx® Embedded Development Kit (EDK). The adaptable block provides bridging between AXI systems for multi-FPGA System on Chip solutions. The core supports multiple FPGA-to-FPGA interfacing options and provides a low pin count, high performance AXI chip-to-chip bridging solution.

Features

- Supports AXI4 Memory Mapped user interface
- Supports SelectIO™ FPGA interface
- Supports Master and Slave modes
- Supports 32-to-64 bit AXI data width
- Supports asynchronous active-Low reset
- Supports Common Clock or Independent Clock operations
- Supports multiple Width Conversion options for reduced I/O utilization
- Supports Link Detect FSM with deskew operation
- Allows all five AXI channels to operate independently
- Supports an additional high-priority cut through channel for communicating interrupts
- Provides a dedicated high-priority internal channel for link status monitoring and reporting
- Generates Link Error and Multibit Error interrupts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000, Virtex®-7, Kintex™-7, Artix™-7
Supported User Interfaces	AXI4
Resources	See Table 2-2.
Provided with Core	
Design Files	Verilog and VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	User Constraints File
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	EDK 14.2 Xilinx Platform Studio (XPS)
Simulation	Mentor Graphics ModelSim
Synthesis	Xilinx Synthesis Technology (XST)
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see Embedded Edition Derivative Device Support.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The LogiCORE™ IP AXI Chip2Chip core functions like a bridge to seamlessly connect two FPGAs over an AXI interface. The core transparently bridges transactions in compliance with AXI protocol specifications. The bridging function allows all five channels to operate independently by forwarding per-channel data and control information in compliance with AXI per-channel Valid-Ready handshake.

Two instances of the AXI Chip2Chip core are required for performing the bridging function. Figure 1-1 provides block diagrams for both Master and Slave AXI Chip2Chip IP cores.

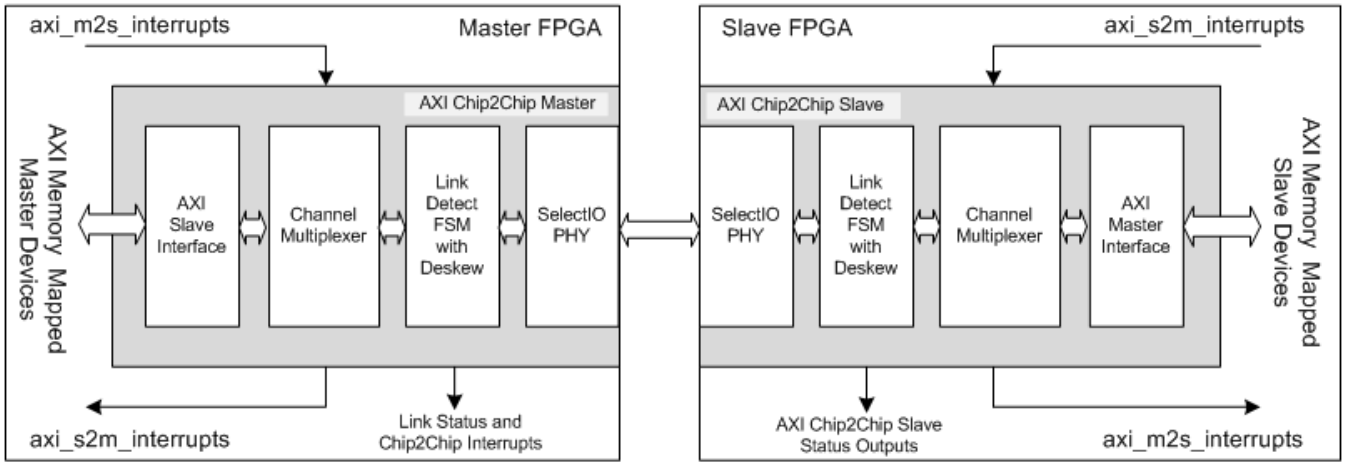

Figure 1-1: **AXI Chip2Chip Block Diagram**

The AXI Chip2Chip Master instance provides an AXI4 slave interface that can be directly connected to an AXI Master or AXI interconnect devices. The AXI Chip2Chip Slave instance provides an AXI4 Master interface that can be connected to an AXI Slave or AXI interconnect devices. The bridging functions in AXI Chip2Chip cores convert the wide on-chip AXI signaling to a compact FPGA-to-FPGA interfacing by utilizing a minimum set of FPGA I/Os. The AXI Chip2Chip bridging also implements functions that provide error-free communication over the FPGA I/Os.

AXI Chip2Chip operations can be categorized into four modules: AXI4 Interface, Channel Multiplexer, Link Detect FSM with Deskew, and PHY interface.

Feature Summary

This section summarizes the functionality of the four modules.

AXI4 Interface

The AXI Chip2Chip core provides an AXI4 interface to map to AXI Memory Mapped devices in the FPGA fabric. AXI Memory Mapped devices can be AXI Master, AXI interconnect, or AXI Slave functions. The AXI Interface can operate in either Common Clock or in Independent clock modes. For more details on clocking and latencies, see General Design Guidelines in Chapter 3.

Note: The AXI4 interface of the Chip2Chip core provides WUSER signals to maintain compatibility with AXI3 interface specifications. Any AXI3 master that supports write interleaving can use the AXI4 WUSER[3:0] signals to map the WID[3:0] signals in AXI3 Write Data channel.

Channel Multiplexer

The Channel Multiplexer multiplexes AXI Address and Data channels over FPGA I/Os. In addition, the AXI Chip2Chip core internally determines a 2:1 or 4:1 width conversion based on the Chip2Chip PHY Width option selected for the cores. Width conversion is used for reduced I/O utilization between the two FPGAs. For more details on width conversion, see Chip2Chip PHY Width in Chapter 4.

Link Detect FSM with Deskew

The Link Detect FSM with Deskew operation ensures that the AXI Chip2Chip Master core initiates transactions only when both Master and Slave cores are out of reset and deskew patterns are exchanged without any bit errors. Deskew operations align data until an optimized sampling point is determined for the data. The nibble level Deskew operation also enhances the maximum frequency of operation for the SelectIO™ interface.

SelectIO PHY Interface

The AXI Chip2Chip core provides the SelectIO interface as an interfacing option between the FPGAs. The SelectIO provides minimum latency between the FPGAs and provides SDR or DDR operations. When the SelectIO interface is used, the I/O type and I/O location must be specified in the User Constraints File (System UCF file).

Interrupt Signals

The AXI Chip2Chip core allows level interrupts to be communicated through a high-priority internal channel. Interrupts can be independently communicated between AXI Masters and AXI Slaves. On detecting a value change in the interrupt inputs, the AXI Chip2Chip Master

core initiates a high-priority transfer to update the interrupt outputs of the AXI Chip2Chip Slave core. Similarly, on detecting a value change in the interrupt inputs, the AXI Chip2Chip Slave core initiates a high-priority transfer to update the interrupt outputs of the AXI Chip2Chip Master core.

The AXI Chip2Chip Master core also generates interrupts for link error conditions. Interrupt signals are asserted by the AXI Chip2Chip Master core. For this, the error conditions detected in the AXI Chip2Chip Slave core are communicated to the Master FPGA through a high-priority internal channel.

The following interrupt signals are supported in the AXI Chip2Chip Master core:

- **Link Error Interrupt**: Asserted when the AXI Chip2Chip Slave core is reset during normal operation. For more details on Link Error Interrupt, see Resets in Chapter 3.
- **Multibit Error Interrupt**: When asserted, a Multibit Error interrupt indicates multiple bits are received in error in the Master or Slave AXI Chip2Chip core. For the SelectIO interface, a multibit error is determined during deskew operations and indicates deskew operation failure.

After being asserted, interrupt flags can be cleared only with a reset.

Applications

Figure 1-2 shows an example of the AXI Chip2Chip use case.

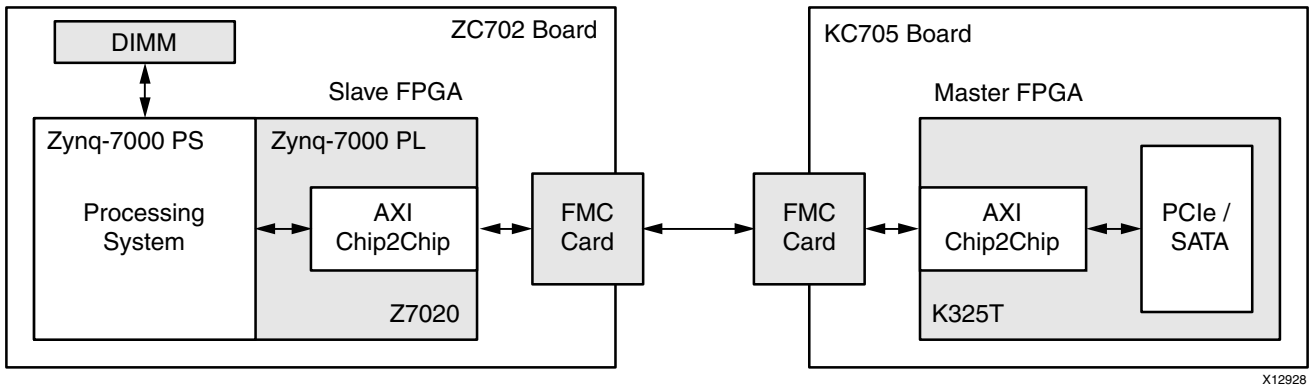

Figure 1-2: **AXI Chip2Chip Core Application Diagram**

In this use case, a Kintex™-7 device implementing a PCIe Master can send an AXI memory-mapped transaction to the DDR memory connected to the Zynq™-7020 device. The processing system in the Zynq-7020 device can be used to process the data written by the PCIe Master. The PCIe Master can then read back the processed data from the DDR memory connected to the Zynq-7020 device.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE® Design Suite Embedded Edition tools under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page.

For more information, visit the AXI Chip2Chip product page.

Product Specification

Standards Compliance

This core has bus interfaces that comply with the *ARM® AMBA® AXI4 Protocol Specification Version 1.0*.

Performance

Maximum Frequencies

The AXI Chip2Chip core operates up to 200 MHz on Artix-7 devices with -1 and higher speed grades.

Latency

Table 2-1 lists the latencies and performance measurements on the AXI4 interface of the Chip2Chip Master core. The measurements were taken with simultaneous read and write operations. The measurement setup issued up to four AXI4 outstanding transactions. The AXI (system) clock frequency in the setup was set to 100 MHz, and ALEN was set to 16 beats. The measured latency can have up to 5-10% variation and does not account for system latencies outside of the AXI Chip2Chip core.

Table 2-1: **Latency for AXI4 Interface of the AXI Chip2Chip Master Core**

Features			Latencies (AXI Clocks)		Performance (Mb/s)	
AXI Data Width	Number of I/Os	PHY Clock / PHY Type(1)(2)	AW_Valid to B_Valid	AR_Valid to R_Valid	Write Data Channel	Read Data Channel
32-bit	38	200 MHz / SDR	77	44	1190	1280
	32	150 MHz / DDR	69	47	1770	1920
	58	100 MHz / DDR	57	42	2350	2550

Table 2-1: **Latency for AXI4 Interface of the AXI Chip2Chip Master Core *(Cont'd)***

Features			Latencies (AXI Clocks)		Performance (Mb/s)	
AXI Data Width	Number of I/Os	PHY Clock / PHY Type[(1)(2)]	AW_Valid to B_Valid	AR_Valid to R_Valid	Write Data Channel	Read Data Channel
64-bit	28	150 MHz / DDR	95	59	1780	1920
	46	100 MHz / DDR	77	51	2370	2560

Notes:

1. Common Clock mode of operation was selected for configurations having the same PHY clock and AXI clock frequencies (100 MHz).
2. The number of I/Os is determined by the PHY Type and PHY Width configurations. See Table 4-1, page 25 for more details.

Resource Utilization

Table 2-2 shows the resource utilization numbers for the AXI Chip2Chip core for the Kintex™-7 family of FPGAs. These values have been generated using the Xilinx® EDK and ISE® tools for version 14.2. The values are derived from actual hardware validation systems.

Table 2-2: **Resource Utilization for the AXI Chip2Chip Core (Kintex-7 FPGAs)**

Features			AXI Chip2Chip Master Core			AXI Chip2Chip Slave Core		
AXI Data Width	Number of I/Os	Clocking	LUTs	FFs	Block RAMs	LUTs	FFs	Block RAMs
32-bit	38	Independent	1302	978	4	1314	881	4
	32	Independent	1408	1098	4	1390	996	4
	58	Common	1446	1241	4	1245	1097	4
64-bit	28	Independent	1482	1074	5	1497	974	5
	46	Common	1434	1144	5	1280	986	5

Notes:

1. Deskew operations for the AXI Chip2Chip core utilize 10 to 15% of LUTs and FF resources.

Port Descriptions

This section provides port descriptions for the AXI Chip2Chip core. It is organized according to Master and Slave ports.

AXI Chip2Chip Master

This section describes the ports when the AXI Chip2Chip core is a Master. It contains these subsections:

Global Signals

Table 2-3 describes the global signals for the AXI Chip2Chip Master core.

Table 2-3: **Global Interface Signals**

Name	Direction	Description
s_aclk	Input	Global Slave Interface Clock. For Independent Clock mode, all signals on the AXI Slave interface of an AXI Chip2Chip Master core are synchronous to `s_aclk`. For Common Clock mode, all AXI Chip2Chip Master core operations are synchronous to `s_aclk`.
axi_c2c_phy_clk	Input	Physical Interface Clock. The `axi_c2c_phy_clk` signal is applicable only when Independent Mode operation is selected for the core. AXI Chip2Chip Master core operations excluding the AXI Slave Interface are synchronous to `axi_c2c_phy_clk`.
idelay_ref_clk	Input	SelectIO Interface I/O Reference Clock. This signal is applicable only when the SelectIO interface is selected as the FPGA interfacing option and when deskew is enabled for the SelectIO interface. The applicable frequency for `idelay_ref_clk` is 200 MHz or 300 MHz (±10 MHz).
s_aresetn	Input	Global Reset. This active-Low signal can be asynchronous.

AXI Interface Signals

Table 2-4 describes the AXI Interface signals for the AXI Chip2Chip Master core.

Table 2-4: **AXI Interface Signals**

Name	Direction	Description
Write Address Channel		
s_axi_awid[C_AXI_ID_WIDTH-1:0]	Input	Write address ID. This signal is the identification tag for the write address group of signals. ID width can be configured from 1 to 6 bits.
s_axi_awaddr[31:0]	Input	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.

Table 2-4: **AXI Interface Signals *(Cont'd)***

Name	Direction	Description
s_axi_awlen[7:0]	Input	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
s_axi_awsize[1:0]	Input	Burst size. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
s_axi_awburst[1:0]	Input	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
s_axi_awvalid	Input	Write address valid. This signal indicates that valid write address and control information are available: 1 = address and control information available. 0 = address and control information not available. The address and control information remain stable until the address acknowledge signal, AWREADY, goes HIGH
s_axi_awready	Output	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.
Write Data Channel		
s_axi_wuser[C_AXI_WUSER_WIDTH-1:0]	Input	Write Data Channel User signals. The WUSER width can be configured from 1 to 4 bits.
s_axi_wdata[C_AXI_DATA_WIDTH-1:0]	Input	Write data. The write data bus can be 32 or 64 bits wide.
s_axi_wstrb[C_AXI_DATA_WIDTH/8-1:0]	Input	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for every eight bits of the write data bus. WSTRB[n] corresponds to WDATA[(8 × n) + 7:(8 × n)].
s_axi_wlast	Input	Write last. This signal indicates the last transfer in a write burst.
s_axi_wvalid	Input	Write valid. This signal indicates that valid write data and strobes are available: 1 = write data and strobes available. 0 = write data and strobes not available.
s_axi_wready	Output	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready. 0 = slave not ready.

Table 2-4: **AXI Interface Signals *(Cont'd)***

Name	Direction	Description
Write Response Channel		
s_axi_bid[C_AXI_ID_WIDTH-1:0]	Output	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding. ID width can be configured from 1 to 6 bits.
s_axi_bresp[1:0]	Output	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
s_axi_bvalid	Output	Write response valid. This signal indicates that a valid write response is available: 1 = write response available. 0 = write response not available.
s_axi_bready	Input	Response ready. This signal indicates that the Master can accept the response information. 1 = Master ready. 0 = Master not ready.
Read Address Channel		
s_axi_arid[C_AXI_ID_WIDTH-1:0]	Input	Read address ID. This signal is the identification tag for the read address group of signals. ID width can be configured from 1 to 6 bits.
s_axi_araddr[31:0]	Input	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided. The control signals that are issued with the address detail how the address is calculated for the remaining transfers in the burst.
s_axi_arlen[7:0]	Input	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
s_axi_arsize[1:0]	Input	Burst size. This signal indicates the size of each transfer in the burst.
s_axi_arburst[1:0]	Input	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
s_axi_arvalid	Input	Read address valid. When High, this signal indicates that the read address and control information is valid and remains stable until the address acknowledge signal, ARREADY, is High. 1 = address and control information valid. 0 = address and control information not valid.

Table 2-4: **AXI Interface Signals *(Cont'd)***

Name	Direction	Description
s_axi_arready	Output	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready. 0 = slave not ready.
Read Data Channel		
s_axi_rid[C_AXI_ID_WIDTH-1:0]	Output	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave. It must match the ARID value of the read transaction to which it is responding. ID width can be configured from 1 to 6 bits.
s_axi_rdata[C_AXI_DATA_WIDTH-1:0]	Output	Read data. The read data bus can be 32 or 64 bits wide.
s_axi_rresp[1:0]	Output	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
s_axi_rlast	Output	Read last. This signal indicates the last transfer in a read burst.
s_axi_rvalid	Output	Read valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = read data available. 0 = read data not available.
s_axi_rready	Input	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready. 0 = master not ready.
AXI Master to AXI Slave Interrupts		
axi_c2c_m2s_intr_in[3:0]	Input	Level Interrupt signaling from AXI Master to AXI Slave.
axi_c2c_s2m_intr_out[3:0]	Output	Level Interrupt signaling from AXI Slave to AXI Master.

Master FPGA Interface Signals

Table 2-5 describes the Master FPGA Interface signals for the AXI Chip2Chip Master core.

Table 2-5: **Master FPGA Interface Signals**

Name	Direction	Description
axi_c2c_selio_tx_clk_out	Output	SelectIO FPGA interface clock from Master FPGA to Slave FPGA.
axi_c2c_selio_tx_data_out[m-1:0]	Output	SelectIO FPGA Interface Data from Master FPGA to Slave FPGA. 'm' is the number of Output I/Os required for Master-to-Slave FPGA interfacing. For details, see Chip2Chip PHY Width in Chapter 4.
axi_c2c_selio_rx_clk_in	Input	SelectIO FPGA interface clock from Slave FPGA to Master FPGA.
axi_c2c_selio_rx_data_in[m-1:0]	Input	SelectIO FPGA interface signals from Slave FPGA to Master FPGA. 'm' is number of Input I/Os required for Slave to Master FPGA interfacing. For details, see Chip2Chip PHY Width in Chapter 4.

Interrupt and Status Signals

Table 2-6 describes the interrupt and status signals for the AXI Chip2Chip Master core.

Table 2-6: **Interrupt and Status Signals**

Name	Direction	Description
axi_c2c_link_status_out	Output	Link Status: Asserted when Link Detect FSM is in the SYNC state. Deasserted when either the Master or Slave AXI Chip2Chip core is under reset or when the Link Detect FSM is not in the SYNC state.
axi_c2c_link_error_out	Output	Link Error Interrupt: Asserted when the AXI Chip2Chip Slave core is reset during normal operations.
axi_c2c_multi_bit_error_out	Output	Multibit Error Interrupt: When asserted, this interrupt indicates multiple bits are received with errors in the Master or Slave AXI Chip2Chip core. For the SelectIO interface, a multibit error is determined during deskew operations and indicates failure of those operations.

AXI Chip2Chip Slave

This section describes the ports when the AXI Chip2Chip core is a Slave. It contains these subsections:

- Global Signals
- AXI4 Interface Signals
- Slave FPGA Interface Signals
- Status Signals

Global Signals

Table 2-7 describes the global signals for the AXI Chip2Chip Slave core.

Table 2-7: **Global Interface Signals**

Name	Direction	Description
m_aclk	Input	Global Master Interface Clock (Independent Clock). The `m_aclk` signal is an input when the Independent Clock mode of operation is selected for the core. **Note:** In Common Clock mode, the `m_aclk` input does not drive any logic in the AXI Chip2Chip Slave core; however, for XPS to build the system, this clock input needs to be connected. For this, the `m_aclk` input pin can be connected to `m_aclk_out` driven by the AXI Chip2Chip Slave core.
m_aclk_out	Output	Global Master Interface Clock (Common Clock). The `m_aclk_out` signal is output when the Common Clock Mode of operation is selected for the core.
idelay_ref_clk	Input	SelectIO Interface I/O Reference Clock. This signal is applicable only when the SelectIO interface is selected as the FPGA interfacing option and when deskew is enabled for the SelectIO interface. The applicable frequency for `idelay_ref_clk` is 200 MHz or 300 MHz (± 10 MHz)
m_aresetn	Input	Global Reset. This active-Low signal can be asynchronous.

AXI4 Interface Signals

Table 2-8 describes the AXI4 Interface signals for the AXI Chip2Chip Slave core.

Table 2-8: **AXI4 Interface Signals**

Name	Direction	Description
Write Address Channel		
m_axi_awid[C_AXI_ID_WIDTH-1:0]	Output	Write address ID. This signal is the identification tag for the write address group of signals. ID width can be configured from 1 to 6 bits.
m_axi_awaddr[31:0]	Output	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.

Table 2-8: **AXI4 Interface Signals *(Cont'd)***

Name	Direction	Description
m_axi_awlen[7:0]	Output	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
m_axi_awsize[1:0]	Output	Burst size. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
m_axi_awburst[1:0]	Output	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
m_axi_awvalid	Output	Write address valid. This signal indicates that valid write address and control information are available: 1 = address and control information available. 0 = address and control information not available. The address and control information remain stable until the address acknowledge signal, AWREADY, goes HIGH.
m_axi_awready	Input	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready. 0 = slave not ready.
Write Data Channel		
m_axi_wuser[C_AXI_WUSER_WIDTH-1:0]	Output	Write Data Channel User signals. The WUSER width can be configured from 1 to 4 bits.
m_axi_wdata[C_AXI_DATA_WIDTH-1:0]	Output	Write data. The write data bus can be 32 or 64 bits wide.
m_axi_wstrb[C_AXI_DATA_WIDTH/8-1:0]	Output	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. WSTRB[n] corresponds to WDATA[(8 × n) + 7:(8 × n)].
m_axi_wlast	Output	Write last. This signal indicates the last transfer in a write burst.
m_axi_wvalid	Output	Write valid. This signal indicates that valid write data and strobes are available: 1 = write data and strobes available. 0 = write data and strobes not available.
m_axi_wready	Input	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready. 0 = slave not ready.

Table 2-8: **AXI4 Interface Signals *(Cont'd)***

Name	Direction	Description
Write Response Channel		
m_axi_bid[C_AXI_ID_WIDTH-1:0]	Input	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding. ID width can be configured from 1 to 6 bits.
m_axi_bresp[1:0]	Input	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
m_axi_bvalid	Input	Write response valid. This signal indicates that a valid write response is available: 1 = write response available. 0 = write response not available.
m_axi_bready	Output	Response ready. This signal indicates that the master can accept the response information. 1 = master ready. 0 = master not ready.
Read Address Channel		
m_axi_arid[C_AXI_ID_WIDTH-1:0]	Output	Read address ID. This signal is the identification tag for the read address group of signals. ID width can be configured from 1 to 6 bits.
m_axi_araddr[31:0]	Output	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
m_axi_arlen[7:0]	Output	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
m_axi_arsize[1:0]	Output	Burst size. This signal indicates the size of each transfer in the burst.
m_axi_arburst[1:0]	Output	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
m_axi_arvalid	Output	Read address valid. When High, this signal indicates that the read address and control information is valid and remains stable until the address acknowledge signal, ARREADY, is High. 1 = address and control information valid. 0 = address and control information not valid.

Table 2-8: **AXI4 Interface Signals *(Cont'd)***

Name	Direction	Description
m_axi_arready	Input	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready. 0 = slave not ready.
Read Data Channel		
m_axi_rid[C_AXI_ID_WIDTH-1:0]	Input	Read ID (RID) tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding. ID width can be configured from 1 to 6 bits.
m_axi_rdata[C_AXI_DATA_WIDTH-1:0]	Input	Read data. The read data bus can 32 or 64 bits wide.
m_axi_rresp[1:0]	Input	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
m_axi_rlast	Input	Read last. This signal indicates the last transfer in a read burst.
m_axi_rvalid	Input	Read valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = read data available. 0 = read data not available.
m_axi_rready	Output	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready. 0 = master not ready.
AXI Slave to AXI Master Interrupts		
axi_c2c_m2s_intr_out[3:0]	Output	Level Interrupt signaling from the AXI Master to the AXI Slave.
axi_c2c_s2m_intr_in[3:0]	Input	Level Interrupt signaling from the AXI Slave to the AXI Master.

Slave FPGA Interface Signals

Table 2-9 describes the Slave FPGA Interface signals for the AXI Chip2Chip Slave core.

Table 2-9: **Slave FPGA Interface Signals**

Name	Direction	Description
axi_c2c_selio_tx_clk_out	Input	SelectIO FPGA interface clock from Slave FPGA to Master FPGA.
axi_c2c_selio_tx_data_out[*m*-1:0]	Input	SelectIO FPGA Interface Data from Slave FPGA to Master FPGA. *m* is the number of input I/Os required for Slave-to-Master FPGA interfacing. For details, see Chip2Chip PHY Width in Chapter 4.
axi_c2c_selio_rx_clk_in	Output	SelectIO FPGA interface clock from Master FPGA to Slave FPGA.
axi_c2c_selio_rx_data_in[*m*-1:0]	Output	SelectIO FPGA interface signals from Master FPGA to Slave FPGA. *m* is number of output I/Os required for Master-to-Slave FPGA interfacing. For details, see Chip2Chip PHY Width in Chapter 4.

Status Signals

Table 2-10 describes the status signals for the AXI Chip2Chip Slave core.

Table 2-10: **Status Signals**

Name	Direction	Description
axi_c2c_link_status_out	Output	Link Status: Link Status from AXI Chip2Chip Slave core. Asserted when the Link Detect FSM is in the SYNC state. Deasserted when either the Master or Slave AXI Chip2Chip core is under reset or when Link Detect FSM is not in the SYNC state.
axi_c2c_multi_bit_error_out	Output	Multibit Error: Multibit Error Status from AXI Chip2Chip Slave core. Indicates multiple bits are received with error. For the SelectIO interface, a multibit error is determined during deskew operations and indicates failure of those operations.

Designing with the Core

This chapter includes guidelines and additional information to make designing with the core easier.

General Design Guidelines

The customizable AXI Chip2Chip core provides multiple clocking and I/O interface options to the user. Users can determine the frequency at which the interface needs to be operated. Based on the interface frequency, the user can select the I/O type by providing the appropriate constraints in the user constraints file (UCF). Selecting the SelectIO™ interface DDR option doubles the I/O speed without impacting the latency or performance. Based on the Chip2Chip PHY Width selection, additional internal width conversion stages can be enabled. Each 2:1 stage of width conversion can increase bridging latencies and can also impact performance.

In addition, common clock and independent clock operations can be selected by the user. The common clock mode of operation reduces clock domain crossing latencies, and the independent clock mode provides additional clock conversion functionality. Both AXI Chip2Chip Master and AXI Chip2Chip Slave cores can be independently selected for either Common Clock or Independent clock operation. Operating the AXI Chip2Chip core at frequencies greater than AXI interface frequencies (Independent clock operation) reduces the bridging latencies and can improve overall performance of the AXI Chip2Chip bridging function.

Clocking

Figure 3-1 provides the clocking requirement for the SelectIO interface. In addition to AXI clocks, the Deskew function, when enabled, requires an additional 200 MHz or 300 MHz (± 10 MHz) reference clock. Both AXI Chip2Chip Master and AXI Chip2Chip Slave cores can be independently selected for either Common Clock or Independent Clock operations. When the AXI Chip2Chip Slave core is selected for Common Clock operation, the core provides clock and reset (Link Status) to the interfacing slave device.

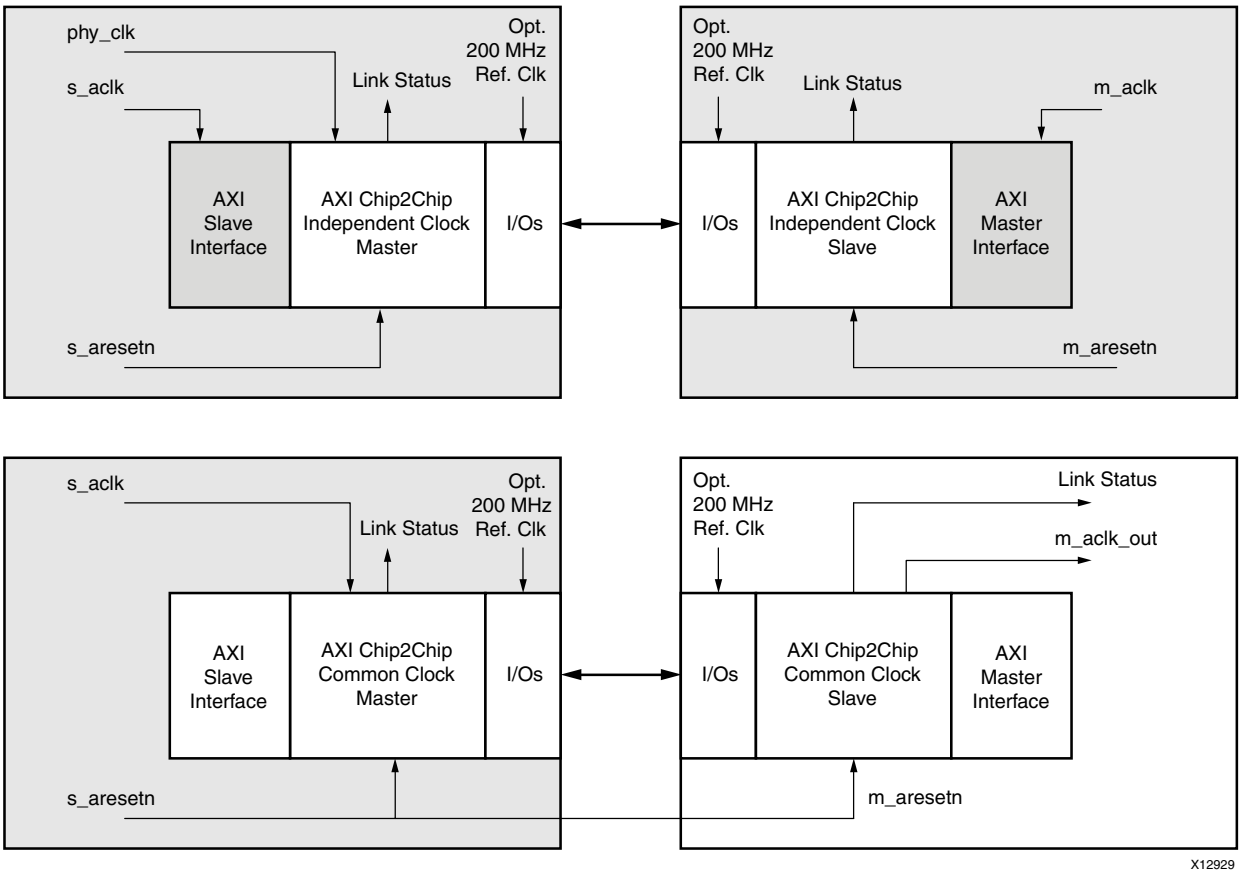

Figure 3-1: **Clocking with the SelectIO Interface**

Resets

The AXI Chip2Chip core allows both Master and Slave cores to have independent reset mapping. The link detect FSM ensures the transactions from the Master FPGA get initiated only when both Master and Slave AXI Chip2Chip cores are out of reset and ready to accept transactions. Reset can also be propagated from Master FPGA to Slave FPGA. In this case, the user needs to map the reset from Master FPGA to Slave FPGA.

It is not recommended to reset either Master or Slave AXI Chip2Chip core during normal operation or when Link Status is asserted. AXI Chip2Chip cores maintain a dedicated channel to communicate the Reset condition during normal operations. When the Slave FPGA is reset during normal operations, the Link Status is deasserted and a link error interrupt is asserted.

Customizing and Generating the Core

This chapter contains information and instructions for using the Xilinx® Embedded Development Kit (EDK) system to customize the LogiCORE™ IP AXI Chip2Chip core.

GUI

Figure 4-1 shows the Customization GUI for the AXI Chip2Chip core. The options are described following the figure.

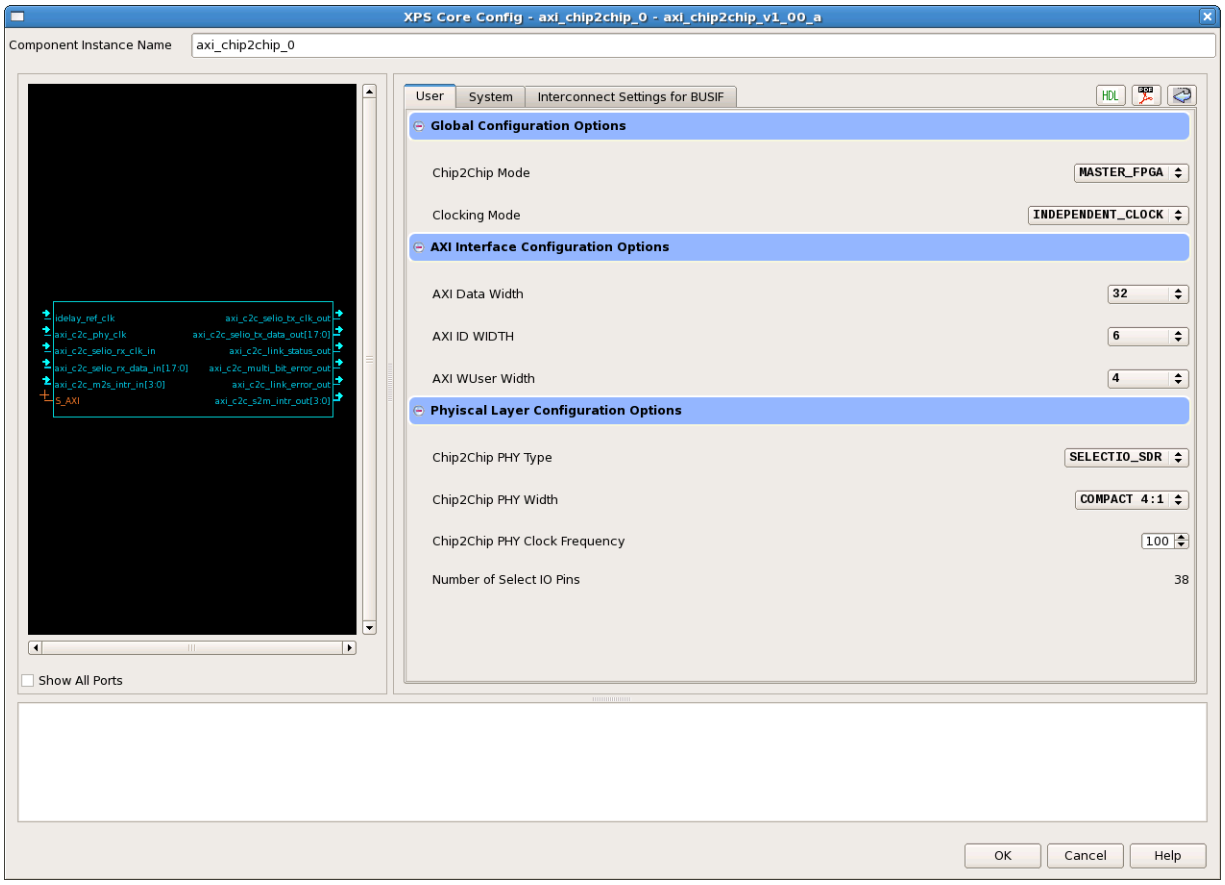

Figure 4-1: **Customization XPS GUI for the AXI Chip2Chip Core**

Chip2Chip Mode

The Chip2Chip Mode configuration option determines AXI Chip2Chip Master or Slave mode of operation.

Clocking Options

The AXI Chip2Chip core can be configured with either Independent or Common Clock domains.

The Independent Clock configuration allows you to implement unique clock domains on the AXI interface and FPGA I/Os. The AXI Chip2Chip core handles the synchronization between clock domains. Both the AXI interface and FPGA I/Os can also be maintained in a single clock domain. The AXI Chip2Chip core can be used to generate a core optimized for a single clock by selecting the Common Clock option.

AXI Data Width

The AXI Data Width user option allows the width of AXI data to be configured. Valid settings for the AXI Data Width are 32 and 64.

AXI ID Width

The AXI ID provides an identification tag for the group of signals in the channel. AXI ID is supported for all write and read channels. ID width can be configured from 1 to 6 bits.

Note: The AXI ID Width of the AXI Chip2Chip Slave core should match the AXI ID Width of the AXI Chip2Chip Master core.

AXI WUSER Width

AXI WUSER defines sideband information that can be transmitted with the write data channel. The valid range for WUSER width is from 1 to 4 bits.

Chip2Chip PHY Type

The Chip2Chip PHY type can be set to either "SelectIO SDR" or "SelectIO DDR."

Chip2Chip PHY Width

The Chip2Chip PHY Width configuration determines I/Os used for FPGA-to-FPGA interfacing. Table 4-1 provides the mapping between Chip2Chip PHY width and the number of input and output I/Os utilized with the selected option.

Table 4-1: **FPGA I/O Utilization**

AXI Data Width	Chip2Chip PHY Type	Chip2Chip PHY Width	Number of Output I/Os	Number of Input I/Os
32	SelectIO SDR	Compact 4:1	19	19
		Compact 2:1	31	31
	SelectIO DDR	Compact 4:1	10	10
		Compact 2:1	16	16
		Compact 1:1	29	29
64	SelectIO SDR	Compact 4:1	26	26
		Compact 2:1	45	45
	SelectIO DDR	Compact 4:1	14	14
		Compact 2:1	23	23
		Compact 1:1	42	42

Note: SelectIO PHY interface routes the clock with the data pins.

Chip2Chip PHY Frequency

The Chip2Chip PHY implements the mixed-mode clock manager (MMCM) on the PHY input clocks. MMCMs are used for clock phase alignment, clock slew reduction, and for compensating clock buffer delays. For common clock AXI Chip2Chip Slave operations, the `m_aclk_out` output is generated from the MMCM. The Chip2Chip PHY Frequency provides the clock frequency parameter to the MMCM.

Parameter Values in the XCO File

Table 4-2 defines the generic parameters from the XCO file.

Table 4-2: **Parameter Values**

Generic Name	Type	Range	Default	Description
C_FAMILY	String	Virtex7, Kintex7, Artix7, Zynq	Kintex7	Carries the family information.
C_MASTER_FPGA	Integer	0-1	0	Determines Master or Slave operation. 0: AXI Chip2Chip Master operation. 1: AXI Chip2Chip Slave operation.

Table 4-2: **Parameter Values *(Cont'd)***

Generic Name	Type	Range	Default	Description
C_COMMON_CLOCK	Integer	0-1	0	Determines the clocking mode. 0: AXI Chip2Chip core in Independent Clock operations. 1: AXI Chip2Chip core in Common Clock operations. This setting can be independently selected in the Master and Slave AXI Chip2Chip cores.
C_AXI_DATA_WIDTH	Integer	32, 64	32	Data width in AXI Interface bits. This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.
C_AXI_WUSER_WIDTH	Integer	1, 2, 3, 4	4	User width in AXI Interface bits. This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.
C_AXI_ID_WIDTH	Integer	1, 2, 3, 4, 5, 6	4	ID width in AXI Interface bits. This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.
C_INTERFACE_TYPE	Integer	0, 1	0	Determines the type of FPGA interface selected. 0: SelectIO SDR. 1: SelectIO DDR This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.
C_INTERFACE_MODE	Integer	0, 1, 2	1	Determines the number of I/Os used for FPGA-to-FPGA interfacing. See Table 2-2, page 10. This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.
C_SELECTIO_PHY_CLK	Integer	40-250	100	Frequency setting for the mixed-mode clock manager (MMCM). For Common clock, C_SELECTIO_PHY_CLK must be set to the `S_ACLK` frequency. For Independent clock, C_SELECTIO_PHY_CLK must be to set to the `axi_c2c_phy_clk` frequency. This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.

Table 4-2: **Parameter Values *(Cont'd)***

Generic Name	Type	Range	Default	Description
C_DISABLE_DESKEW	Integer	0-1	0	When set to 1, disables the deskew function in the Master or Slave core. The deskew function can be disabled for low frequency I/O operations. This setting must be maintained the same in both Master and Slave AXI Chip2Chip cores.
C_DISABLE_CLK_SHIFT	Integer	0-1	0	When set to 1, disables 90-degree phase shift for DDR I/O and 180-degree phase shift for SDR I/O in the MMCM. Clock shifting can be disabled for high-frequency DDR I/O operations when the clock half cycle period is less than the maximum deskew range of 2.5ns. This setting must be maintained the same in both Master and Slave, AXI Chip2Chip cores.

Constraining the Core

Required Constraints

The physical layer is a set of SelectIO™ interface pins that carry source synchronous clock with the data pins.

These I/O pins need I/O Location and I/O Standard constraints. These constraints are board specific and needs to be specified accordingly in the top-level UCF.

Clock Frequencies

The recommended frequency for the AXI interface is up to 200 MHz. For the maximum frequency numbers achieved on the SelectIO PHY interface, see Table A-1 in Appendix A, Verification, Compliance, and Interoperability. The clocking mode for the AXI Chip2Chip core needs to be set based on the AXI Interface Frequency and the required SelectIO interface PHY frequency. The required clocking constraints for the AXI Chip2Chip core are listed below:

- s_aclk. The AXI interface of the AXI Chip2Chip Master core operates in the s_aclk clock domain. This clock is constrained by the XPS tool based on the system/interconnect clock wired to this pin.
- axi_c2c_phy_clk. axi_c2c_phy_clk is the SelectIO interface PHY clock and is applicable when the AXI Chip2Chip Master core is configured in Independent Clock mode. For Common Clock mode, this clock constraint is not required because the PHY clock is the same as s_aclk. This clock is constrained by the XPS tool based on the clock wired to this pin.
- m_aclk. The AXI interface of the AXI Chip2Chip Slave core operates in the m_aclk clock domain. This clock is constrained by the XPS tool based on the system/interconnect clock wired to this pin. When the core is configured in Common Clock mode, this constraint is not required because the AXI interface runs on the PHY clock. For more details, see Clocking in Chapter 3.
- idelay_ref_clk. Both the master and slave AXI Chip2Chip cores utilize the IDELAY_CTRL block for calibration. The idelay_ref_clk input is the reference clock to the IDELAY_CTRL

block. This clock is 200 MHz or 300 MHz (± 10MHz) based on the selected device. This constraint is not required when deskew operation is disabled for the cores. The XPS tool generates the constraint for this clock pin based on the clock wired to it.

- axi_c2c_selio_rx_clk_in. axi_c2c_selio_rx_clk_in is the source synchronous clock of the physical layer. This clock pin must be constrained with the PHY clock frequency. When Common Clocking mode is used, this clock runs at the same frequency as s_aclk.

Clock Management

The AXI Chip2Chip core utilizes the MMCM module to recover the PHY clock. The frequency of the PHY clock is specified by setting the C_SELECTIO_PHY_CLK parameter.

Clock Placement

The clock input pins on the physical layer must be placed on clock-capable I/Os only.

Banking

Device-specific banking rules for placement of PHY I/O pins need to be considered when specifying the top-level UCF.

I/O Standard and Placement

The I/O pins of the AXI Chip2Chip core need I/O Location and I/O Standard constraints. These constraints need to be specified in the top-level UCF.

Verification, Compliance, and Interoperability

This appendix includes information about how the IP was tested for compliance with the protocol to which it was designed.

Simulation

AXI Chip2Chip cores have been tested with Xilinx® ISE® software v14.2 and the Mentor Graphics ModelSim simulator. For the supported versions of these tools, see the Xilinx Design Tools: Release Notes Guide.

The IP is tested using Xilinx proprietary standard AXI Memory Mapped OVM Verification Components (OVCs).

Hardware Testing

Figure A-1 shows the hardware testing setup for the AXI Chip2Chip core.

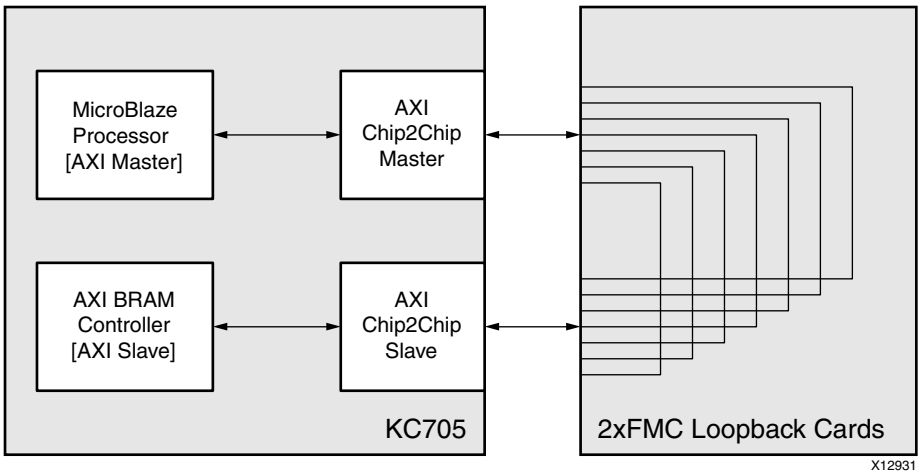

Figure A-1: **AXI Chip2Chip Hardware Testing Setup**

The AXI Chip2Chip core has been hardware validated on a KC705 board using a Kintex™-7 FPGA with -1 speed grade (325T). The setup uses two additional FMC loopback cards. Table A-1 provides configuration details for the AXI Chip2Chip core and the frequency achieved by utilizing this setup.

Table A-1: **Hardware Testing Configuration**

Features			I/Os Utilized	PHY Clock (MHz)
AXI Data Width	**Chip2Chip PHY Type**	**Chip2Chip PHY Width**	**Single Ended [HR I/O Banks]**	**LVCMOS_25 IO [Unterminated]**
32-bit	SelectIO SDR	Compact 4:1	38	200
	SelectIO DDR	Compact 1:1	58	100
	SelectIO DDR	Compact 2:1	32	150
	SelectIO DDR	Compact 4:1	20	150
64-bit	SelectIO DDR	Compact 2:1	46	100
	SelectIO DDR	Compact 4:1	28	150

Note: The AXI (system) clock frequency was set to 100 MHz, and the Common Clock mode of operation was selected for configurations having the same PHY clock and AXI clock frequencies (100 MHz).

Appendix B

Debugging

See Solution Centers in Appendix C for information helpful to the debugging progress.

Appendix C

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

This section provides supplemental material useful with this product guide:

- AMBA® AXI4 specification

  http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ihi0022d/index.html

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the

documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the Embedded Edition Derivative Device Support web page (www.xilinx.com/ise/embedded/ddsupport.htm) for a complete list of supported derivative devices for this core.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/25/12	1.0	Xilinx Beta release.

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