Virtex-5 FPGA Aurora 64B/66B v1.3

DS528 (v1.3) September 19, 2008 **Product Specification**

Introduction

The LogiCORE™ IP Aurora 64B/66B core implements the Aurora 64B/66B protocol using the high-speed serial RocketIO™ GTX transceivers in Virtex®-5 FXT FPGAs. The core can use up to 24 Virtex-5 FPGA GTX transceivers running at any supported line rate to provide a low cost, general purpose, data channel with throughput from 150 Mbps to over 6.25 Gbps.

Aurora 64B/66B is a scalable, lightweight, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented by Aurora 64B/66B protocol licensees using any technology. The protocol is typically used in applications requiring simple, low-cost, high-rate data channels.

The CORE Generator™ software produces source code for Aurora 64B/66B cores with variable datapath width. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control. The Aurora 64B/66B core is delivered with an example design implemented using LFSR for understanding/verification of the core features.

Aurora 64B/66B cores are verified for protocol compliance using the Aurora 64B/66B bus functional model (BFM) and an array of automated simulation tests. The core comes with an example design that supports both single lane and multilane Aurora designs.

Features

- General purpose data channels with throughput range from 150 Mbps to over 6.25 Gbps
- Supports up to 24 RocketIO GTX transceivers
- Aurora 64B/66B v1.1 compliant (64B/66B encoding)
- Low resource cost with very low transmission overhead (3%)
- Easy-to-use framing interface and optional flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation
- LocalLink (framing) or streaming user interface

LogiCORE IP Facts				
Core Specifics				
Supported Device Family	Virtex-5 FXT FPGAs (1)			
Resources Used	I/O	LUTs	FFs	Block RAMs
	Varies with the channel size See "Resource Utilization," page 8			1 per Aurora lane
Special Features	Open source; core is free to use with Xilinx devices			
Provided with Core				
Documentation	Product Specification User Guide			
Design File Formats	Verilog/VHDL			
Constraints File	.ucf (user constraints file)			
Verification	Aurora 64B/66B Bus Functional Model			
Design Tool Requirements				
Xilinx Implementation Tools	ISE®(2) 10.1 or later			
Verification	Mentor Graphics® ModelSim® v6.3c			
Simulation	Mentor Graphics ModelSim v6.3c			
Synthesis	XST 10.1			
Support				
Provided by Xilinx, Inc. www.xilinx.com/support				

1. For more information on the Virtex-5 FPGAs, see DS100: *Virtex-5 Family Overview*
2. ISE Service Packs can be downloaded at www.xilinx.com/support/download.htm

Functional Overview

Aurora 64B/66B is a lightweight, serial communications protocol for multi-gigabit links (Figure 1). It is used to transfer data between devices using one or many GTX transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (data in either one of the directions).

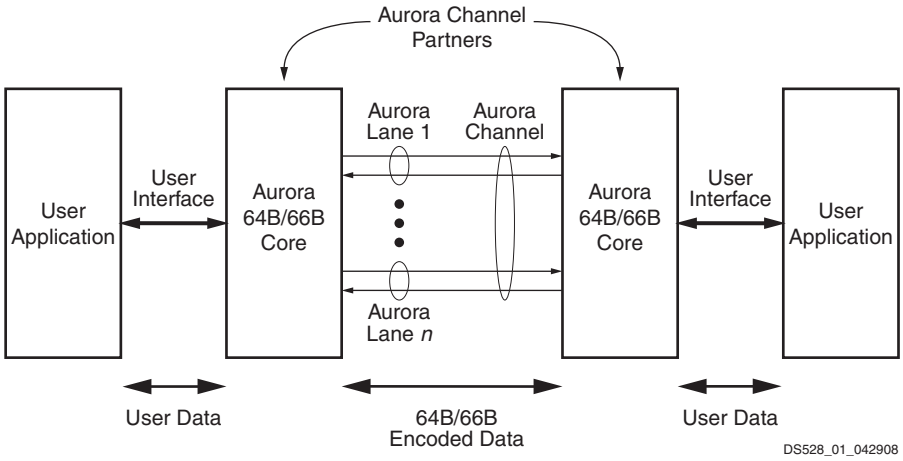

Figure 1: **Aurora 64B/66B Channel Overview**

Aurora 64B/66B cores automatically initialize a channel when they are connected to an Aurora 64B/66B channel partner. After initialization, applications can pass data across the channel as *frames* or *streams* of data. Aurora 64B/66B *frames* can be of any size, and can be interrupted any time by high priority requests. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora 64B/66B, and can be used to throttle the link partner's transmit data rate, or to send brief, high-priority messages through the channel.

Streams are implemented in Aurora 64B/66B as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. The Aurora 64B/66B core can detect errors using 64B/66B coding rules, but it is recommended that a cyclic redundancy check (CRC) block implementing CRC-32 be used with the core to ensure data integrity. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to initialize a new channel. The Aurora 64B/66B protocol uses 64B/66B encoding. The 64B/66B encoding offers improved performance because of its very low (3%) transmission overhead, compared to 25% overhead for 8B/10B encoding.

Applications

Aurora 64B/66B cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora 64B/66B core applications include:

- **Chip-to-chip links:** Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The Aurora 64B/66B core provides the logic needed to use GTX transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links:** Aurora 64B/66B uses standard 64B/66B encoding, which is the preferred encoding scheme for 10-Gigabit Ethernet making it compatible with many existing hardware standards for cables and backplanes. Aurora 64B/66B can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **One-way connections:** In some applications there is no need for a high-speed back channel. The Aurora 64B/66B simplex protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTX transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.
- **ASIC connections:** Aurora 64B/66B is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora 64B/66B protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora 64B/66B bus functional model with automated compliance testing make it easy to get an Aurora 64B/66B connection up and running.

Functional Description

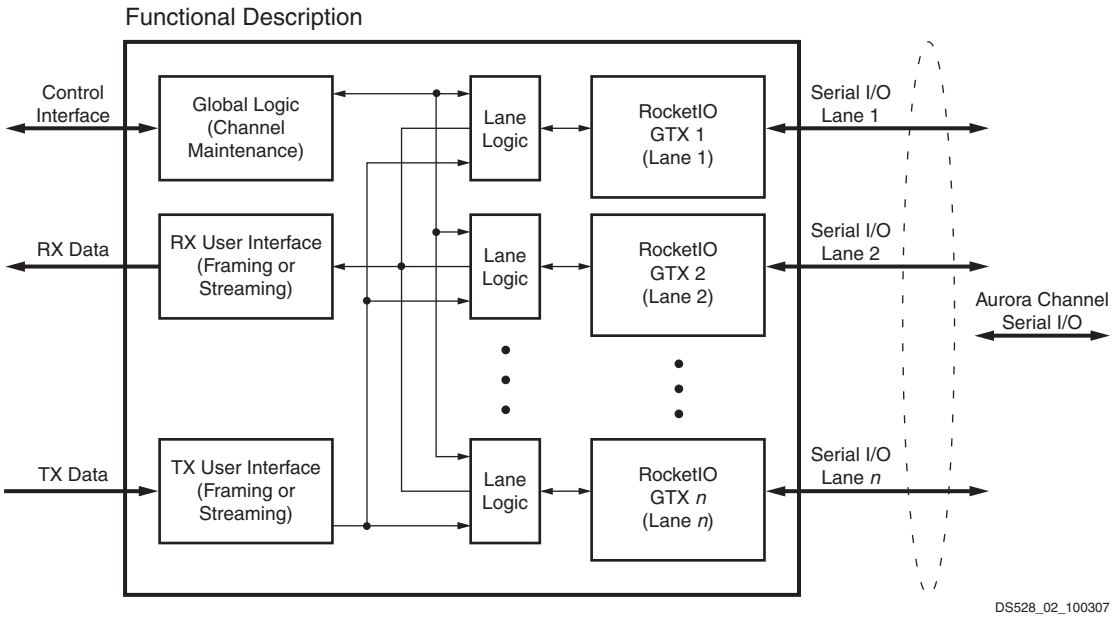

Figure 2: **Aurora 64B/66B Core Block Diagram**

Figure 2 shows a block diagram of the implementation of the Aurora 64B/66B core. The major functional modules of the Aurora 64B/66B core are:

- **Lane logic:** Each GTX transceiver is driven by an instance of the lane logic module, which initializes each individual GTX transceiver and handles the encoding and decoding of control characters and error detection.

- **Global logic:** The global logic module in each Aurora 64B/66B core performs the channel bonding for channel initialization. While the channel is operating, it keeps track of the Not Ready idle characters defined by the Aurora 64B/66B protocol and monitors all the lane logic modules for errors.
- **RX user interface:** The receive (RX) user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and *source ready* and *destination ready* signals for flow control operation. Frames are presented using a standard LocalLink interface. This module also performs flow control functions.
- **TX user interface:** The transmit (TX) user interface moves data from the application to the channel. A stream interface with source ready and destination ready signals are used for streaming data. A standard LocalLink interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora 64B/66B cores). Normally, this interface is driven by a standard clock compensation manager module provided with the Aurora 64B/66B core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

CORE Generator software users can customize Aurora 64B/66B cores for a given application by setting the parameters for the core. Table 1 describes the customizable parameters.

Table 1: **Core Parameters**

Parameter	Description	Values Supported by Aurora 64B/66B Core
Lanes	The number of GTX transceivers used in the channel.	1 to a maximum of 24 GTX transceivers depending on the chosen device
Device	The type of FGPA used to implement the design.	Any Virtex-5 FXT FPGA with GTX transceivers
HDL	The language in which the source code for the core is generated.	Verilog/VHDL
Direction	The type of channel the core will create. Can be full-duplex, simplex in the TX direction, simplex in the RX direction, or two separate simplex modules (one TX and one RX) sharing the same GTX transceiver.	Full-Duplex Simplex-TX Simplex-RX Simplex-Both
Flow Control	Enables optional Aurora 64B/66B flow control. There are two types of flow control: • **Native Flow Control (NFC):** NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • **User Flow Control (UFC):** UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
User K-Blocks	Aurora 64B/66B includes several control blocks that are not decoded by the Aurora interface, but are instead passed directly to the user. These blocks can be used to implement application specific control functions. There are 9 available User K-blocks.	Enable/Disable

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported by Aurora 64B/66B Core
Interface	The user can specify one of two types of interfaces: • **Framing:** The framing user interface is LocalLink compliant. After initialization, it allows framed data to be sent across the Aurora 64B/66B channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • **Streaming:** The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface that has source ready and destination ready signals. User data has to be integral multiple of 8 bytes.	Framing (LocalLink) Streaming
Line Rate	The line rate for Virtex-5 FPGA cores can be set from 150 Mbps to 6.25 Gbps using the CORE Generator software. See the *Virtex-5 FPGA Aurora 64B/66B v1.3 User Guide* for detailed instructions.	150 Mbps to 6.25 Gbps
Reference Clock Frequency	The CORE Generator software accepts parameters to set the reference clock rate for Virtex-5 devices. See the *Virtex-5 FPGA Aurora 64B/66B v1.3 User Guide* for detailed instructions.	A selection of legal rates based on the selected line rate and available clock multipliers in the Virtex-5 FPGA GTX transceivers
Reference Clock	The GTX transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *Virtex-5 FPGA Aurora 64B/66B v1.3 User Guide* for instructions to select the best reference clock network for a given application.	GTXD GREF_CLK
GTX Transceiver Placement	The CORE Generator software provides a graphical interface that allows users to assign lanes to specific GTX transceivers. The *Virtex-5 FPGA Aurora 64B/66B v1.3 User Guide* includes guidelines for placing GTX transceivers for best timing results.	Any combination of GTX transceivers can be selected

Core Interfaces

The parameters used to generate each Aurora 64B/66B core determine the interfaces available (Figure 3, page 6) for that specific core. The Aurora 64B/66B cores have three to six interfaces:

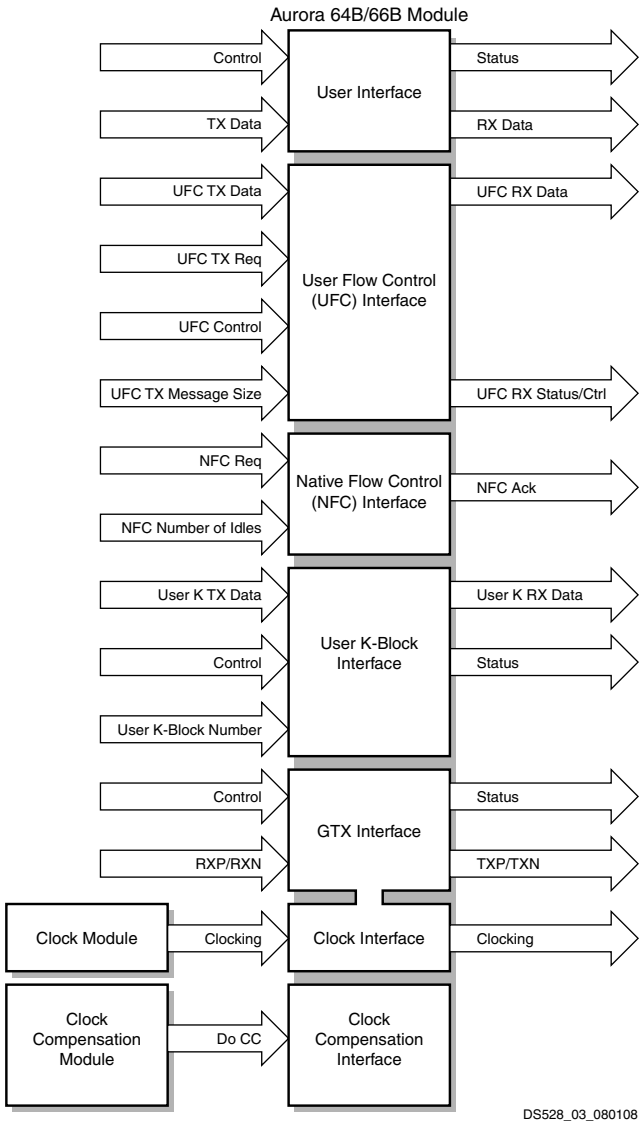

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora 64B/66B core. LocalLink ports are used if the Aurora 64B/66B core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports and source ready and destination ready ports. Full-duplex cores include ports for both transmit (TX) and receive (RX); simplex cores use only the ports they require in the direction they support. The width of the data ports in all interfaces depends on the number of GTX transceivers used by the core.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request and source ready and destination ready ports that are used to start a UFC message, and a port to specify the length of the message. The user supplies the message data to the UFC data port immediately after a UFC request, depending on source ready and destination ready ports of the UFC interface; this in turn deasserts the destination ready port of the user interface

indicating that the core is no longer ready for normal data, thereby allowing UFC data to be written to the UFC data port.

The RX side of the UFC interface consists of a set of LocalLink ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, an NFC XOFF port that when asserted sends XOFF code to the lane partner to stop transmission, and an 8-bit port to specify the NFC PAUSE count (number of idle cycles requested).

Note: NFC completion mode is not applicable to streaming designs.

User K-Block Interface

If the core is generated with User K-block feature enabled, a User K interface is created. User K-blocks are special single block codes that includes control blocks that are not decoded by the Aurora interface, but are instead passed directly to the user. These blocks can be used to implement application specific control functions. The TX side consists of source ready and destination ready ports that are used to start a User K transmission along with the block number port to indicate which of the nine User K-blocks needs to be transmitted. The User K data is transmitted once the core provides a destination ready for the User K interface. It also indicates to the user interface that it is no longer ready for normal data, thereby allowing User K data to be written to the User K data port. The User K-blocks are single block codes.

The receive side of the User K interface consists of an RX source ready signal to indicate the reception of User K-block. Full-duplex modules include both TX and RX User K ports; simplex modules retain only the interface they need to send data in the direction they support.

GTX Transceiver Interface

This interface includes the serial I/O ports of the GTX transceivers and the control and status ports of the Aurora 64B/66B core. This interface is the user's access to control functions such as reset, loopback, and powerdown. Status information about the state of the channel, and error information are also provided by this interface.

Clock Interface

This interface is most critical for correct Aurora 64B/66B core operation. The clock interface has ports for the reference clocks that drive the GTX transceivers, and ports for the parallel clocks that the Aurora 64B/66B core shares with application logic.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. Each Aurora 64B/66B core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance with the *Aurora 64B/66B Protocol Specification*. When the same physical clock is used on both sides of the channel, DO_CC should be tied Low.

Resource Utilization

Table 2 and Table 3 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora 64B/66B *framing* and *streaming* modules. The Aurora 64B/66B core is also available in configurations not shown in the tables; the estimated resource usage for the other modules can be extrapolated from the tables. These tables do not include the additional resource usage for flow controls.

Table 2: **Virtex-5 FXT FPGA Resource Usage for Framing**

Virtex 5 FXT FPGAs			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	LUTs	374	234	263	421
		FFs	580	246	412	614
2	4	LUTs	722	313	548	774
		FFs	1,116	368	830	1,156
4	4	LUTs	1,367	462	1,076	1,436
		FFs	2,148	613	1,628	2,198
8	4	LUTs	2,659	770	2,131	2,767
		FFs	4,213	1,101	3,224	4,282
16	4	LUTs	5,231	1,294	4,244	5,429
		FFs	8,342	2,078	6,416	8,452
24	4	LUTs	7,813	1,797	6,360	8,079
		FFs	12,471	3,039	9,608	12,625

Table 3: **Virtex-5 FXT FPGA Resource Usage for Streaming**

Virtex 5 FXT FPGAs			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	LUTs	363	219	261	406
		FFs	566	232	412	600
2	4	LUTs	695	283	545	746
		FFs	1,092	345	830	1,131
4	4	LUTs	1,319	414	1,067	1,389
		FFs	2,106	571	1,628	2,155
8	4	LUTs	2,572	671	2,115	2,680
		FFs	4,135	1,024	3,224	4,204
16	4	LUTs	5,058	1,157	4,217	5,254
		FFs	8,192	1,928	6,416	8,301
24	4	LUTs	7,554	1,709	6,306	7,829
		FFs	12,249	2,833	9,608	12,398

Performance

Virtex-5 FPGA GTX transceivers have fewer restrictions on line rate, so the speed of Aurora 64B/66B cores in those devices is typically limited by the f_{MAX} of the FPGA design. The maximum line rate is 6.25 Gbps per GTX transceiver.

Verification

The Aurora 64B/66B core supports only the Virtex-5 FXT FPGA and is verified using the Aurora 64B/66B BFM and proprietary custom test benches. An automated test system runs a series of simulation tests on the most widely used set of cores, as well as cores chosen at random. Aurora 64B/66B cores are also tested in hardware for functionality, performance, and reliability using the Virtex-5 FPGA RocketIO characterization platform. The Aurora 64B/66B verification test suites for all possible modules are continuously being modified to increase test coverage across the range of possible parameters for each individual module.

Table 4: **Board Used for Verification**

Test Board
ML523

References

1. Xilinx Aurora Web site: www.xilinx.com/aurora
   - UG237, *Virtex-5 FPGA Aurora 64B/66B v1.3 User Guide*
   - SP011, *Aurora 64B/66B Protocol Specification*
2. SP006, *LocalLink Interface Specification v2.0*
3. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Aurora 64B/66B core is provided free of charge to licensed users. The license for the Aurora 64B/66B core is also free and can be obtained by visiting www.xilinx.com/aurora.

There are three steps required to obtain the core:

1. Install Xilinx ISE 10.1 or greater. See ISE product page for instructions if ISE is not already installed.
2. Install Xilinx ISE 10.1 IP Update 3 to add version v1.3 of the Aurora 64B/66B core to the list of cores available in the Core Selection window in the CORE Generator software.
3. Electronically sign the Aurora 64B/66B Core License Agreement to obtain a license file for the Aurora 64B/66B core. Instructions for this step and the link to the page with the license and the CORE Generator software license file are also at www.xilinx.com/aurora. You must be a registered user on www.xilinx.com to sign the license.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	1.1	LogiCORE IP Aurora 64B/66B v1.1 release.
03/24/08	1.1.1	Miscellaneous typographical edits.
06/27/08	1.2	Virtex-5 Aurora 64B/66B v1.2 release. Updated Figure 3, page 6. Updated throughput speed range. Expanded definition of User K-blocks in "User K-Block Interface," page 7. Added introductory paragraph to "Resource Utilization," page 8. Replaced *Both* simplex with *RX/TX* simplex. Miscellaneous typographical edits.
09/19/08	1.3	LogiCORE IP Aurora 64B/66B v1.3 release. Added support for VHDL to design format and to HDL Parameter inTable 1, page 4. Added Note to "Native Flow Control Interface," page 7. Updated resource usage inTable 2, page 8 and Table 3, page 8.

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