SP605 PCB Assembly Known Issues

This document describes known issues for the SP605 evaluation board.

General Issues

A summary of known issues related to Xilinx tools, IP, and other issues related to the SP605 Evaluation Kit is provided by
AR #33839, *SP605 Known Issues and Release Notes Master Answer Record*.

Boards having assembly number 0431534 are affected by the silicon errata associated with Spartan-6® FPGA LXT CES devices. See
EN118, *Spartan-6 FPGA LX45T CES Errata*.

All revision D SP605 evaluation board assemblies are modified to comply with the V_{CCINT} requirement defined in EN118 under "Operating Conditions Required when Using I/O Delay Variable Mode." The V_{CCINT} regulator has been adjusted to provide an output of 1.25V instead of the nominal 1.2V by changing the firmware for the TI programmable power device.

A subset of SP605 evaluation board assemblies exceed the Spartan-6 FPGA MGTAVCC voltage rail maximum by 0.18 V. See
AR #34093, SP605 Change Two Resistor Network Values on the MGT_A_{VCC} Rail for details.

PCB Issues

There are no known issues associated with the SP605 printed circuit board (PCB).

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
10/20/09	1.0	Initial Xilinx release.
10/03/11	2.0	Converted document to the current template. Revised the use of "SP605 printed circuit board" to be more specific when referring to the "SP605 evaluation kit" and the "SP605 evaluation board assembly." Added reference to answer record 34903.

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