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5V Tolerance Techniques for CoolRunner-II Devices

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Summary

This document describes several different methods for interfacing 5V signals to CoolRunner™-II devices. These techniques may be used whenever voltage signal levels exceed the maximum input requirements of logic devices.

Introduction

The migration to new processes allows for an improvement in many characteristics of semiconductor devices. Die size decreases which lowers cost, propagation delays become smaller, yield improves, and the device's power consumption also decreases. Packages reduce in size, components become more integrated, and additional features become "free" as chip designers can fill additional white space with functions. The one side effect which might be viewed as unfavorable is that the voltage at which the devices operate also decrease. Not too long ago, 12V CMOS logic was the industry standard; however, over the last few months, 1.8V and 1.5V signalling have become commonplace, and designers are examining even lower voltage signal standards with interest.

However, not everyone wants or needs to be on the edge of this voltage migration. A number of components lag the cutting edge, especially analog-specific devices or other semiconductors that benefit from the improved signal to noise ratio associated with higher voltage rail operation.

CoolRunner-II devices operate at a core voltage of 1.8V, and the I/Os have an operational range of 1.5 to 3.3V. While they are not 5V tolerant, several techniques may be used to interface 5V signals to the I/O structures.

Understanding the Basics

Gate Oxide Thickness

One of the predominant factors in determining the input voltage tolerance of an input buffer is the gate oxide thickness used in the fabrication of the device. (Other factors certainly apply, such as process pitch, device geometry, temperature, and other process variation.) Gate oxide plays an important role in the physical characteristics of the basic transistor element. In broad generic terms, a thick gate oxide provides a high amount of voltage tolerance, but sacrifices speed and threshold levels. A thin gate oxide makes for a faster transistor, but the overvoltage tolerance is poor.

Figure 1 is an example of a typical CMOS gate cross section showing the basic components.
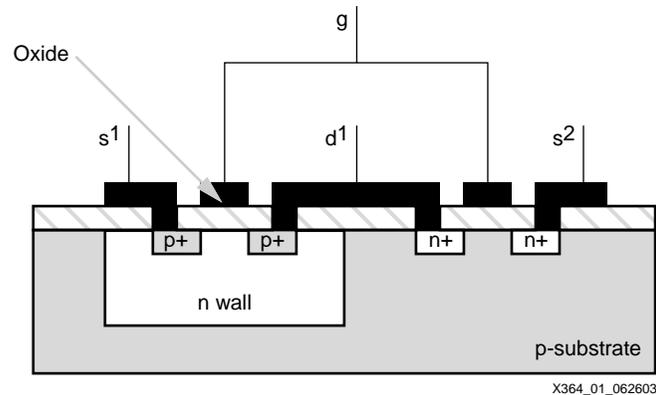
Figure 1: **Basic CMOS Transistor**

Gate oxide is an insulating material that has a specific dielectric strength. This is an insulator that has a "resistance" to a field strength before it begins to break down and conduct. A rule for the insulating strength of gate oxide is typically 6 million volts per cm of oxide thickness. While this initially seems like quite a bit, gate oxide thicknesses are on the order of tens of Angstroms thick. The CoolRunner-II gate oxide thickness is typically 70 Angstroms. This results in an "absolute" limit of about 4.2V. The CoolRunner-II data sheet lists the absolute maximum input voltage as 4.0V. The sensitivity of the input to increased voltage levels changes exponentially. Therefore, 4.2V is significantly more stressful than 4.0V; since higher voltages decrease the life and reliability of the device, it is important to stay within the defined limits of operation.

Charge Tunneling

We would like to think of oxide as a pure insulator, but (for any given temperature) as voltage levels increase on the gate of the transistor, electrons increasingly begin to travel through the gate oxide in an activity called "tunneling." This is typically a benign activity that does not affect the operation nor the reliability of the device, as long as the electrons pass completely through the oxide. However, the gate oxide contains impurities, and these impurities can cause the charge to become trapped in the oxide. If enough of these particles become trapped in the oxide, the dielectric strength of the oxide is diminished, and the insulative properties of the oxide are compromised because the trapped electrons provide a place for additional charge particles to easily 'skip' through the oxide (think of a person being able to step across stones in a stream, where the stones jutting out of the surface of the water are the trapped electrons. The more rocks in the water, the easier it is to cross.). In the case of an input buffer, the input leakage increases substantially. This is an accumulative process that is dependent on the amount of time spent in over voltage conditions. The resulting effect is that the normally insulative, non-conducting gate has now become a conductor. Note that this trapped charge can eventually escape, but enough particles can build up to alter the gate input impedance.

A much more serious effect would be for an over-voltage condition to destroy the structure of the gate oxide.

For these reasons, it is important to not stress input buffers with over-voltage conditions.

Interfacing Techniques

Integrated Circuits

The best solution to translation is to use a dedicated voltage translation device, such as ON Semiconductor's MC74VHC1GT50. This device has a maximum input voltage rating of 7.0V, independent of Vdd. The typical power consumption at 25 degrees Celsius is 1 µA, and it is available in tiny packages such as the SOT353. The propagation delay for this device is 3.5ns. ON Semiconductor also offers solutions for designers seeking bidirectional capability, such as the NCN6011 translator for SIM Card interfacing.

Other vendors supply similar components. Check with Xilinx distributor FAEs for additional offerings.

Resistor Termination

A simple series terminating resistor is **NOT** an acceptable solution to interfacing to 5V input signals. In this situation, the current applied to the pin is not the offending factor. Since the cumulative damage to the gate oxide impedance is caused by voltage, merely limiting the input current does not protect the oxide.

N**ote:** $Vtt + Vf \leq 4.0V$

Resistor Diode Termination

A series resistor and a termination diode to Vtermination may be used to limit the signal swing. A few important parameters must be considered when selecting components. Because of the inherent capacitance associated with a diode, the resistor/diode pair should be matched to the application. The forward voltage of the diode must be taken into consideration also, as this will be the primary limiting factor in association with the termination voltage. Refer to Figure 2 for a block diagram of the technique.
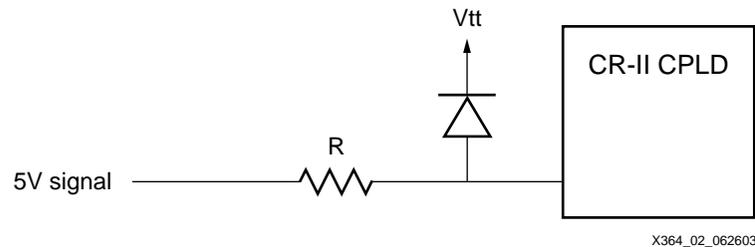

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Figure 2: **Simple Resistor / Diode Termination**

Edge Speed

The combination of the diode capacitance and the resistance will set the RC constant for the rise and fall characteristics of the network. Because of the characteristics of the limiting diode, it is not unusual for the rising edge and the falling edge to exhibit different transition speeds.

Resistor Choice and Power Consumption

Because the signal is being clamped to the termination voltage, a certain amount of power is being "wasted" by the limiting resistor. The selection of this resistor presents an opportunity for compromise between power consumption and edge speed. For any particular diode, an increase in resistance value will result in slower edge transition, and lower power consumption. The converse also applies; a lower value resistor will result in faster edges, but more power is consumed. This further highlights the need for proper diode selection.

Diode Selection

In addition to diode capacitance and forward voltage, the switching characteristics of the diode are important. A fast diode will assist in transition times, and will enhance the symmetry of the rise and fall characteristics of the signal.

Some Empirical Data

To illustrate some of the varied results associated with different resistor/diode pairs, several screen captures from the test bench have been included below. In all instances, the termination voltage is 1.8V, the input type was configured as a LVCMOS 1.8V, and Vdde is 1.8V. The transition speed for the input signal is set to be 3ns, with a 0 to 5 volt swing.

Channel 1 indicates the input signal to the R/D termination pair, and Channel 2 represents the signal captured at the input pin of the CPLD.

Diode Choice: 1n4148

Typical capacitance 4pf, forward voltage 1V, recovery 4ns

This is a very common diode and is probably found in every lab. The characteristics of this diode are acceptable but not ideal. The benefit of this particular diode selection is its low cost.
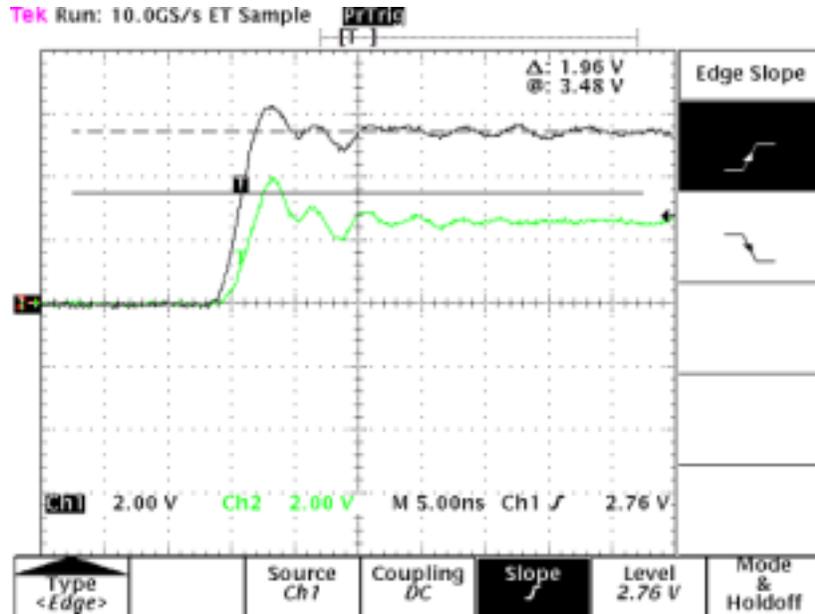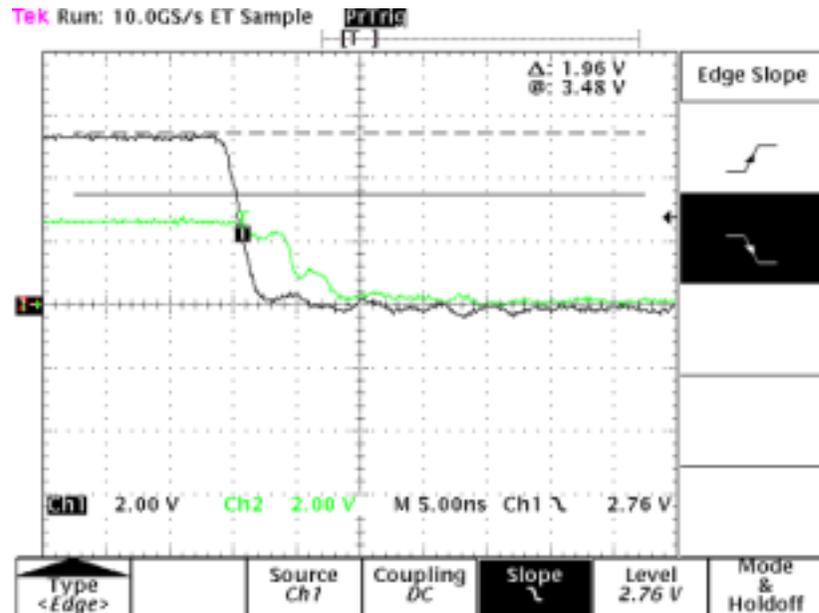

Figure 3: **100 Ohm Series Resistor, Rise, 1n4148**
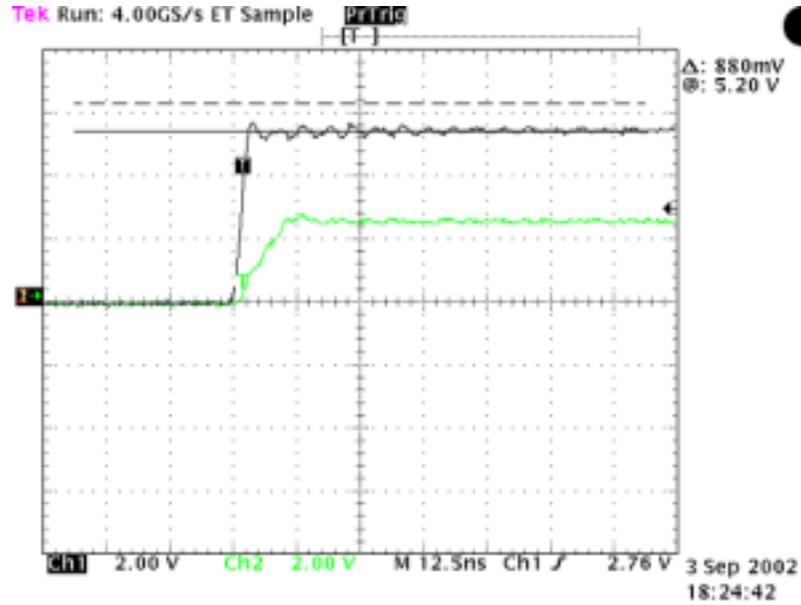

Figure 4: **100 Ohm Series Resistor, Fall, 1n4148**

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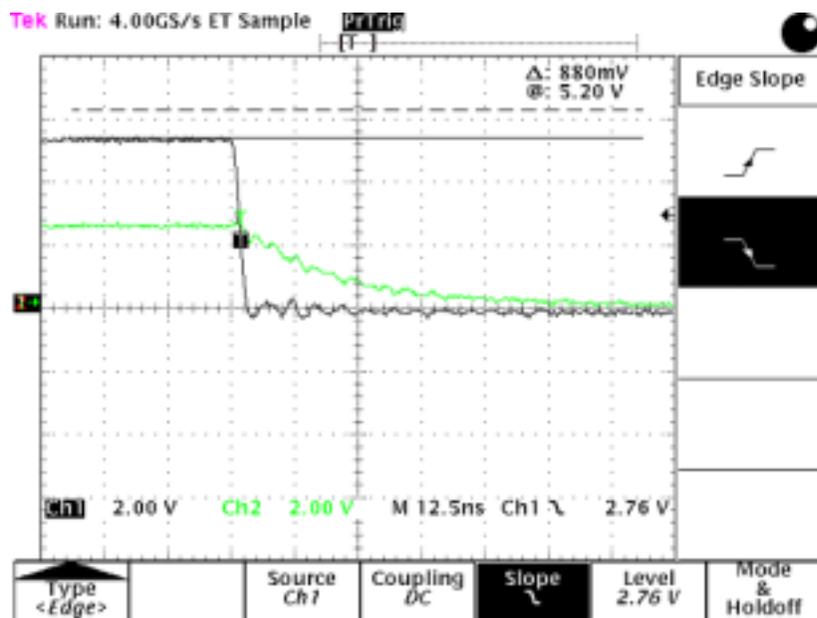*Figure 5:* **1000 Ohm Series Resistor, Rise, 1n4148**

Figure 6: **1000 Ohm Series Resistor, Fall, 1n4148**

Diode Choice: SD101

This is a 2pf capacitance diode with a switching speed of 1ns. It is considerably faster than the 1n4148.
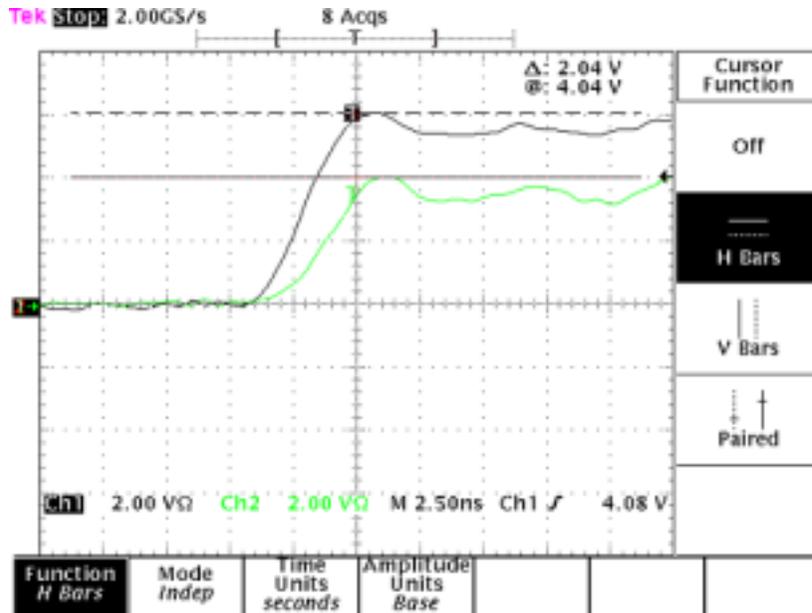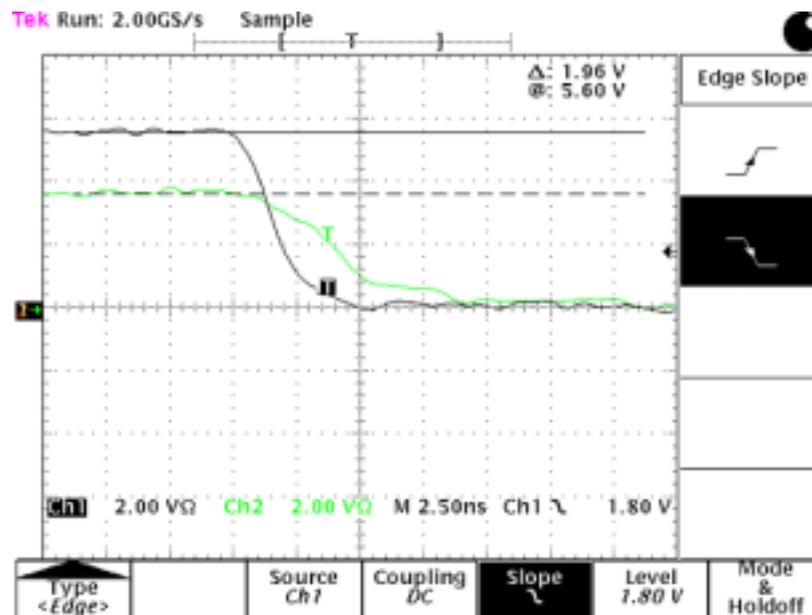
Figure 7: **100 Ohm Series Resistor, Rise, SD101**

Figure 8: **100 Ohm Series Resistor, Fall, SD101**

Some Additional R/D Notes:

1. Besure that the termination voltage is decoupled, tied directly to a power plane, or both. This must be a low-impedance connection to the termination voltage.

2. Keep trace lengths as short as possible to minimize reflection.

3. Use low-capacitance, fast recovery diodes.

4. Watch out for current through diode and termination resistor.

5. For CoolRunner-II devices, use LVCMOS18 or LVCMOS25 input with no internal termination. Terminate diode to 1.8 volts or less, depending on the forward voltage of the termination diode and the I/O input buffer standard.

6. If the rise time of the input signal to the CPLD exceeds 50ns, turn on the input pin's Schmitt trigger.

Source Follower

An n-channel MOSFET may also be used to safely drop the voltage to the input pin of the CPLD; this also has the added benefit of not dissipating any power in a termination resistor. The voltage at the pin of the CPLD is determined by the value of the termination voltage minus the threshold voltage.

This technique depends on the threshold voltage of the transistor, which can vary significantly over process variation. Although it is not recommended for volume production due to the intensive selection of individual transistors, the influencing factors affecting the choice of the transistor include:

1. A transistor with a low threshold (1.0 to 2.5V) should be used.

2. Termination voltage may need to be non-typical in order to accommodate threshold voltage.

3. Choose a transistor with a low gate capacitance.

4. Decouple the gate to Ground, ensuring that this is a low-impedance connection to the termination voltage.

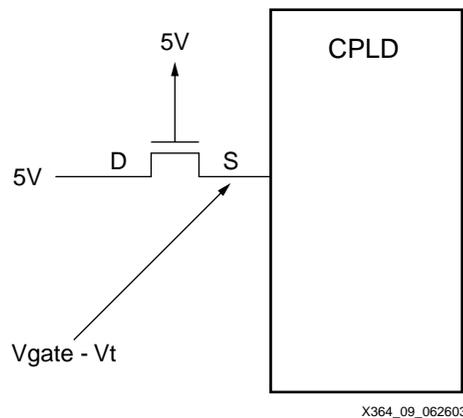Refer to Figure 9 for an example of how to implement this technique.

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Figure 9: **Source Follower Voltage Clamp**

Conclusion

Although CoolRunner-II CPLDs have a maximum input specification of 4.0V, the implementation of several very simple techniques can allow users to input 5V signals to the device. In addition, the true complementary outputs of the CoolRunner-II CPLD allow the driving of 5V devices, as the output swing for 3.3V outputs are capable of driving well above the minimum Vih of 5V devices.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/08/03	1.0	Initial Xilinx release