⟨XILINX⟩®

Power Evaluation Equation for CoolRunner-II CPLDs

XAPP317 (v1.0) September 23, 2003

Summary

This application note provides a quick and simple method for estimating power consumption of CoolRunner-II CPLDs. As an alternative to XPower, power can be quickly and easily computed using the provided equation and coefficients as described in this application note.

Introduction

Many times, users wish to evaluate the potential value of using a low power device such as the CoolRunner-II CPLD prior to designing the system. This precludes using XPower as a power evaluation tool since the system design is usually not a point that is useful to XPower. It is often that design engineers are simply evaluating devices early in the design cycle to determine which is best regarding not only power, but pricing, density, features, etc. It is in these cases that a simple method of evaluating power consumption can be useful. The designer does not often have time early in the design cycle to complete a full power evaluation. Using a simple equation, as described below, will greatly assist the designer during this evaluation period.

CoolRunner-II CPLDs are supported in XPower starting with FISE 6.1i or ISE WebPACK 6.1i.

Derivation

The equation given in this application note was derived first by breaking down the capacitive elements of the device. All CMOS logic devices consume power in two basic ways: Static current, and dynamic current.

Static Current

Static current is the current which exists as current flows through the PMOS and NMOS transistors in a logic element when either of these transistors is turned off. This is an artifact of CMOS structures since these devices leak small amounts of current when one of these transistors is in the off state. Summing these leakages over the complete structure of the device will yield static current for the entire device. The equation represents this current as I_{CCSB}.

In addition, static current in CoolRunner-II CPLDs contains a component due to other circuitry active in the background that is not accessible to the user.

In CoolRunner-II CPLDs, static current is consistent regardless of design and therefore is not a calculated value.

Dynamic Current

Dynamic current is realized when the logic gates change states. Current flows momentarily through the P and N channel transistor in a logic gate when both are turned on at the same time. Figure 1 shows a non-inverting buffer where through current is denoted as Transition Current, commonly known as crowbar current. Transition current is a minor portion of dynamic current due to fast edge rates within the CoolRunner-II CPLD and is therefore considered negligible.

In addition, dynamic current is comprised of other effects of a switching logic gate. Specifically, charge must enter or leave the gate of the next logic element in the chain and is supplied using the P channel transistor or is removed using the N channel transistor of the first logic gate, as shown in Figure 1. Similarly, the routing between gates consists of a capacitive element that must also be charged or discharged in a similar manner.

If the logic gate is the last in the chain of logic and is driving an external load, this load will also have a capacitive element to its structure. For example, this external load can be the printed circuit board (PCB) trace capacitance and the input capacitance of subsequent devices.
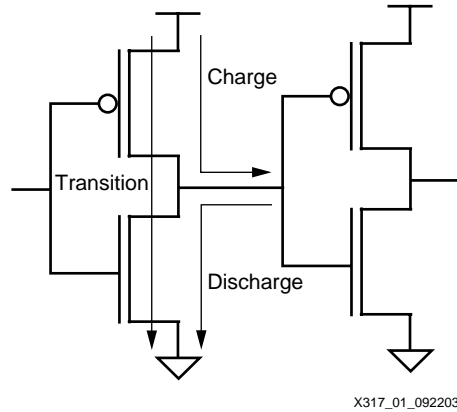

X317_01_092203

Figure 1: **Non-Inverting Buffer**

Using this method, CMOS logic elements can therefore be modeled as simple capacitors. The basic equation to calculate dynamic current consumed in a capacitor is:

$$I = C \cdot V \cdot f$$

where:

- **I** = current, in Amperes
- **C** = capacitance, in Farads
- **V** = voltage, in Volts
- **f** = frequency, in Hz

Summing these capacitive elements over the entire structure of the CMOS device, total dynamic current can be calculated. In the simple equation given below, total capacitance is assumed to be lumped as one capacitive element to simplify the task of deriving the equation.

Over the entire device, dynamic current can further be broken down into several categories to attempt to gain granularity in the calculation: core, I/O and load currents. The core current is comprised of the logic gates which make up the total user functional design. I/O current is derived from I/O logic switching, which is simply the I/O buffer. Load current is found when the I/Os must charge and discharge the external load capacitive elements. These three elements will toggle based on the user/system supplied frequency.

Data Source

The equation in this application note requires the user to insert numbers for some coefficients. These coefficients are included in Table 1 below and are derived in the laboratory.

Core Current Coefficient

Using a 16 bit binary up/down resettable counter, each CoolRunner-II CPLD is filled with one 16 bit counter per Function Block, utilizing the entire device. These counters are clocked from the same clock but have no outputs enabled. The clock frequency is swept from 0Hz up to the

maximum frequency the device can sustain. This data is then used to determine the coefficient for core current, **A**.

16 bit up/down binary counters only have 2 product terms per macrocell, and half of these product terms do not toggle when using the counter in either direction. Also, all product terms and macrocells do not toggle at the same time, reducing the amount of total logic that changes states at any one time. Effectively, 12.5% of macrocells in each counter toggles over time where the MSBs toggle very infrequently with respect to the clock. This type of characterization method is, therefore, not a good benchmark for programmable logic devices. Unfortunately, the PLD industry has selected the 16 bit binary counter as the prime design for comparison.

With this in mind, it is important to understand that the equation and coefficients given below will yield a "ball park" estimate, and are by no means to be considered accurate or a prime standard. XPower was designed to provide a much more accurate representation of power consumption in CoolRunner-II CPLDs. Again, this equation is intended to provide the system designer with an early taste of power consumption in CoolRunner-II CPLDs during the device selection phase of the design process.

I/O Current Coefficient

Similarly, the I/O Current Coefficient is obtained by measurement in the lab. This number is derived from the same data used in XPower which is obtained from more than one type of test. I/O Current is calculated in the equation using the coefficient, **B**.

Load Current Capacitance

It is up to the user to determine the correct value of load capacitance. This may not be an easy task since determining PCB trace capacitance is not straight forward. A network analyzer may be used where a Smith Chart is used to determine impedance of the trace. Extracting the capacitive element from the Smith Chart is the only component of the impedance that is needed for the equations.

Alternatively, since PCBs are not yet manufactured early in the design process, the PCB layout engineers may be able to estimate capacitance of the trace based on line width, length, and board type. It is relatively easy to determine input capacitance of other devices on the PCB trace since these numbers are usually described in the respective data sheets. All of these capacitive elements must be summed by the user and then added into the equation as the coefficient, **C_L**.

The Equation

Below is the equation for calculating total current in the CoolRunner-II CPLD. Again, this equation is intended to provide an evaluation value for current consumption and is simply a "ball park" estimate.

$$I_{CC} = I_{CCSB} + MC_{TOG} \cdot f_{MC} \cdot MC \cdot A + IO_{TOG} \cdot f_{IO} \cdot IO \cdot \left(B \cdot V_{CCIO} + \frac{C_L \cdot V_L}{1000} \right)$$

where:

I_{CC} = total device current, in mA

I_{CCSB} = quiescent current, in mA

MC = total number of non-I/O macrocells used in design

IO = total number of bi-directional or output macrocells used in design

f_{MC} = maximum clock frequency of non-I/O macrocells, in MHz

f_{IO} = maximum clock frequency of I/O macrocells, in MHz

MC_{TOG} = average non-I/O macrocell toggle rate, usually 12.5% (as a fraction, e.g. 0.125)

IO_{TOG} = average I/O macrocell toggle rate, usually 12.5% (as a fraction, e.g. 0.125)

V_{CCIO} = I/O power supply voltage, in V

V_L = external load voltage, in V, usually the same as V_{CCIO}

C_L = external load capacitance, in pF

A = core capacitive coefficient, as given in Table 1

B = I/O capacitive coefficient, as given in Table 1

Table 1: **Power Equation Coefficients for CoolRunner-II CPLDs**

Device	I_{CCSB}	A	B
xc2c32	0.016	0.0085	0.0152
xc2c64	0.017	0.0091	0.0152
xc2c128	0.019	0.0105	0.0152
xc2c256	0.021	0.0119	0.0152
xc2c384	0.023	0.0128	0.0152
xc2c512	0.025	0.0136	0.0152

For CoolRunner-II CPLDs where the I/Os are operated in SSTL or HSTL modes, add 2mA per I/O configured in this manner.

Toggle rate is based on the percentage of edges the average macrocell toggles with respect to the clock active edge. It is typical to specify a number of 12.5% which is derived from the 16 bit binary counter example. In this example, the LSB toggles on 100% of the rising edges of the clock, yielding 1/2 the frequency of the clock at the output of the register. The next significant bit toggles at 50% of the rising clock edges resulting in 1/4 the clock frequency at the register output. Evaluating all 16 bits in this manner yields an average of 12.5% toggle rate for all registers in the counter. It is up to the user to determine the average toggle rate of the macrocells or I/Os based on the intended design. As a quick reference 12.5% may be useful, but toggle rate will vary with different designs.

To obtain power in mW, use the above equation as modified below:

$$P = V_{CC} \cdot (I_{CCSB} + MC_{TOG} \cdot f_{MC} \cdot MC \cdot A) + IO_{TOG} \cdot f_{IO} \cdot IO \cdot \left(B \cdot V_{CCIO}^2 + \frac{C_L \cdot V_L^2}{1000} \right)$$

where:

P = total device power, in mW

Vcc = core voltage, in V

For CoolRunner-II CPLDs where the I/Os are operated in SSTL or HSTL modes, there is 2mA adder per I/O configured in this manner. Therefore, add to the results V_{CCIO} times 2mA per pin with this configuration.

Conclusion

The equation given in this application note provides the designer with an easy method for evaluating the future use of CoolRunner-II CPLDs in a proposed system. This equation provides a value that is reasonable compared to the actual characteristics of the device, but should not be considered an accurate number. XPower should be used to obtain more accurate numbers if this is desirable.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/23/03	1.0	Initial Xilinx release.