Product Not Recommended for New Designs

I/V Curves for Xilinx FPGA and CPLD Families

XILINX ®

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These typical curves describe the output sink and source current for average processing, nominal supply voltage and room temperature. For additional data see the Xilinx IBIS files at: http://www.xilinx.com/techdocs/htm_index/sw_ibis.htm

Note: The Xilinx IBIS files also list the extremes of the processing, temperature and voltage conditions as "min" and "max" (delay). Some tools rename these values as "fast-strong" and "slow-weak". This has nothing to do with the FAST or SLOW slew-rate configuration options, invoked as attributes for each output pin (the default is SLOW).

These slew-rate options are covered in separate IBIS files, with a trailing **"s"** for SLOW slew rate, and **"f"** for FAST slew rate.
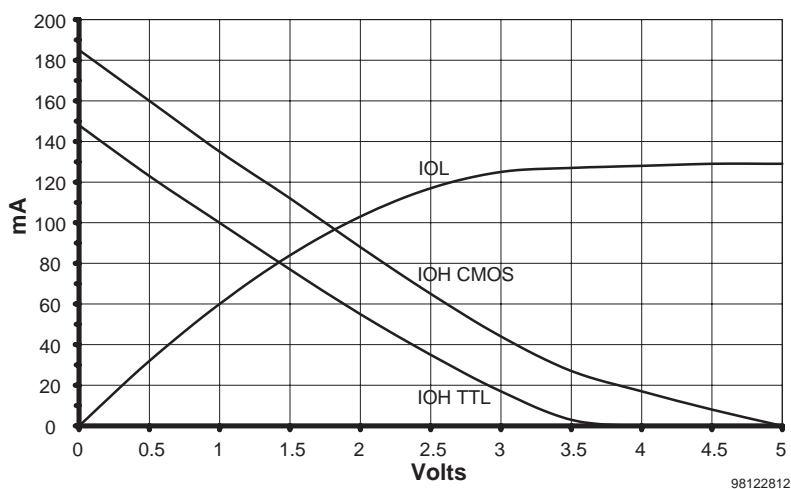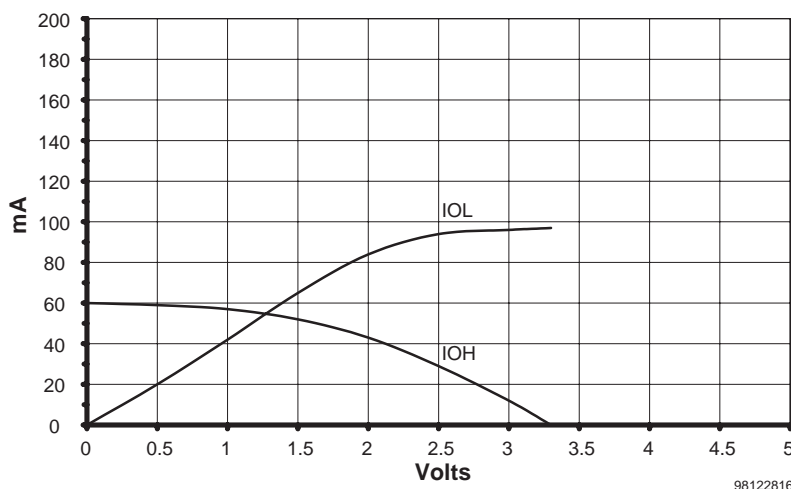
XC4000 Series

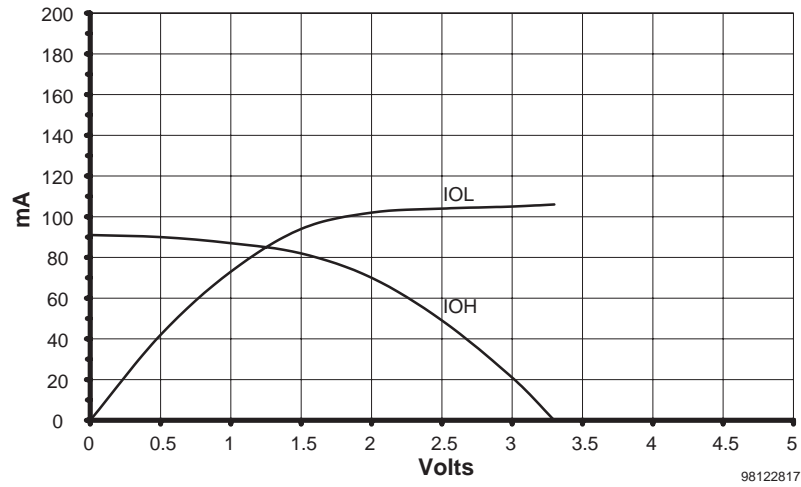*Figure 1:* **XC4000E Family**

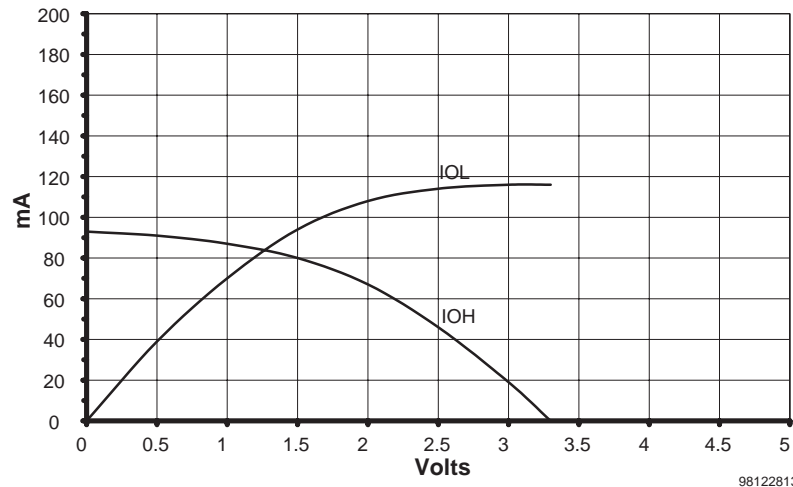*Figure 2:* **XC4000XL Family**

Figure 3: **XC4000XV Family**

Figure 4: **XC4000XLA Family**

Spartan Series
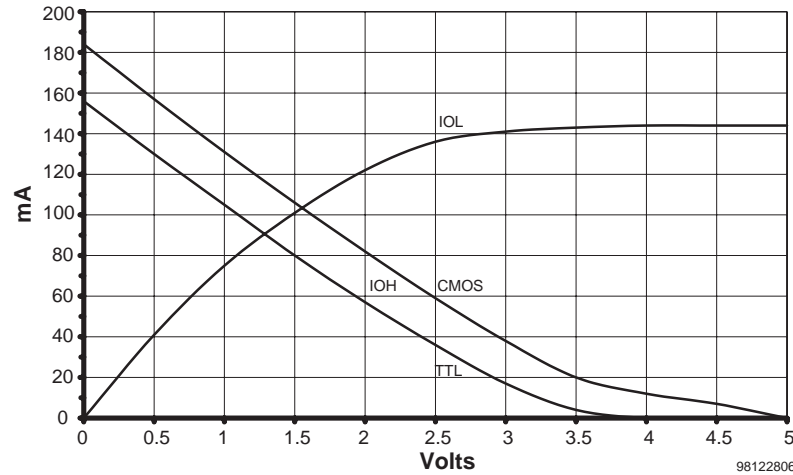
Figure 5: **Spartan Family**
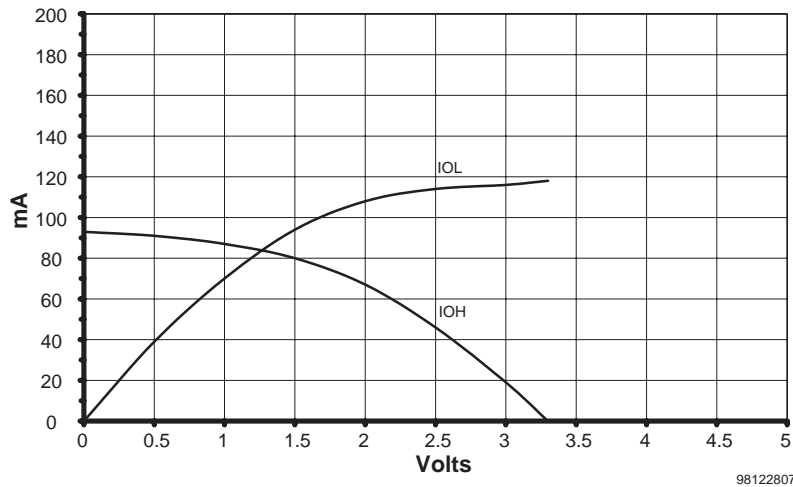
Figure 6: **Spartan-XL Family**
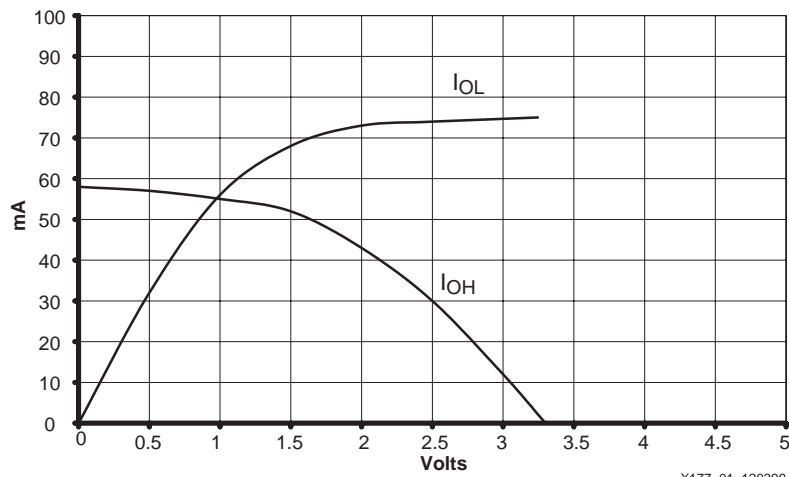
Figure 7: **Spartan-II Family: LVTTL**
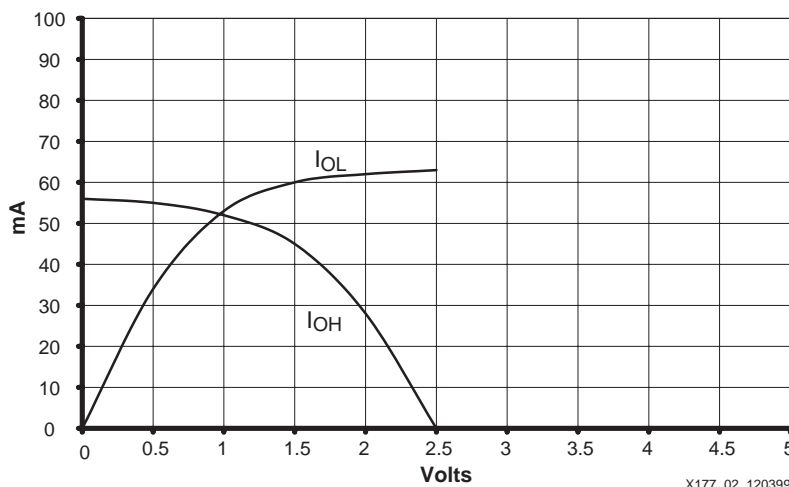
Figure 8: **Spartan-II Family: LVCMOS2**
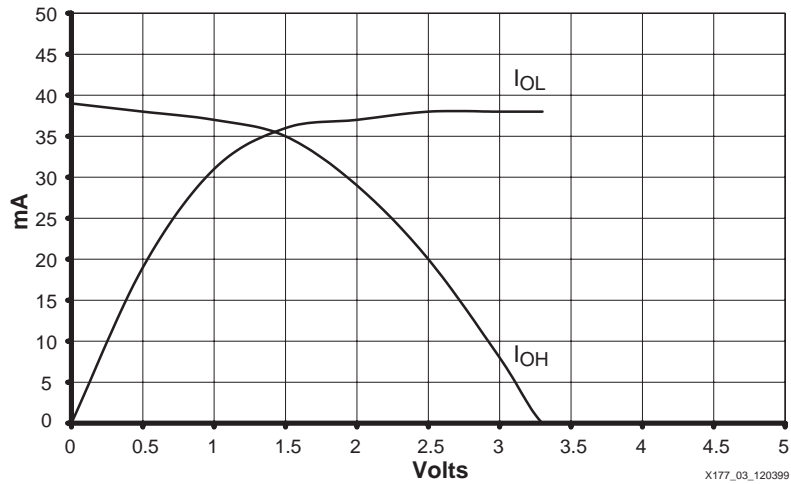
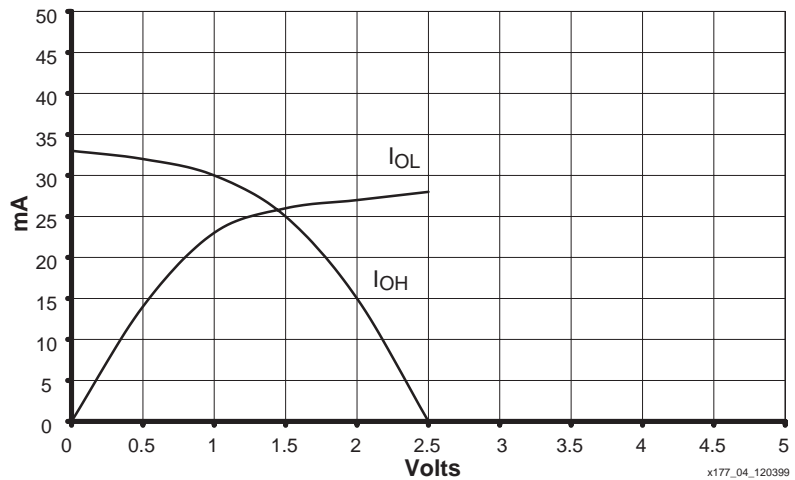*Figure 9:* **Spartan-II Family: SSTL3I**

Figure 10: **Spartan-II Family: SSTL2I**
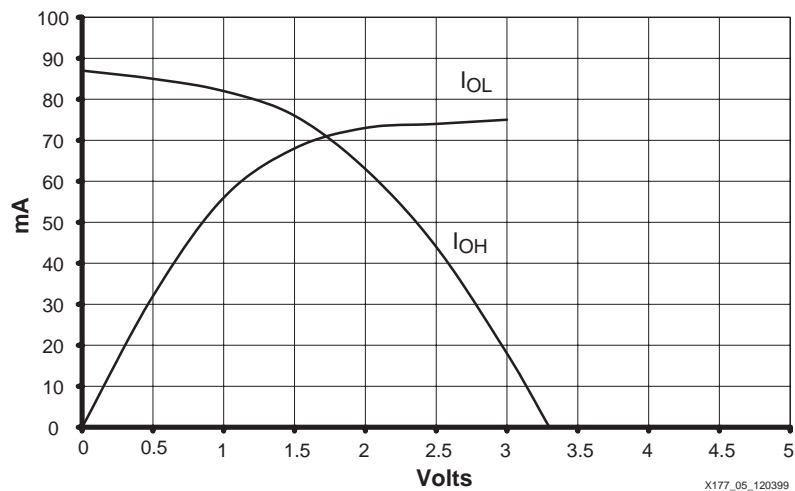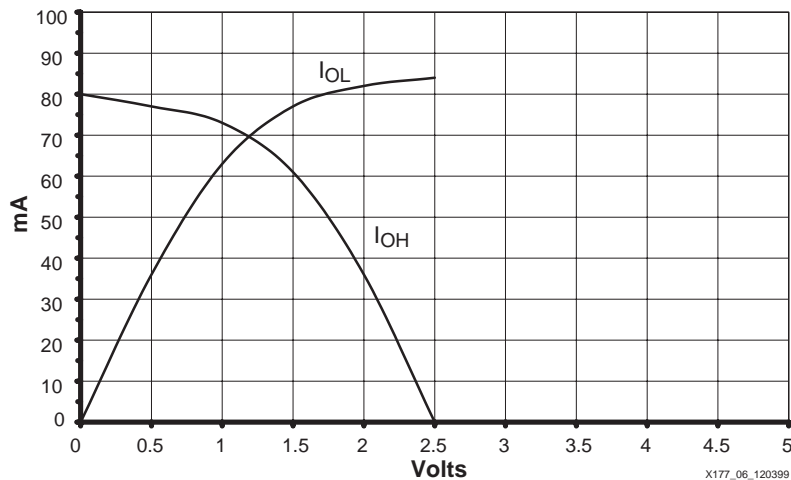

Figure 11: **Spartan-II Family: SSTL3II**

Figure 12: **Spartan-II Family: SSTL2II**
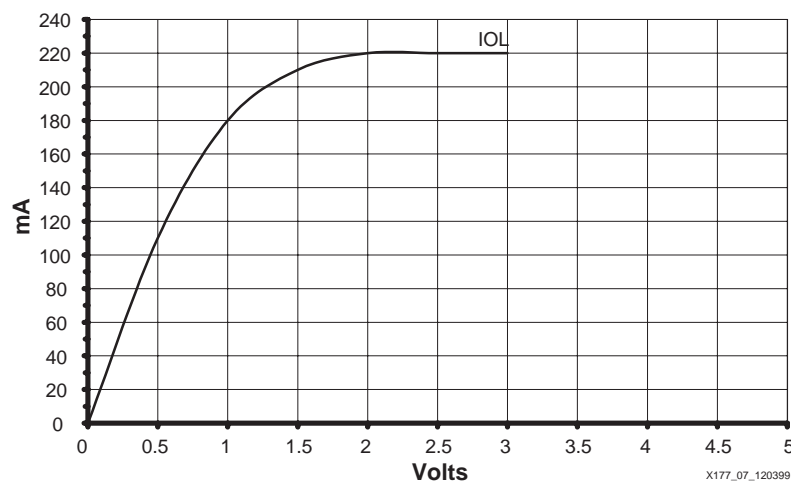
Figure 13: **Spartan-II Family: GTL**
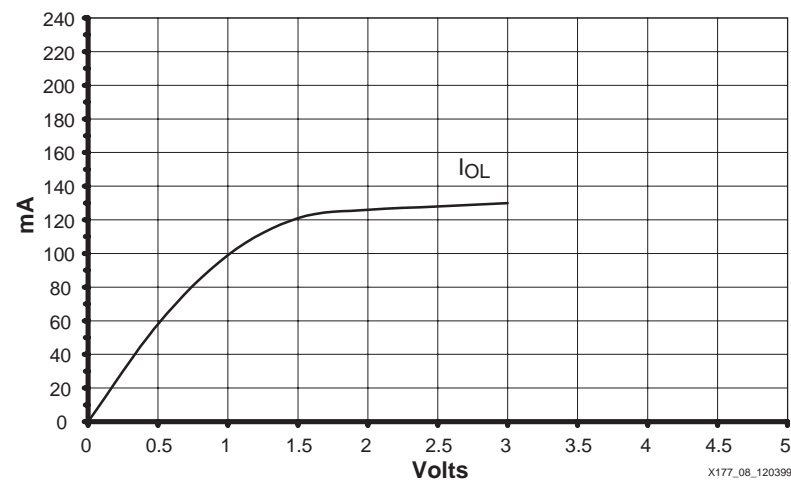
Figure 14: **Spartan-II Family: GTL+**

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XC9500 Series
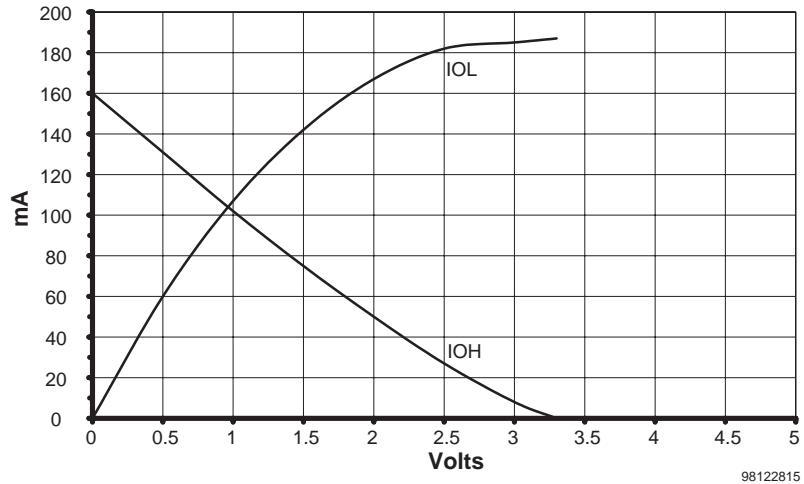
Figure 15: **XC9500 Family**
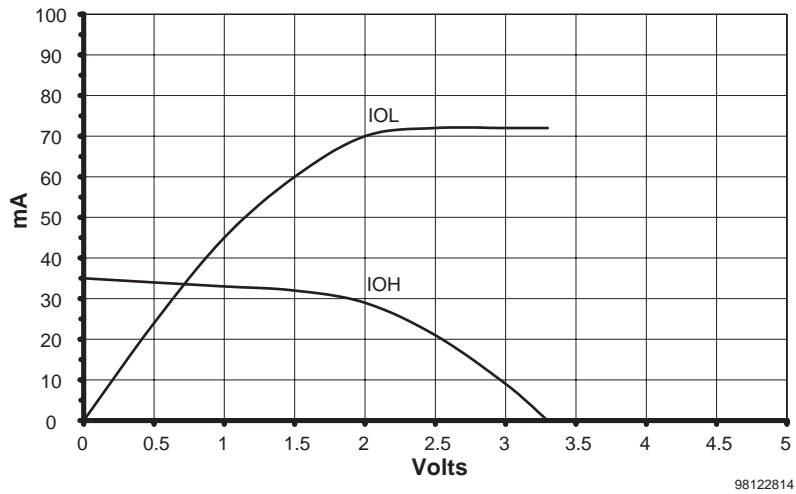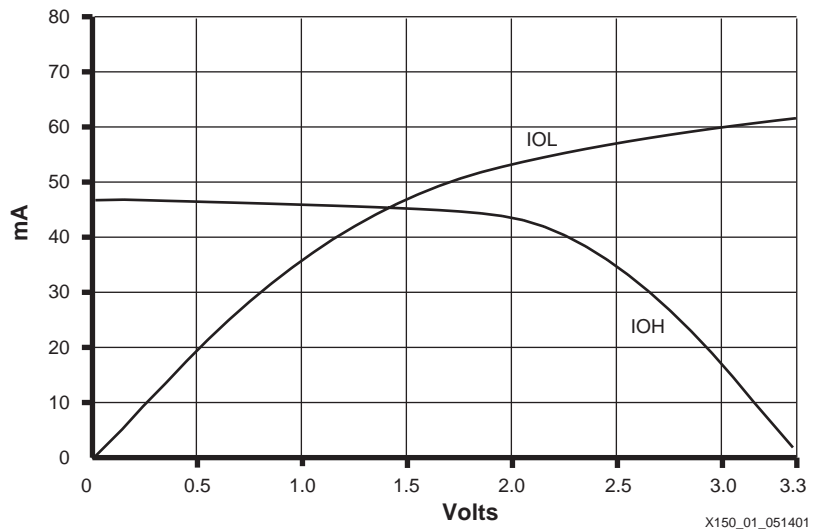

Figure 16: **XC9500XL**

Figure 17: **XC9500XV Family**
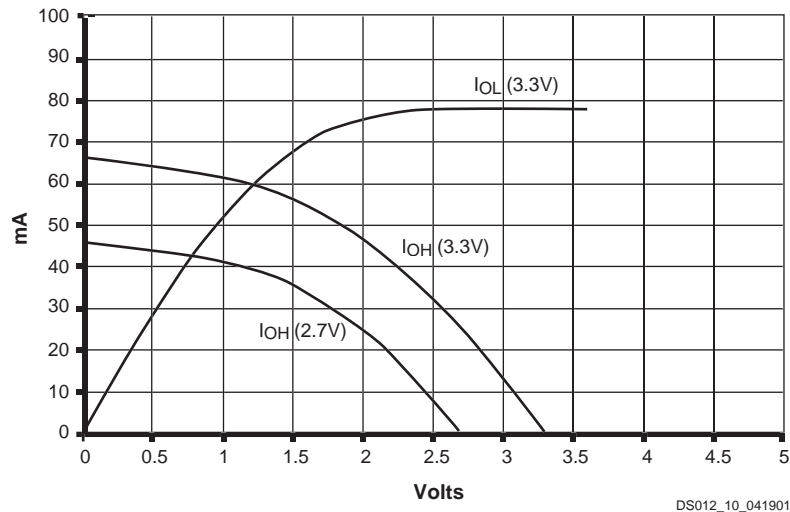
CoolRunner CPLD

Figure 18: **CoolRunner XPLA3**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/04/99	1.0	Initial release
05/15/01	1.1	Changed title, updated format, added Spartan-II Family curves, XC9500XV curve, and CoolRunner XPLA3 curve.