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Understanding XC9500XL CPLD Power

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Summary

The goal of this application note is to discuss XC9500XL CPLD power estimation and optimization and provide the reader with an understanding of sense-amplifier based CPLD power dissipation. A brief discussion of the process for estimation is given. With this information, you can accurately assess the power dissipation for a design. You will also be given guidelines permitting you to make key choices to manage the power dissipation of your design and understand the package thermal limits.

Introduction

Power estimation for CMOS circuits appears to be deceptively straightforward. Most vendors provide a table or an equation that basically splits out the various components of power dissipation for a CMOS part (see Figure 1). Typically, these include a component for the input receivers, which must be derated if driven from TTL rather than CMOS external drivers. Next, there is a component for the internal core of the chip, which usually includes a negligible DC component and an AC component that requires detailed knowledge of the various switching frequencies encountered. It also requires knowledge of exactly how much circuitry is used or unused at any time. Finally, there is a component attributed to the output stages which are functions of both the switching frequencies as well as the external load capacitance. The power is found as the sum of all three components:

$$Power = P_{IN} + P_{CORE} + P_{OUT}$$

This approach is intellectually satisfying, but most users quickly find that they have little knowledge of the various switching frequencies and load capacitance that their circuits create and encounter. They must resort to estimating the speed and loading parameters to obtain a power estimate. One estimate is used as the basis for another, giving fuzzy, inaccurate results. Because of the complexity of arriving at a simple number, many CPLD vendors have resorted to simplifying the power estimation process by providing a single equation for their customers. Frequently, when misused, this results in optimistic values. Often, calculation constants are introduced to simplify the process, but no explanation of their meaning is given, or even limitation guidelines. .
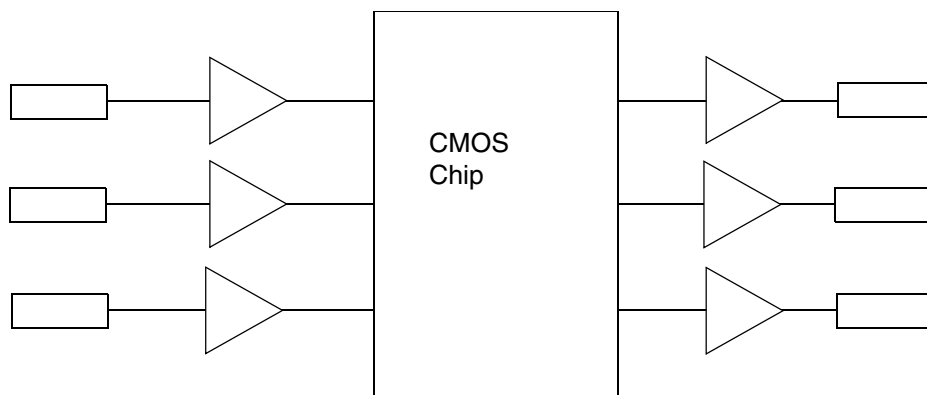
Figure 1: **Power Components of a Typical CMOS Chip**

The approach taken here will be to provide a systematic approach to obtain good results for Xilinx XC9500XL CPLDs. The approach assumes you have already completed the basic

design and wish to know a best and worst case power dissipation, to make an estimate between extremes. For the basis of calculation, we will assume we need to estimate the I_{CC} of a part to determine its power (simply multiply by the corresponding V_{CC}).

Power Dissipation in CPLDs

The basic structure of a CPLD differs from any CMOS device primarily in its programmable internal core. Figure 1 could be modified to insert a programmable AND array structure into the core and most of the power differences between a CPLD and any CMOS chip would negligible. Input power must be accounted for, as well as output power, but the core power is different, due to the CPLD sense amplifier approach. See Figure 2, where we see a simplified structure for a programmable "AND" gate (actually, it is a NOR internally) which performs the programmable logic operations. Figure 2 shows three transistors with floating gates that form a "Wired NOR" when appropriately programmed. (Comment: the XC9500XL parts normally have 108 transistors attached to the Bitline for each product term!) Note the pullup and pulldown resistors (R1 and R2) attached to the Bitline are in reality transistors.
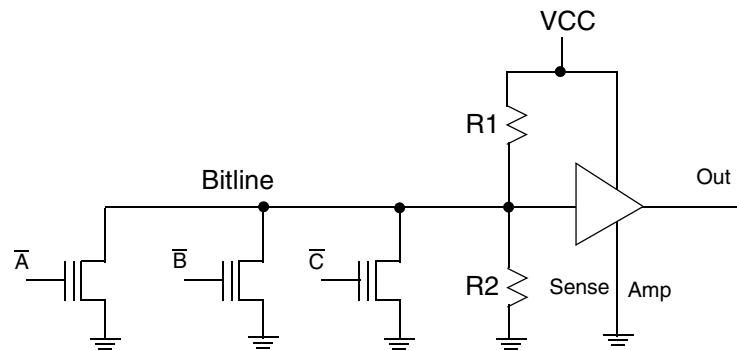
Figure 2: **Simplified CPLD Programmable Structure**

When the Bitline is High (exceeding the trip voltage of the sense amplifier), the output switches. Otherwise, the output remains Low. From a power dissipation viewpoint, lower consumption occurs when $V_{bitline\_hi}$ is driven onto the bitline. Because CPLDs are comprised of macrocells, that include flip-flops, it is important to realize that the flip-flops consume negligible power compared to the programmable cells. With that in mind, a CPLD design can be viewed as being a collection of product terms driving pins and flip-flops. The switching speed of the product terms and output pins become the dominant factor in most cases.
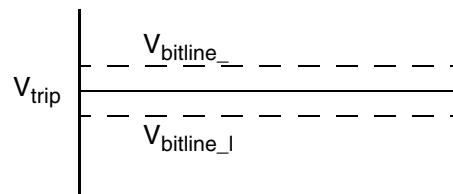
Figure 3: **Trip Voltage, Bitline High and Bitline Low Relationships**

There is a component of current always present in the standard CPLD programmable structure. The current will be typically one of two values passing either through R2 or the transistor(s) to ground. This is the primary factor contributing to DC current consumption in the CPLD core. It cannot be ignored.

R1 in Figure 2 is actually a programmable transistor structure. R1 can be programmatically altered to supply current to the Sense Amp input node to select between a fast ramping input

signal, or a low current slower ramping signal. Table 1 gives relative values of the current drawn by a product term depending on the value of R1 and the condition of the Bitline.

Table 1: **Relative Product Term Currents**

R1 Configuration	Bitline = High	Bitline = Low
High Performance	I/2 µA	I µA
Low Power	I/10 µA	I/2 µA

Table 1 tells us several things. First, each product term can have four different current values. Second, the range is large (10X). And finally, the value is a strong function of whether the product term is driving High or Low. For combinational designs, where all product term inputs are directly driven from the input pins, this is easily accounted for and an accurate static power estimation can be measured. For sequential circuits, the binary values of flip-flops will be attached to the various product terms, so it is difficult to know what the power consumption is unless careful analysis includes the state of the circuit in the estimation. See Figure 4.
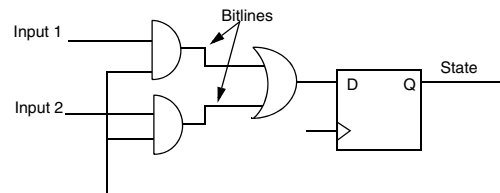
Figure 4: **State Influence on CPLD Power**

In Figure 4, consider the case where Input 1 and Input 2 are both logical ones. If the State variable feeds back a logical one, the Bitlines will both be High. However, if the State variable feedsback a logical zero, both Bitlines will be Low and draw significantly more current. Frequently, this behavior is seen by customers that attempt to measure accurate power when the clock is stopped. Figure 5 gives an example of how this creates an ambiguous measurement.

As shown in Figure 5, there exists an ambiguous region for I_{CC} when the switching frequency is very near DC. This is because the exact state of the sequential machine will dictate just how many specific bitlines are High or Low when the clock is turned off (or very slowly switching). Very quickly after the frequency rises, the I_{CC} assumes a much more linear relationship with frequency. This is why the static current can vary widely with sense amp based CPLDs.
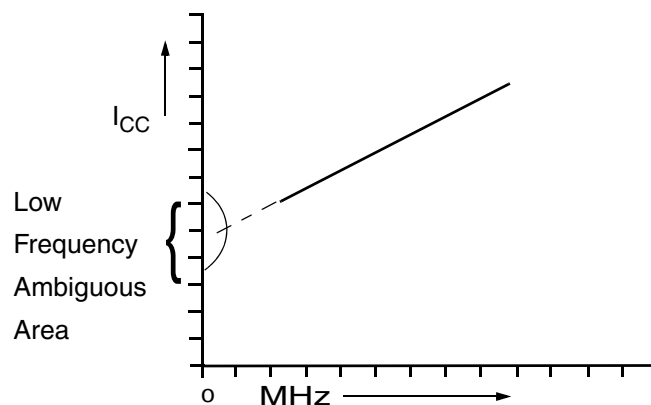
Figure 5: I_{CC} **vs. Frequency**

Returning to Table 1, some additional patterns may be noted. First, unused product terms should be driven high and maintained in low power to minimize I_{CC}. Second, high-performance

mode should be absolutely minimized. Third, driving the bitlines low should be minimized in either High or Low power. An unstated fact is that if a Function Block is totally unused, the design software will not assert the FB power enable bit. In this case, the entire block stays powered down (a few microamps for the block).

Fitting Report Statistics

Estimating the number of p-terms used in a design is not trivial. To obtain an estimate of the design's power dissipation requires first, obtaining an accurate estimate of the distribution of internal components (p-terms, flip-flops, pins, etc.). Frequently, it is easier to do the design in a transportable HDL so the software does the work. It can be reused later. With this approach in mind, it is easy to arrive at a fitting report explicitly giving the number of product terms, the pin split out and how many macrocells are in high-performance or low-power mode. Summary numbers appear at the top of the fitter report. Current XC9500XL reports give results numerically in macrocells. To understand exact product term usage, the individual equations need to have their p-terms tallied.

Knowing the number of product terms does not immediately show how many are high or low on their Bitlines. If buried flip-flops (i.e., the circuit state) have various flip-flops High with others Low, this adds uncertainty regarding whether a product term draws the current for the Bitline high or low situation. Although this approach would yield best results, it is immediately seen why a simpler approach is desirable.

The "One Equation" Approach

Another approach that is common among CPLD vendors is to describe the behavior of the CPLD parts when filled with 16-bit counters. The rationale here is that counters have the basic behavior of state machines, CPLDs are frequently used to build state machines and a straightforward approach with a single equation is desirable. For XC9500XL parts filled with 16-bit counters and allowing a single output (the LSB) to be enabled, the following expression was derived (by laboratory measurement):

$$I_{CC}(mA) = MC_{HP}(0.175*PT_{HP} + 0.345) + MC_{LP}(0.052*PT_{LP} + 0.272) + 0.04 * MC_{TOG}(MC_{HP} + MC_{LP})* f$$

where:

MC_{HP} = # macrocells in high-performance configuration

PT_{HP} = average number of high-performance product terms per macrocell

MC_{LP} = # macrocells in low-power configuration

PT_{LP} = average number of low-power product terms per macrocell

f = maximum clock frequency (in MHz)

MCTOG = average % of flip-flops toggling per clock (~12%)

Additional current must be included for more than one output, or if the load capacitance exceeds the standard load. Also, if no macrocells are used in a Function Block, it may be neglected in the power calculation. However, if even one is used, the product terms for that function block must be included as part of the MC_{LP} count.

Limitations on One Equation Approach

The following limitations may apply to using a counter model for power estimation. This applies to all CPLD manufacturers.

1. Macrocells is a misleading unit of measure

Our single equation is neatly cast in terms of high-performance and low-power macrocells, but it is not macrocells that are configured for power, but product terms. Also, how many product terms are being used in the definition of the macrocell? Many counters only use one, two or three product terms, and the rest are available to be used by other "macrocells."

2. **Invalid for combinational designs**

   Clearly, counter behavior does not model combinational designs with any accuracy because the existence of a state is absent in the combinational design. Combinational portions are probably best handled separately.

3. **Unrealistic sequential model**

   Counters might be a valid model for state machines that use strict binary encoding, but counters do not exhibit a wide range on the number of product terms required for a state machine with a wide variety of transition conditions (i.e., more than a couple of product terms). If, however, the state machine uses between one and three p-terms per flip-flop and has binary encoded states, a counter may be appropriate.

4. **One output enabled**

   Having a single output enabled is optimistic. *Some manufacturers give data with no outputs enabled.* Most counters present several if not all outputs to the outside world. Also, many state machines deliver all outputs to the outside world. This limitation must be accounted for by adding additional output current to the equation provided by the manufacturer. The additional terms will be similar to the following: CV^2f.

   To account for the additional current due to more outputs, it is vital to know the load capacitance (C), the frequency of operation (f) and the voltage swing (V). Note that the values of C and f may be different for each output pin. In particular, C includes the printed circuit board trace capacitance. Also, the voltage swing may not be 5 volts in systems that support multiple voltage output stages. The XC9500XL swings a range of $V_{OH} - V_{OL}$ (2.4 – 0.5) or about 1.9 volts if heavily loaded. If unloaded, it swings closer to 3.3 volts. If V_{CCIO} is attached to 2.5 volts, the situation changes again. Note that one way to lower power consumption in a CPLD is to use the 2.5 V_{CCIO}, which drops I/O power.

5. **Optimistic power consumption**

   If the least significant bit of the counter has a current "I", then the next bit will have I/2 due to it switching at half the frequency. Similarly, the next bit will have I/4, the next I/8, the next again I/16, etc. This shows that an N bit counter will sum to I(1 + ½ + ¼ + 1/8 + 1/16 + 1/32 + 1/64 …). For large counters, this converges to 2. Hence, a 16 bit counter will consume about the same power as two flip-flops simultaneously toggling. By this model, using smaller counters and packing in more of them will dramatically increase the power! Most state machines are only a few flip-flops, so 16-bit counters may not be accurate here, either.

Impact on Packaging

Different packages have different thermal characteristics. Table 2 summarizes the θ_{JA} for the various XC9500XL packages. This information and the following relation can be used to estimate junction temperature for various parts.

Table 2: **Junction to Ambient Thermal Resistance**

θ_{JA}	PC44	VQ64	TQ100	TQ144	PQ208	CS48	CS144	BG352
°C/W	46	41	31	32	32	45	35	12

Notes:
1. θ_{JA} = Junction-Ambient Thermal Impedance.

A maximum junction temperature is established with the following inequality:

$$T_j(max) > \theta_{JA} * V_{CC} * I_{CC} + T_A$$

where:

   T_j = junction temperature

   T_A = ambient temperature

It is advisable to always remain within the package limitations of a given package, so it is appropriate to consider standard ways to reduce power to keep Tj less than 150°C.

Power Minimization Techniques

Knowing that CPLDs can require substantial power, it makes sense to consider some obvious actions that can dramatically lower power. The following checklist should help for starters.

1. **Minimize HP macrocells**

   Because most CPLD users seek raw speed, the XC9500XL design software currently defaults with macrocells configured for high performance. Which also takes the most current. By carefully selecting only those macrocells that need be in high-performance mode, others can be set into low-power mode, which will reduce power.

2. **Minimize FBs used**

   If a single macrocell occupies a Function Block, the Function Block will be turned "on". When this occurs, all unused macrocells in that FB will be powered up to at least the low power Bitline high condition. If this can be avoided, the FB can be eliminated from the power calculation. Naturally, an unused FB strongly suggests investigating a smaller part. This should be done, unless additional capacity is being reserved for a future design upgrade.

3. **Set VCCIO to 2.5V**

   Restricting the voltage swing of the output stage will lower the CV^2f portion of the power consumed. It may impact other chips that expect a larger voltage range, but can dramatically lower power consumed in the CPLD.

4. **Attach unused input pins to UPG**

   Unused pins should not float. Floating input receivers can reside at a totally arbitrary level and may induce input stages to draw as much as 10 mA per pin. This factor is easily remedied by driving the pins to known CMOS levels. One easy way to do this is to simply invoke the User Programmable Ground Option (UPG). Care must be taken that these pins are indeed unused and not reserved for future functionality. They will be driven to ground and if wished, may be externally attached to the PCB ground to provide additional chip grounding.

5. **Use global resources where possible.**

   Overusing P-term clocks, sets, resets and OEs can add up in the power budget.

Conclusions

Power estimation and optimization can be simplified to the point where it is less daunting. However, oversimplified calculation gives optimistic results, which can cause thermal problems. Knowing the amount of circuitry used (report file), the way the circuit is used and having an idea of the input signal behavior can dramatically improve estimation results. If estimated power raises an issue, it is imperative to minimize chip power to obtain the most reliable design. XC9500XL CPLDs offer abundant options to substantially reduce power dissipation to minimize any thermal packaging issues, when operated within their specified conditions.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/22/99	1.1	Initial Xilinx release.
07/18/08	1.2	Change MCHS to MCHP in power equation, page 4. Make note that frequency (f) is in MHz in power equation, page 4.