Designing FPGAs Using the Vivado Design Suite 1

FPGA 1

FPGA-VDES1 (v1.0)

Course Specification

Course Description

This course offers introductory training on the Vivado® Design Suite and demonstrates the FPGA design flow for those uninitiated to FPGA design.

The course provides experience with:

- Creating a Vivado Design Suite project with source files
- Simulating a design
- Performing pin assignments
- Applying basic timing constraints
- Synthesizing and implementing
- Debugging a design
- Generating and downloading a bitstream onto a demo board

What's New for 2021.2

- All labs have been updated to the latest software versions

Level – FPGA 1

Course Details

- 2 days ILT or 16 hours OnDemand
  - 24 lectures
  - 12 labs
  - 7 demos

Course Part Number – FPGA-VDES1

Who Should Attend? – Digital designers new to FPGA design who need to learn the FPGA design cycle and the major aspects of the Vivado Design Suite

Prerequisites

- Basic knowledge of the VHDL or Verilog language
- Digital design knowledge

Software Tools

- Vivado Design Suite 2021.2

Hardware

- Architecture: UltraScale™ family*
- Demo board: Zynq® UltraScale+™ MPSoC ZCU104 board*

* This course focuses on the UltraScale architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the New Project Wizard to create a new Vivado IDE project
- Describe the supported design flows of the Vivado IDE
- Generate a DRC report to detect and fix design issues early in the flow
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Synthesize and implement the HDL design
- Apply clock and I/O timing constraints and perform timing analysis
- Describe the "baselining" process to gain timing closure on a design
- Use the Schematic and Hierarchy viewers to analyze and cross-probe a design
- Use the Vivado logic analyzer and debug cores to debug a design

Course Outline

Day 1

Xilinx Device Architectures

- **Introduction to FPGA Architecture, 3D ICs, SoCs, ACAPs**
  Overview of FPGA architecture, SSI technology, and SoC device architecture. {Lecture}

UltraFast Design Methodology

- **UltraFast Design Methodology: Board and Device Planning**
  Introduces the methodology guidelines covered in this course and the UltraFast Design Methodology checklist. {Lecture}

HDL Techniques

- **HDL Coding Techniques**
  Covers basic digital coding guidelines used in an FPGA design. {Lecture}

Vivado Tool Flow

- **Introduction to Vivado Design Flows**
  Introduces the Vivado design flows: the project flow and non-project batch flow. {Lecture}
- **Vivado Design Suite Project-based Flow**
  Introduces the project-based flow in the Vivado Design Suite: creating a project, adding files to the project, exploring the Vivado IDE, and simulating the design. {Lecture, Lab}

Design Analysis

- **Basic Design Analysis in the Vivado IDE**
  Use the various design analysis features in the Vivado Design Suite. {Lab, Demo}
- **Vivado Design Rule Checks**
  Run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations. {Lab}
- **Introduction to Vivado Reports**
  Generate and use Vivado timing reports to analyze failed timing paths. {Lecture, Demo}

Simulation

- **Behavioral Simulation**
  Describes the process of behavioral simulation and the simulation options available in the Vivado® IDE. {Lecture}

Power

- **Xilinx Power Estimator Spreadsheet**
  Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE. {Lecture, Lab}
- **Power Estimation Using the XPE Tool for Versal ACAPs**
  Describe how to use the Xilinx Power Estimator (XPE) spreadsheet tool for the Versal™ ACAP architecture {Lab}

Synthesis and Implementation

- **Vivado Synthesis and Implementation**
  Create timing constraints according to the design scenario and synthesize and implement the design. Optionally, generate and download the bitstream to the demo board. {Lecture, Lab}

Day 2

Vivado IP Catalog

- **Vivado IP Flow**
  Customize IP, instantiate IP, and verify the hierarchy of your design IP. {Lecture, Demo, Lab}

Pin Planning

- **Vivado Design Suite I/O Pin Planning**
  Use the I/O Pin Planning layout to perform pin assignments in a design. {Lecture, Lab}

Timing – Basics

- **Introduction to Clock Constraints**
  Apply clock constraints and perform timing analysis. {Lecture, Demo, Lab}
- **Generated Clocks**
  Use the report clock networks report to determine if there are any generated clocks in a design. {Lecture, Demo}
- **I/O Constraints and Virtual Clocks**
  Apply I/O constraints and perform timing analysis. {Lecture, Lab}
- **Timing Constraints Wizard**
  Use the Timing Constraints Wizard to apply missing timing constraints in a design. {Lecture, Lab}
- **Basics of Clock Gating and Static Timing Analysis**
  Describes the basics of clock gating and static timing analysis. {Lecture}
- **Calculating Setup and Hold Timing**
  Reviews setup and hold timing calculations. {Lecture}

Configuration

- **Introduction to FPGA Configuration**
  Describes how FPGAs can be configured. {Lecture}

Debugging

- **Introduction to the Vivado Logic Analyzer**
  Overview of the Vivado logic analyzer for debugging a design. {Lecture, Demo}
- **Introduction to Triggering**
  Introduces the trigger capabilities of the Vivado logic analyzer. {Lecture}
- **Debug Cores**
  Understand how the debug hub core is used to connect debug cores in a design. {Lecture}

Tcl

- **Introduction to the Tcl Environment**
  Introduces Tcl (tool command language). {Lecture, Lab}
- **Tcl Syntax and Structure**
  Understand the Tcl syntax and structure. {Lecture}
- **Using Tcl Commands in the Vivado Design Suite Project Flow**
  Explains what Tcl commands are executed in a Vivado Design Suite project flow. {Lecture, Demo}

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