



WP509 (v1.0) February 20, 2019

Understanding Key Parameters for RF-Sampling Data Converters

Xilinx® Zynq® UltraScale+™ RFSoCs provide a single device RF-to-output platform for the most demanding applications. Updated performance metrics more accurately present the direct-sampling RF capabilities of these devices.

ABSTRACT

In direct-sampling RF designs, data converters are typically characterized by the NSD, IM3, and ACLR parameters rather than by traditional metrics like SNR and ENOB. In software-defined radio and similar narrow-band use cases, it is more important to quantify the amount of data-converter noise falling into the band(s) of interest; legacy data conversion metrics are ill-suited to do this.

This white paper first presents the mathematical relationships underlying traditional ADC parameters—SFDR, SNR, SNDR (SINAD), and ENOB—and illustrates why these metrics provide good characterization of data converters in wide-band applications such as superheterodyne receivers. It then delineates why these metrics are inappropriate for data converters that do not function over their full Nyquist bandwidth, as in direct RF sampling applications like SDR. Derivation and measurement of NSD, IM3, and ACLR are described in detail, including use of the Xilinx RF Data Converter Evaluation Tool in the measurement of RF data conversion parameters.

Introduction

Analog data converters based on vacuum-tube technology were developed during World War II for message encryption systems. Since those early days, industry has defined and adopted key parameters (e.g., SNR, SFDR, and ENOB) to quantify the performance of data converters. These historical parameters were developed for conventional architectures that use mixers and filters for channel selection and for conventional Nyquist-rate (i.e., low-frequency sampling) data converters.

Recently, many new RF sampling data converters have been developed for implementation in software-defined radio (SDR) applications, but the parameters adopted for conventional data converters cannot fully characterize RF sampling converters. A new set of parameters, such as noise spectral density (NSD), 3rd-order intermodulation ratio (IM3), and adjacent-channel leakage ratio (ACLR), are required to define the dynamic performance of RF sampling data converters, especially for direct-RF sampling applications.

Xilinx has been providing highly flexible digital processing solutions over a range of SDR applications for some time. Recently, Xilinx released its industry-first Zynq® UltraScale+™ RFSoC, integrating UltraScale™ architecture programmable logic (PL), soft-decision FECs, and multi-channel RF-ADCs and RF-DACs. In these RF-ADCs (12-bit) and RF-DACs (14-bit), the NSD, IM3, and ACLR metrics compare favorably with the same-resolution bit data converters offered by top-tier analog IC vendors—yet the Xilinx Zynq UltraScale+ RFSoC provides reduced power consumption, greater programmability, and higher integration levels. Thus, the Zynq UltraScale+ RFSoC enables the system designer to create highly flexible SDR applications, while simultaneously addressing many of the challenges associated with competitive direct-RF sampling solutions.

In this white paper, the specifications for both conventional data converters and new RF sampling data converters are described, and the preferred parameters for RF sampling converters are identified.

Conventional ADC Specifications: SFDR, SNR, SNDR, ENOB

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is commonly used to measure the usable dynamic range of a data converter before the spurious component interferes with or distorts the fundamental signal. SFDR is defined as the ratio of the root mean square (RMS) value of the fundamental sine wave signal to the RMS value of the peak spurious signal in the output, measured from 0Hz (DC) to one-half the sampling rate of data converters (i.e., $f_s/2$). The peak spurious component could be harmonically or non-harmonically related.

SFDR can be calculated with the following equation:

$$SFDR_{(dBc)} = 20 \log \left(\frac{\text{Fundamental Amplitude (RMS)}}{\text{Largest Spur Amplitude (RMS)}} \right) \quad \text{Equation 1}$$

or,

$$SFDR_{(dBc)} = \text{Amplitude of Fundamental} - \text{Amplitude of Largest Spur}$$

[Figure 1](#) illustrates the SFDR and harmonics performance of the RF-ADC in Zynq UltraScale+ RFSoC, with -1dBFS amplitude @ 240MHz input, such that $\text{SFDR} = 79.0\text{dBc}$, measured from the Xilinx RF Data Converter Evaluation Tool included in the ZCU111 Evaluation Kit set-up. [\[Ref 1\]](#)

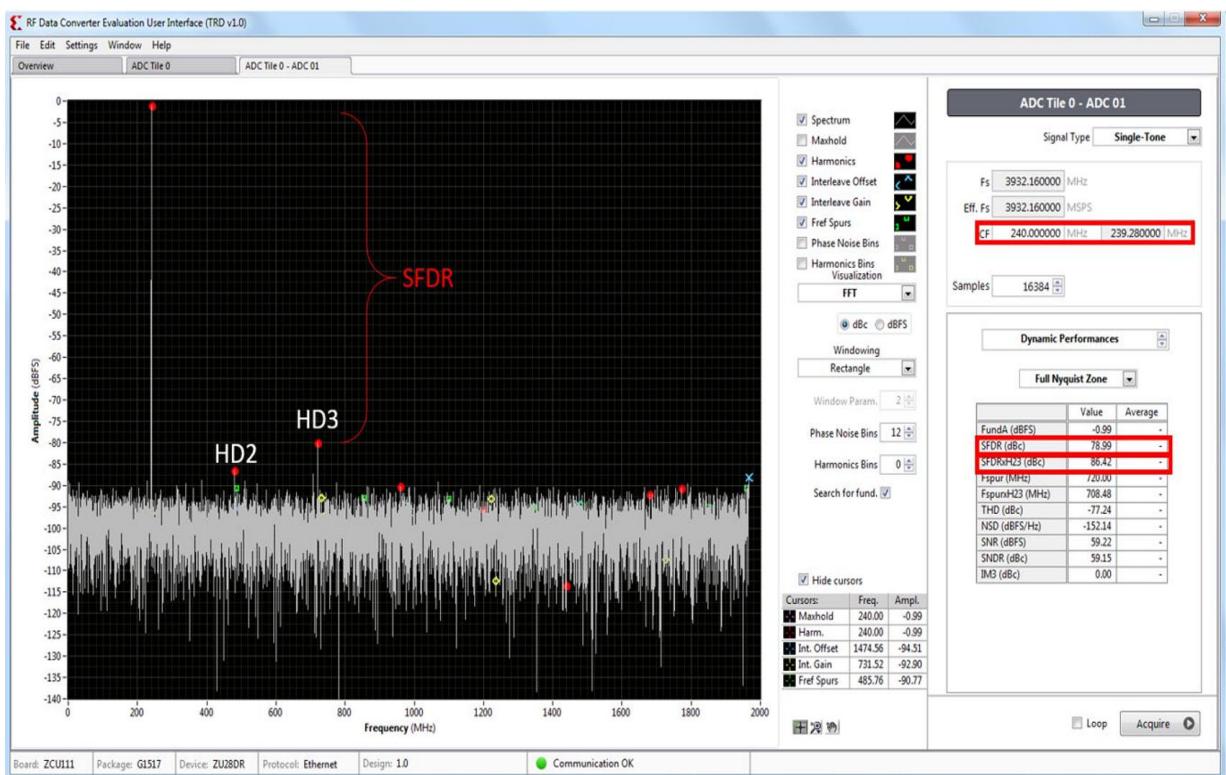


Figure 1: Xilinx Zynq UltraScale+ RFSoC 12-bit RF-ADC, where $f_{in} = -1\text{dBFS}$ @ 240MHz, $f_s = 3.93216 \text{ GSPS}$ (SFDR measured by Xilinx RF Data Converter Evaluation Tool)

According to the above FFT measurement, the largest spur is the third harmonic of the input signal. The SFDR of data converters is often limited by the second or third harmonic of the input signal, but by careful filter design and optimum frequency planning, HD2 and/or HD3 can typically be avoided, greatly improving SFDR. Excluding HD2 and HD3, SFDRxH23 in [Figure 1](#) is 86.42dBc.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is the parameter typically used to quantify the noise in data converters, which is the ratio of the power of the input signal to the power of the noise and is commonly expressed in dB. Similarly SNR can also be evaluated using the RMS value of the signal and noise amplitudes, as shown in [Equation 2](#):

$$\begin{aligned}
 \text{SNR} &= \frac{\text{Power}_{signal}}{\text{Power}_{noise}} \\
 &= \left(\frac{\text{Amplitude}_{signal(RMS)}}{\text{Amplitude}_{noise(RMS)}} \right)^2 \\
 &= 20\log\left(\frac{V_{in(RMS)}}{V_{Q(RMS)}}\right)
 \end{aligned} \tag{Equation 2}$$

SNR usually degrades at higher frequency due to sampling jitter. Noise comes from three sources:

- Quantization noise
- Thermal noise of ADC
- Jitter or sampling uncertainty noise

The theoretical maximum SNR for an ADC with a full-scale sine wave input derives from the quantization noise. SNR has another formula representation,

$$SNR = 6.02N + 1.76\text{dB} \quad \text{Equation 3}$$

over the Nyquist bandwidth, where N is the number of bits of an ideal ADC. This formula gives the best possible SNR over the whole Nyquist bandwidth, assuming a sine wave input for an ideal N -bit data converter (not including harmonic distortion). The SNR of a data converter is also limited by its own thermal noise and sampling clock phase noise. SNR improves when input signal bandwidth is lower than the Nyquist rate. (Detailed derivation is given in the [Appendix](#).) [Ref 2]

Signal-to-(Noise + Distortion) Ratio (SNDR)

SNDR (also called SINAD) is the ratio of RMS signal power to (a) total noise power and (b) the RMS sum of all other spectral components power plus all other harmonic components power at the output (excluding DC), when the input is a sinusoidal wave.

SNDR is one of the key parameters employed to measure the dynamic performance of data converters because SNDR includes all the noise and spurs over the Nyquist bandwidth. SNDR indicates the quality of the input signal; a higher SNDR means the stronger input power differentiated from noise and spurious performance. The SNDR equation can be represented as:

$$SNDR = 10 \log_{10} \left(\frac{P_{Signal}}{P_{Noise} + P_{Distortion}} \right) \quad \text{Equation 4}$$

where P_{Signal} is the average power of the signal of interest, noise, and distortion components. SNDR is commonly expressed in dB (decibels), dBc (decibels relative to the carrier), or dBFS (decibels relative to full scale).

SNDR has another equation representation:

$$SNDR = 20 \log_{10} \sqrt{10^{\frac{-SNR}{10}} + 10^{\frac{THD}{10}}} \quad \text{Equation 5}$$

SNDR is a combination of the SNR and THD specifications, and thus SNDR compares all undesired frequency components with the input frequency, which shows an overall measure of a data converter's dynamic performance.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is a parameter adopted to characterize the quality of a data converter's conversion (in bits) with respect to the input signal over the Nyquist bandwidth. ENOB implies that the converter performs as if it were a theoretically perfect converter. The perfect data converter has absolutely no distortion, and the only noise it exhibits is quantization noise, so SNR would then be equal to SNDR in [Equation 3](#)—i.e., $SNR_{(dBFS)} = 6.02N + 1.76$. Therefore, ENOB is another representation of specifying SNDR:

$$ENOB(N) = \frac{SNDR_{(dBFS)} - 1.76}{6.02} \quad \text{Equation 6}$$

where $SNDR_{(dBFS)}$ assumes a full-scale input signal.

For non-ideal data converters, however, SNDR and ENOB degradation includes noise along with imperfections such as device thermal noise, missing output code, harmonics, AC/DC nonlinearity, gain/offset error, and aperture clock phase noise or jitter. Noise on the external bias reference and power-supply rails also decreases ENOB. [\[Ref 3\]](#)

Furthermore, the ENOB value degrades as frequency increases for the same reason that THD degrades with input frequency due to the non-linearity issue. ENOB comes from SNDR, which is related to THD and SNR. To show an accurate ENOB for a data converter, detailed specifications and conditions required are highlighted in the data sheet.

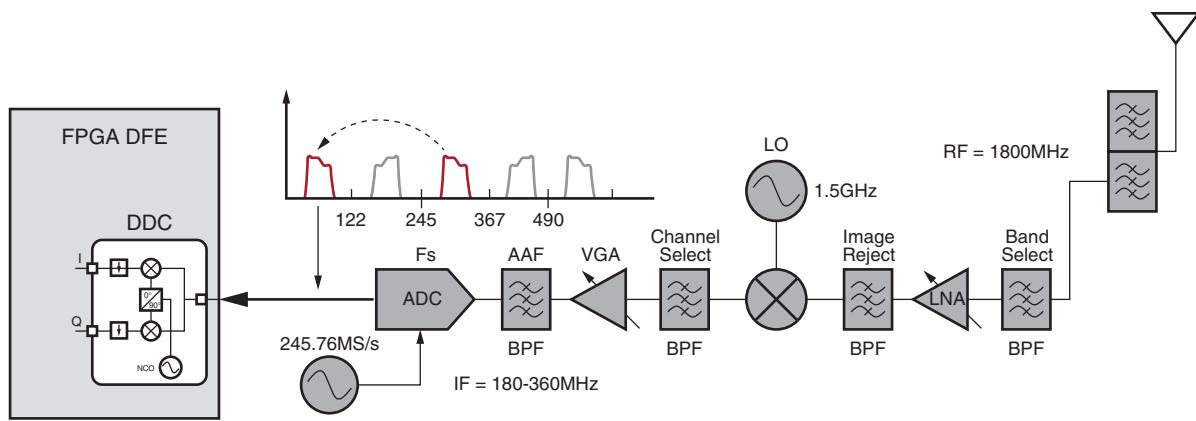
Due to the above criteria, most analog data converter IC vendors generally tend to promote their ENOB in an ideal scenario, especially the ENOB value in the title of the data sheet. However, many system engineers and procurement managers are still curious as to why the measured ENOB value is different from the ideal one in the data sheet. A few key points about ENOB:

- The “number of bits” (12-bit or 14-bit) normally shown in the title of the data converter data sheet refers to digital bit or voltage resolution. This is *not related* to ENOB.
- ENOB is principally a function of noise, non-linearity, and input frequency.
- ENOB is degraded by many external uncertainties (e.g., clock source, power supply).
- ENOB is calculated over the full Nyquist bandwidth (DC to $fs/2$).
- ENOB is *not* a good metric to analyze direct-RF systems such as SDR.

Conventional Data Converter Metrics and the SDR

By definition, SFDR, SNR, SNDR, and ENOB are all metrics derived from the data converter's full Nyquist bandwidth with respect to a single-tone sinusoidal wave input.

A traditional high-IF superheterodyne receiver architecture is shown in [Figure 2](#). In this example, an 1,800MHz RF input is down-converted to an intermediate frequency (IF) of 300MHz by mixing with a 1,500MHz local oscillator (LO). The IF signal is aliased back to 54.24MHz by sampling the ADC at 245.76MSPS. In this case, the signal of interest occupies most of the ADC Nyquist bandwidth. Therefore, SNR and ENOB parameters are valid for use in characterizing the dynamic performance of the ADC.

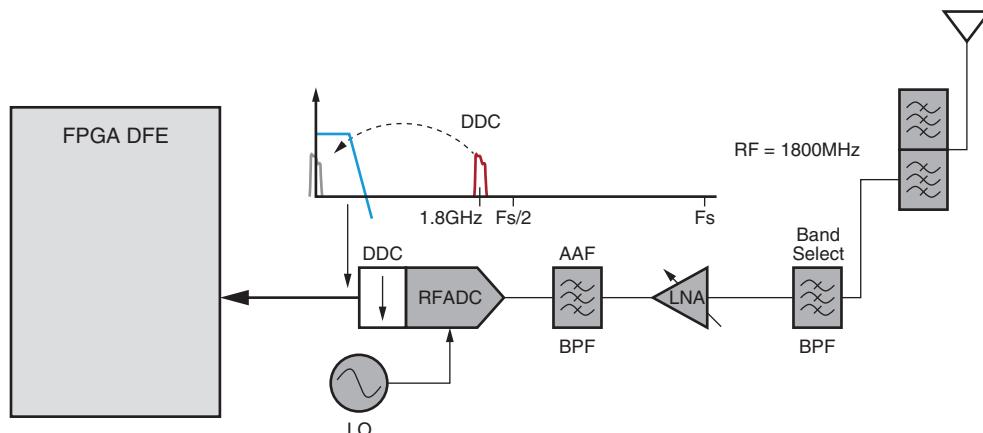


WP509_02_010719

Figure 2: System Block Diagram of High-IF Superheterodyne Receiver

When this is compared with direct-RF sampling as used in the software-defined radio (SDR), it becomes clear that ENOB is not an accurate parameter for characterizing a data converter. In the SDR example illustrated in [Figure 3](#), the RF-ADC samples a large bandwidth containing the signal of interest, with down-conversion and filtering occurring in the digital domain. The biggest concerns in the direct-RF implementation are the artifacts in the down-sampled and filtered band. The SNR, SFDR, and ENOB defined over the Nyquist bandwidth are not relevant because the out-of-band distortions can be filtered out with good frequency planning.

The most important metric is the sensitivity rather than ENOB, SNR, or SFDR defined over Nyquist bandwidth. NSD, IM3, and ACLR are more relevant specifications to quantify the RF sampling data converter's performance because they reflect the true impact of noise and distortion over the decimated band of interest.



WP509_03_010719

Figure 3: System Block Diagram of Direct-RF Sampling Architecture

Applications for RF-Sampling Data Converters

The applications listed below are examples of SDR implementations with usable bandwidth narrower than the entire Nyquist bandwidth:

- 4G Long Term Evolution (LTE) multi-carrier
- 5G massive MIMO (sub-6GHz)
- Microwave backhaul
- Phased-array radar

4G LTE Multi-Carrier

4G LTE has reached more than 80% penetration in most developed countries. The 4G LTE multi-carrier standard is deployed mainly in frequency bands located within the 700–3,800MHz range with 1–20MHz scalable carrier bandwidth and a maximum five aggregated component carriers.

Two major schemes are used in 4G LTE to govern transmission and reception: frequency-division duplex (FDD) and time-division duplex (TDD). FDD aggregated carriers are split over two different frequencies, making it possible to transmit and receive signals (DL and UL) simultaneously. In contrast, TDD component carrier frequencies and their bandwidths are the same for DL and UL.

The 4G LTE standard is presented here (Figure 4) as a practical example that illustrates why SNR, SFDR, and ENOB are irrelevant in evaluating narrow-band RF-ADC and RF-DAC performance. For instance, five 20MHz channels can be received in a 100MHz bandwidth centered on 700MHz, and the data converters in the system are sampled at 4,000MSPS.

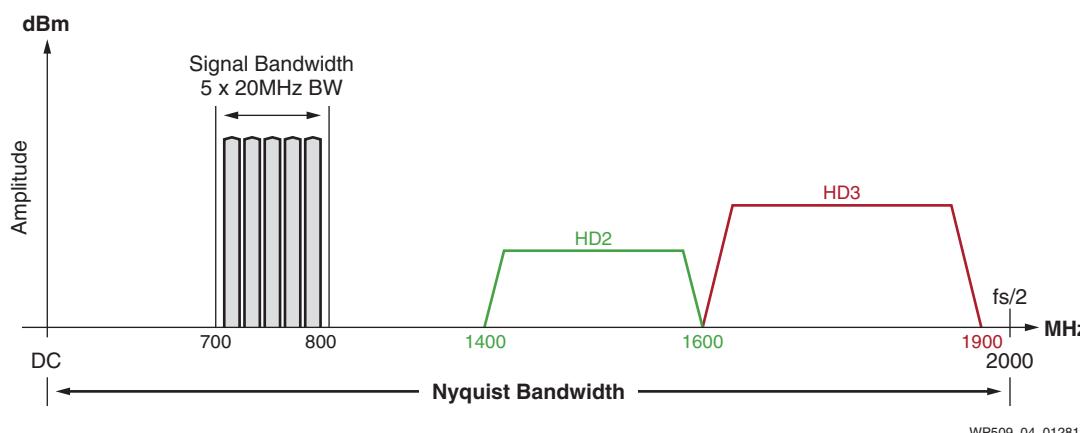


Figure 4: 4G LTE Multi-Carrier Signal Spectrum, 5x20MHz BW Centered at 700MHz (4GSPS Sampling)

- Based on the SNR definition given in the [Signal-to-Noise Ratio \(SNR\)](#) section, the RMS of quantization noise over the entire Nyquist frequency range (i.e., 2,000MHz) is integrated; however, only 20MHz noise channel bandwidth is required to be considered in the 4G LTE implementation.
- Similarly, the [Spurious-Free Dynamic Range \(SFDR\)](#) section reveals the second or third harmonics as the worst-case spurs limiting SFDR performance; thus, SFDR does not affect the performance of the 4G LTE system in the 100MHz receiver bandwidth, assuming correct channel filtering, optimum sampling clock, and good frequency planning. HD2- and HD3-centered frequencies are located at 1,500MHz and 1,750MHz respectively in the Nyquist zone, well removed from the signal. Such out-of-band harmonics are easily filtered out with a bandpass filter in the system.
- Finally, [Effective Number of Bits \(ENOB\)](#) cannot provide realistic system performance metrics because 4G LTE performance is not characterized over the full Nyquist range. [\[Ref 4\]](#)

5G Massive MIMO + 4G LTE Multi-Carrier Solution

The 3GPP has specified two frequency ranges (FR1 and FR2) for the 5G wireless communication system as shown in [Table 1](#).

Table 1: FR1/FR2 Frequency Usage

Frequency Range (FR) Designation	Frequency Range (MHz)	Maximum Channel Bandwidth (MHz)
FR1 (sub-6GHz)	450–6,000	100
FR2 (millimeter wave)	24,250–52,600	400

With an optimal balance between coverage and capacity for cost-efficient implementation, the 3,300–5,000MHz segment of C-band is the primary frequency band for the introduction of 5G for FR1 (sub 6GHz). The advantage of using this frequency band can be exploited in combination with 3,300–3,800MHz (using the LTE/NR uplink coexistence feature of the 3GPP standards) allowing operators to benefit from faster, more cost-efficient deployment of C-band, therefore delivering enhanced capacity without incurring network densification costs.

[Figure 5](#) illustrates an example of 5G Massive MIMO with 100MHz signal bandwidth in FR1 plus a 4G LTE multi-carrier solution with three 20MHz signal bandwidth, centered at 3,500MHz with the sampling clock at 4GSPS, folding back to Nyquist zone 1. HD2- and HD3-centered frequencies are located at 1,000MHz and 1,500MHz, respectively, in Nyquist zone 1. A separation bandwidth of 260MHz exists between the 5G signal and HD2, which is wide enough for a bandpass filter to reduce or even filter out the HD2 and HD3. With the simplicity of this 4G LTE implementation, the total signal bandwidth below the 5G implementation is 160MHz, which is much narrower than the whole Nyquist bandwidth (2,000MHz). By carefully selecting the optimum frequency planning of the narrow-band system, the SNR, SFDR, and ENOB metrics are incapable of characterizing the true performance of RF-sampling data converters for both 5G massive MIMO and 4G LTE communication systems. [\[Ref 5\]](#)

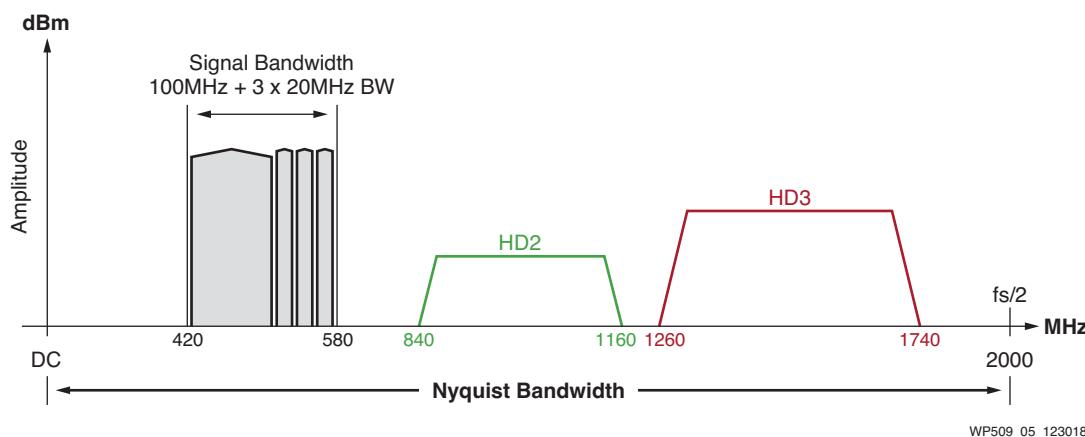


Figure 5: 5G Massive MIMO Signal Spectrum with 100MHz + 3x20MHz Bandwidth Centered at 3,500MHz with Sampling Clock at 4GSPS, Folding Back to Nyquist Zone 1

RF-Sampling Data Converter Specifications

As semiconductor process geometry has been getting smaller, transistor maximum frequency (f_{max}) has been rapidly increasing. Accordingly, usability and performance of RF-sampling data converter products used in direct-sampling communication applications have been significantly improved. As a result, analog data converter makers have largely agreed to use noise spectral density (NSD), 3rd-order intermodulation distortion (IM3), and adjacent channel leakage ratio (ACLR) to characterize the performance of RF-sampling data converters in their data sheets.

Noise Spectral Density (NSD)

As previously described, SNR and ENOB metrics consider a data converter's entire Nyquist bandwidth, which is not relevant to today's RF-sampling data converters, especially for SDR applications. In real applications, tight bandpass filters around the band of interest are often employed, and many RF-sampling ADCs include decimation features to extract only the signal bandwidth of interest. Both aspects always eliminate all the noise outside of those bands. Thus, NSD is a more appropriate metric to quantify the RF-sampling data converter's ability because NSD provides the amount of noise energy in 1Hz bandwidth for a data converter.

While NSD has been applied to data converters for some time, it is still new to some engineers and IC procurement managers. By definition, NSD refers to the noise power per hertz of frequency relative to the RF-ADC full scale input tone, commonly expressed as dBFS/Hz, and is applied to examine the noise performance of data converters with distinct sampling rates.

To obtain the NSD of data converters, the RMS quantization noise power over the whole Nyquist bandwidth must be obtained from the SNR equation, which is defined as the ratio of the power of the fundamental signal to the power of the noise integrated over the first Nyquist zone.

$$SNR_{(dB)} = 10 \log_{10} \left(\frac{P_{fundamental\ signal}}{P_{noise\ (over\ Nyquist\ BW)}} \right) \quad \text{Equation 7}$$

Equation 8 includes the units of the components:

$$SNR_{(dBFS)} = P_{fundamental\ signal\ (dBFS)} - \left(NSD_{(dBFS/Hz)} + 10\log_{10}\left(\frac{f_s}{2}\right)_{(Hz)} \right) \quad Equation\ 8$$

Assuming $P_{fundamental\ signal\ (dBFS)} = 0_{dBFS}$ yields

$$SNR_{(dBFS)} = 0_{dBFS} - NSD_{(dBFS/Hz)} - 10\log_{10}\left(\frac{f_s}{2}\right)_{(Hz)} \quad Equation\ 9$$

Then,

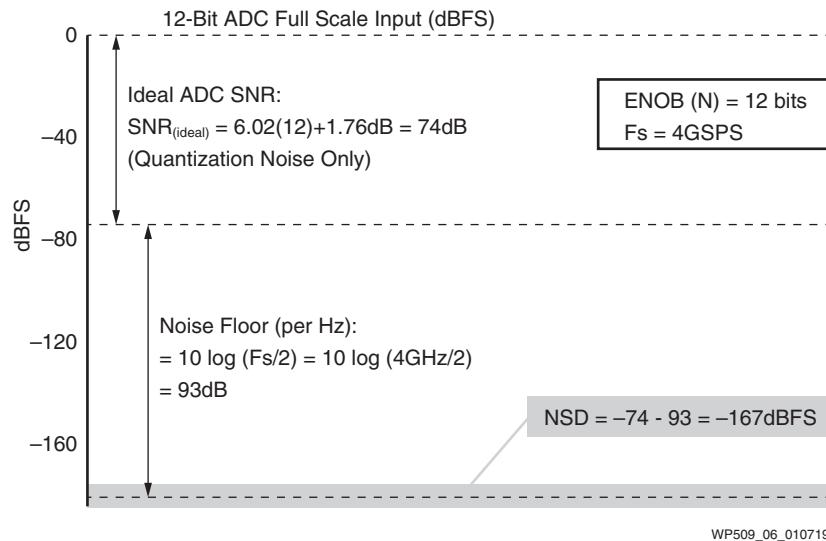
$$NSD_{(dBFS/Hz)} = - SNR_{(dBFS)} - 10\log_{10}\left(\frac{f_s}{2}\right)_{(Hz)} \quad Equation\ 10$$

This NSD equation is useful to evaluate different RF-sampling data converters with different sampling frequencies to characterize which devices have the lowest frequency-band specific noise in SDR applications.

For an ideal 12-bit ADC with a 4GSPS sampling clock,

$$\begin{aligned} NSD &= -(6.02 \times 12 + 1.76)_{(dBFS)} - 10\log_{10}(4GSPS/2)_{(Hz)} \\ &= -(74 + 93) \text{ dBFS/Hz} \\ &= -167 \text{ dBFS/Hz} \end{aligned}$$

[Figure 6](#) illustrates the noise power for this device.



[Figure 6: Graphical Depiction of SNR and NSD in FFT Spectrum](#)

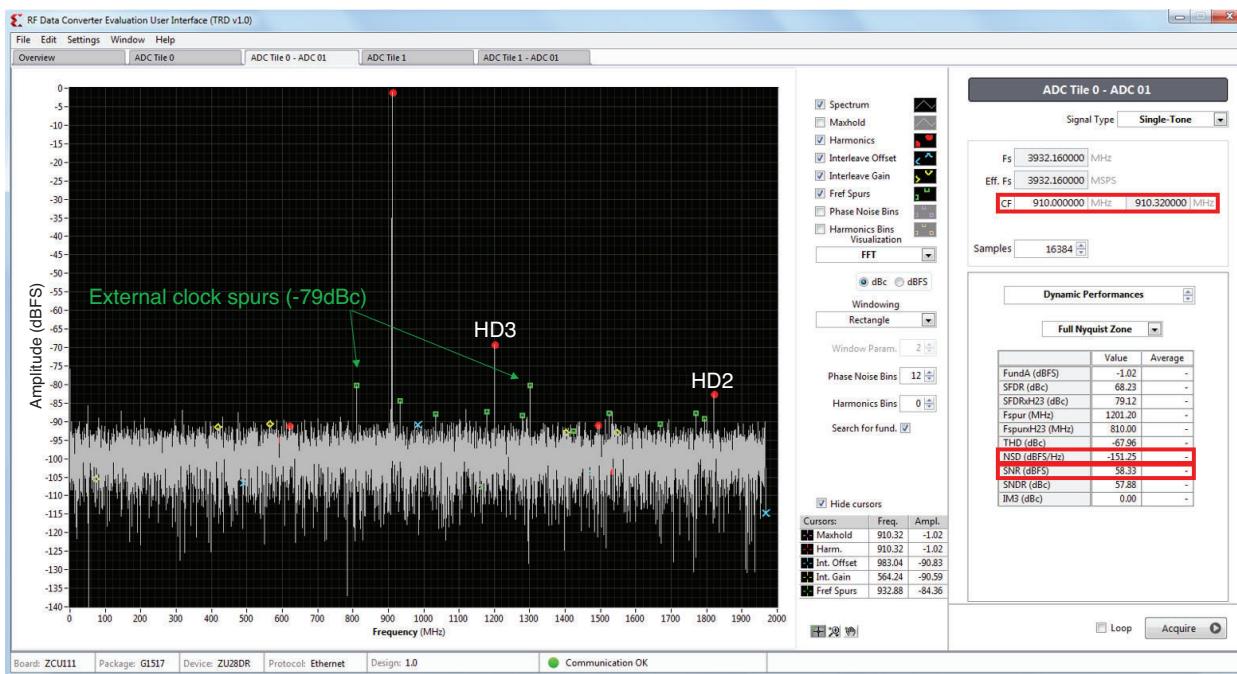
For non-ideal data converters, the NSD equation is

$$NSD_{(dBFS/Hz)} = - SNR_{measured(dBFS)} - 10\log_{10}\left(\frac{f_s}{2}\right)_{(Hz)} \quad Equation\ 11$$

The full-scale $SNR_{measured}$ in [Equation 11](#) should be obtained either by direct measurement or from the data sheet supplied by vendors. [Ref 6]

According to the Xilinx Zynq UltraScale+ RFSoC RF Data Converter Evaluation Tool shown in [Figure 7 \[Ref 6\]](#), 58.33_{dBFS} of measured SNR and -151.25dBFS/Hz of measured NSD are shown on the RF-ADC Performance Characteristics @ 3.93216GSPS sampling clock for $F_{out} = 900\text{MHz}$ sine wave at -1dBFS. Verifying this in the above equation,

$$\begin{aligned}\text{RF-ADC NSD}_{(\text{dBFS})} @ 900\text{MHz} &= - \text{SNR}_{\text{measured}(\text{dBFS})} - 10\log_{10}(f_s/2)(\text{Hz}) \\ &= -58.33\text{dBFS} - 10\log_{10}(3.93216\text{GSPS}/2) \\ &= -151.33\text{dBFS/Hz}\end{aligned}$$



WP509_07_12308

Figure 7: NSD Measurement of RF-ADC on the RF Data Converter Evaluation Tool @ 900MHz

Third-Order Intermodulation Distortion (IM3)

Any complex signal contains components at several frequencies simultaneously. Nonlinearity in the converter's transfer function not only causes distortion of a pure tone, it causes two or more signal frequencies to interact and produce intermodulation products. When this happens, the result is called intermodulation distortion, or IM3.

Typically, the "two-tone test" is commonly used to measure non-linear behavior (i.e., IM3) for a wide range of RF devices, especially data converters. For instance, a two-tone input signal (f_1, f_2) with small separation is injected into the RF device (i.e., the ADC), and an output that includes two tones at the exact same frequencies as the input signal is produced *if the ADC is perfectly linear*. For the non-linear ADC, however, $2f_1-f_2$ and $2f_2-f_1$ intermodulation distortion products, as well as nf_1 and nf_2 harmonic components, are generated. A two-tone test is illustrated in [Figure 8](#).

Some applications, especially those concerned with RF signal processing, are more sensitive to some modulation products than to others. For example, in RF applications, the third-order difference products $2f_1-f_2$ or $2f_2-f_1$ are important because they are closest to the input

frequencies, where other terms can be digitally filtered out. For this reason, terms other than IM3 are usually ignored where IMD is specified for RF applications.

IM3 can lead to serious issues in RF communication systems that create additional frequency components (called “spectral regrowth”) in bands adjacent to the modulated signals. In a receive path, spectral regrowth can cause out-of-band signals to interfere with the signal of interest. In a transmit path, on the other hand, bad IM3 can affect adjacent channels which then cannot pass the frequency mask of the wireless protocol. [Ref 3]

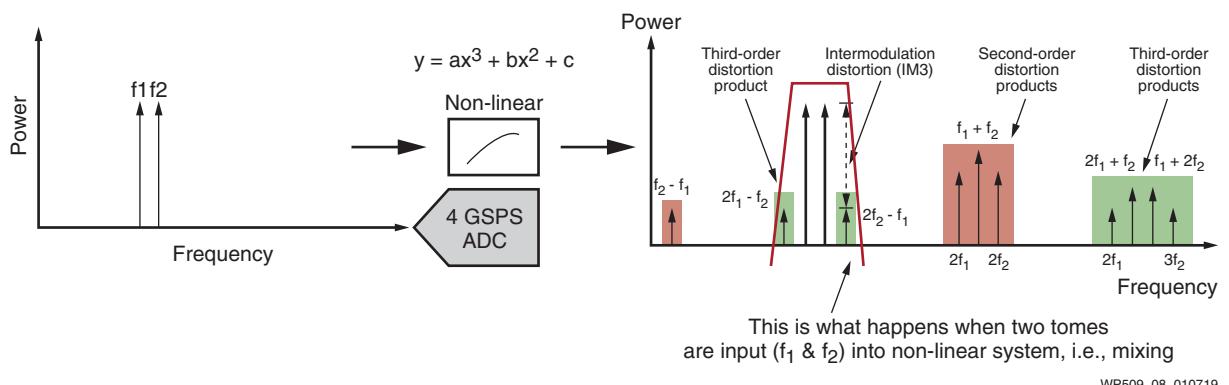


Figure 8: Graphical Depiction of IM3 in Non-Linear System

The superior IM3 performance of the Zynq UltraScale+ RFSoC RF-DAC at 900MHz input frequency with 20MHz spacing between two generated tones is -85.63dBc at both the $2f_1-f_2$ and $2f_2-f_1$ intermodulation distortion frequencies, with -7.26dBm input, as shown in Figure 9. For the Zynq UltraScale+ RFSoC RF-ADC IM3 measurement, two -7dBm inputs at 900MHz apart from 20MHz spacing from signal generators are used. The IM3 of RF-ADC is -78.08dBc is measured at the RF Evaluation Tool, as shown in Figure 10. Consequently, both RF-DAC and RF-ADC support excellent linearity in the two-tone distortion test, preventing creation of large new frequency components.

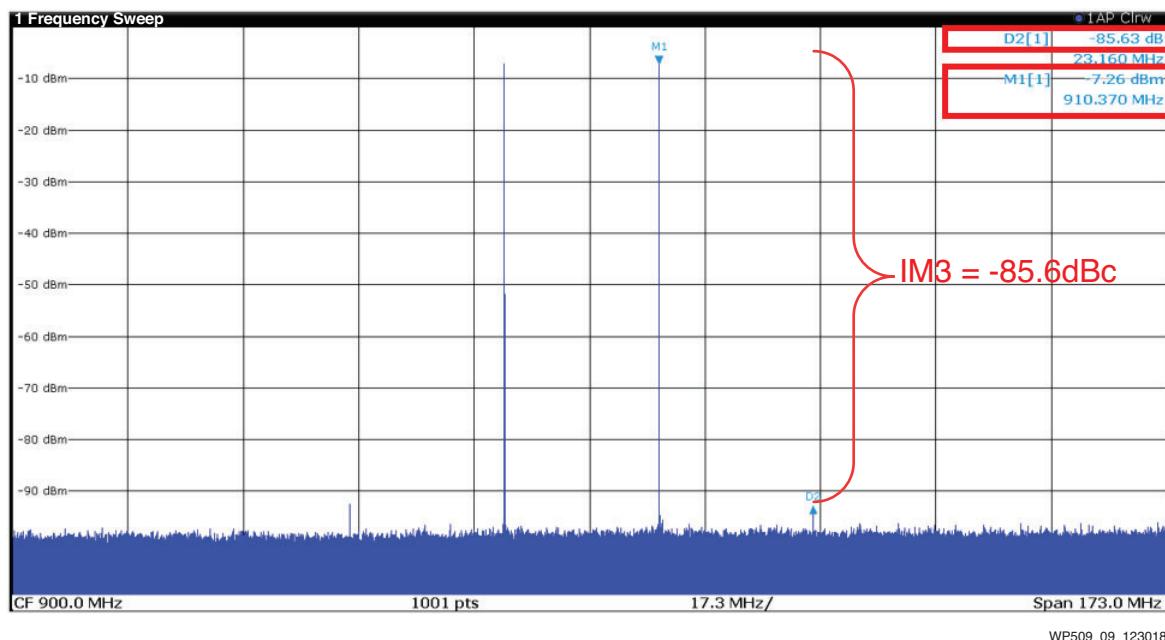


Figure 9: Zynq UltraScale+ RFSoC RF-DAC IM3 Measurement with Dual-Tone Input

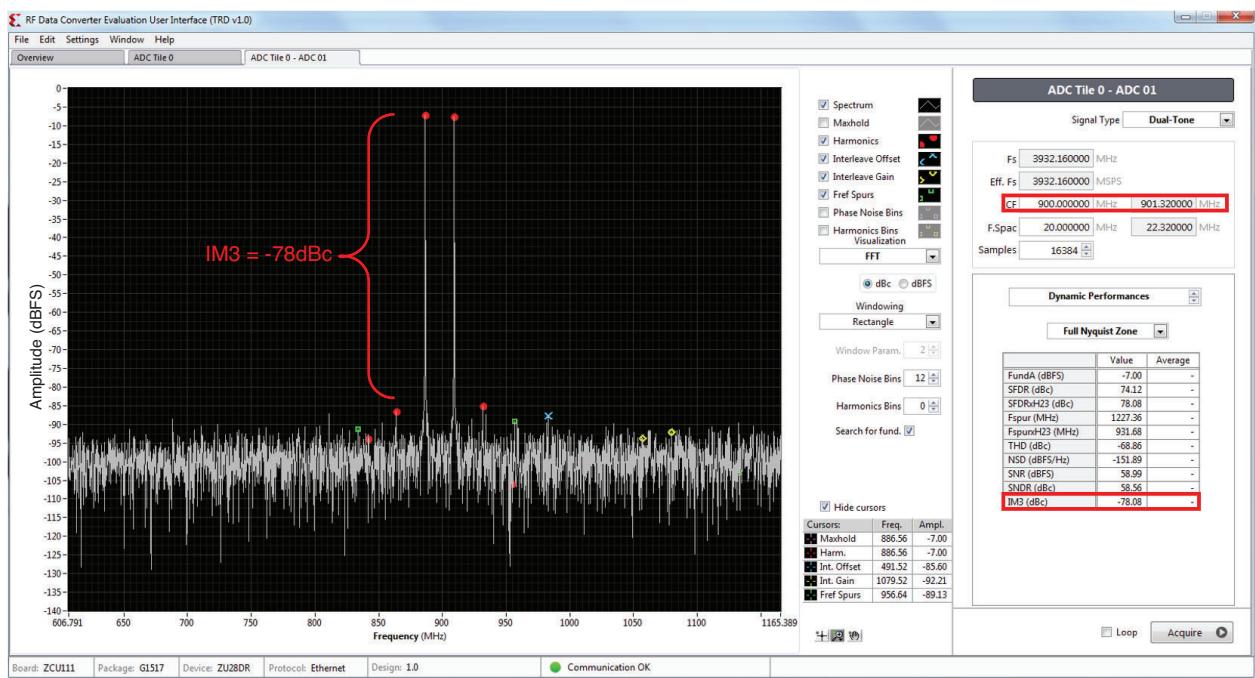


Figure 10: Zynq UltraScale+ RFSoC RF-ADC IM3 Measurement, Dual-Tone Input (RF Data Converter Evaluation Tool)

Adjacent Channel Leakage Ratio (ACLR)

As wireless demand has been increasing dramatically, the allocated frequency spectrum is getting crowded. Nowadays, the wireless infrastructure requires much greater data capacity and bandwidth to deliver IP services to more subscribers and mobile devices. While transmitting signals through an over-air interface, the power that leaks from a transmitted signal into adjacent channels can interfere with transmission in the adjoining channels and impair overall radio system performance.

ACLR is a key standards-compliant spectrum measurement designed for use in wireless radio systems such as 3GPP 5G, LTE, and W-CDMA. As shown in [Figure 11](#), it characterizes the ratio of modulated signal power versus power emitted or leaked into adjacent channels of the communication system. The ability to vary channel bandwidths and adjacent channel spacing is required within the context of various communication protocols. To measure ACLR of the device under test (DUT), a modulated signal generator or DAC is commonly utilized.

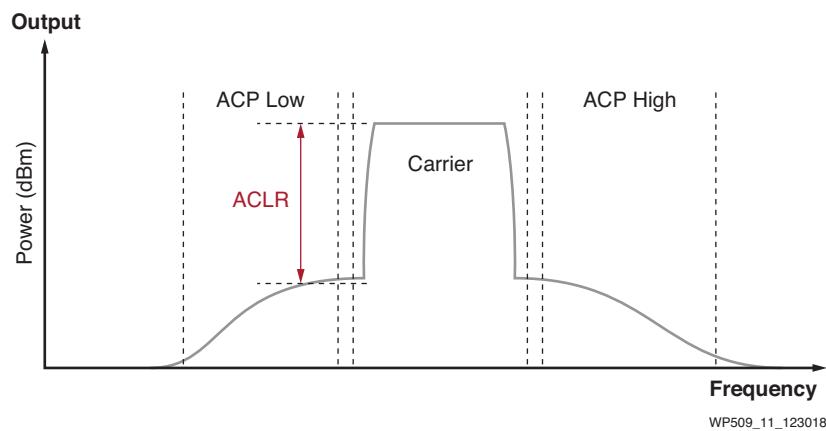
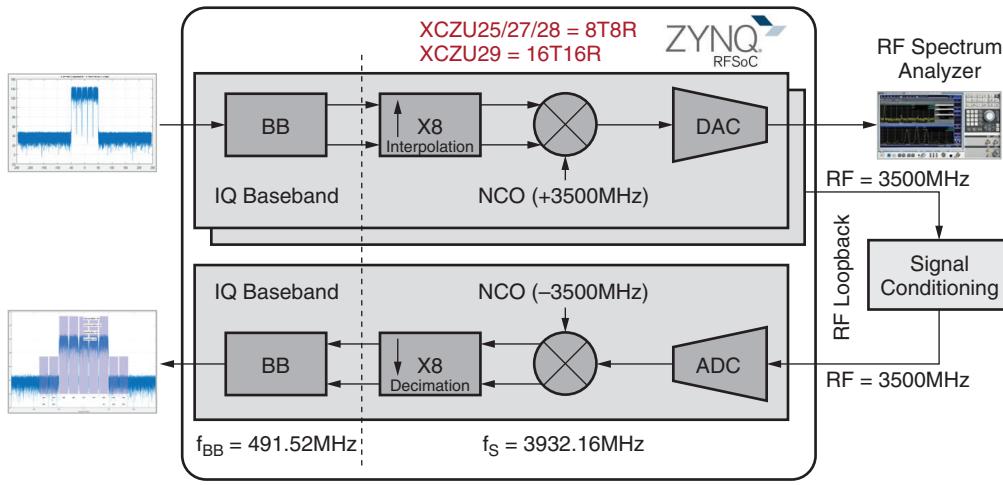


Figure 11: ACLR Graphical Illustration

The Zynq UltraScale+ RFSoC integrates either 8x8 or 16x16 DAC and ADC channels. To measure ACLR performance of both DAC and ADC, the test setup is easily configured in loopback mode.

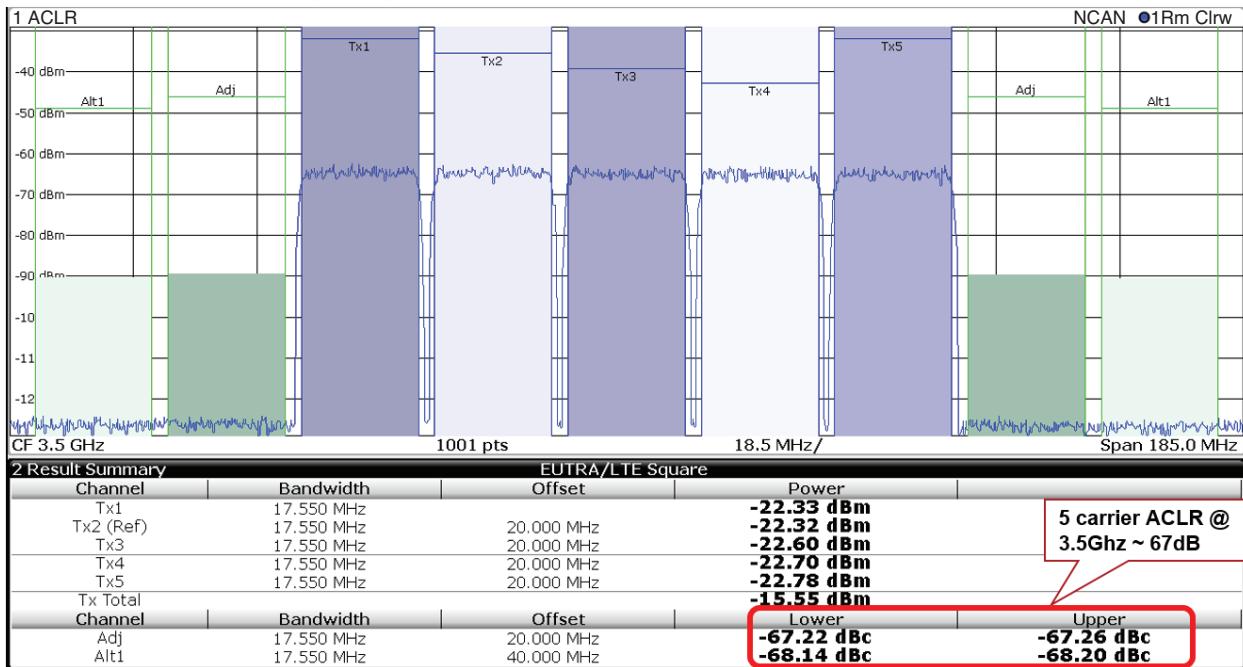
[Figure 12](#) illustrates the ACLR measurement use case. A band 42 IQ-modulated signal with 5x20MHz 64QAM LTE carriers is generated at digital baseband in the transmit path, interpolated 8x, and mixed up to 3,500 MHz in two DAC channels. One channel is connected to a frequency spectrum analyzer, while the other channel is looped back to the ADC through an external Mini-Circuits ZRL-3500+ amplifier. Then the 3,500MHz RF signal is decimated 8x and mixed down to baseband. For the clocking scheme, 3,932.16MHz is adopted as the RFSoC data converter sampling clock, while 491.52MHz is applied as the baseband sampling clock.



WP509_12_010719

Figure 12: Zynq UltraScale+ RFSoC ACLR Measurement Use Case

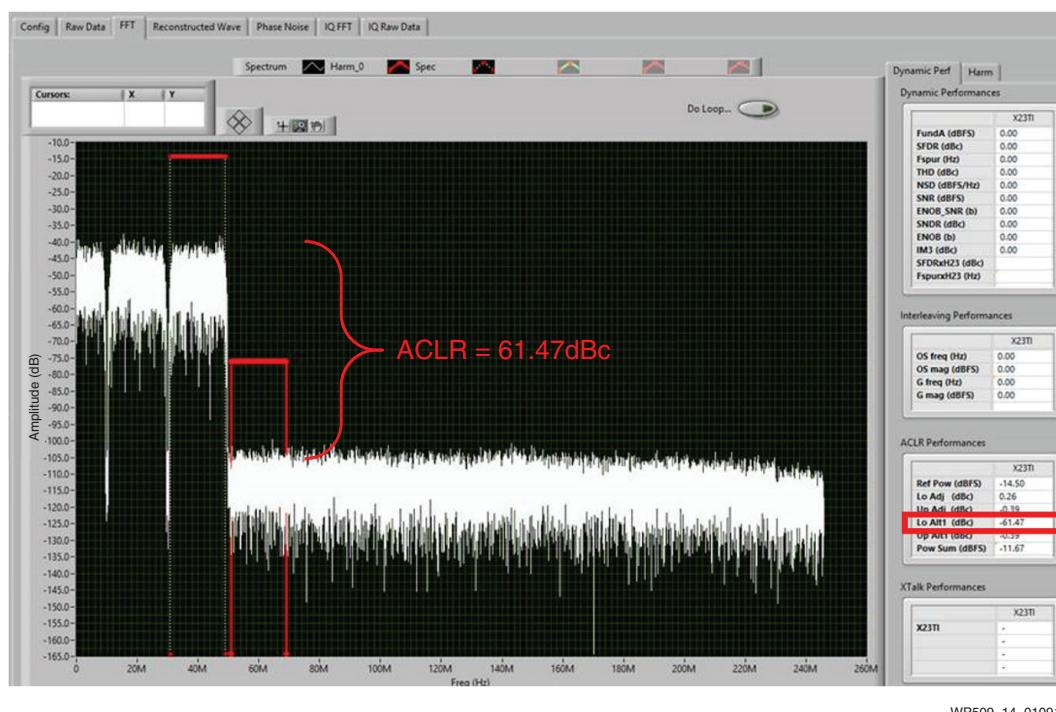
A Rohde & Schwarz FSW26 spectrum analyzer was used to analyze the dynamic performance of the DAC. Figure 13 shows the spectrum analyzer ACLR measurement for 5x20MHz multi-carrier in 64QAM modulation at 3,500MHz transmit output generated by the Zynq UltraScale+ RFSoC DAC with internal PLL sampled at 3,932.16MHz. With the 20MHz offset ("Adj" on the analyzer screen) from the Tx1 and Tx5 channels, ACLR of both upper and lower adjacent channels are about -67dBc. With the 40MHz offset ("Alt1" on the analyzer screen), both ACLRs are -68dBc.



WP509_13_123018

Figure 13: RF-DAC ACLR Measurement for 5x20MHz 64QAM Modulation @ 3,500MHz

For ACLR of the Zynq UltraScale+ RFSoC RF-ADC, 61.42dBc is measured in loopback configuration from DAC to ADC, as shown in Figure 14.



WP509_14_010919

Figure 14: RF-ADC ACLR for 5x20MHz 64QAM Modulation @ 3,500MHz (Loopback Mode)

According to the 3GPP 5G requirement [Ref 7] for a 5G NR base station, the ACLR emission limit of the overall system for transmit path is -45dB with respect to the carrier signal. Therefore, the Zynq UltraScale+ RFSoC ACLR performance (see Xilinx Data Sheet DS926) [Ref 8] is superior, leaving plenty of margin for the rest of the system (e.g., the power amplifier) to reduce design challenges.

Summary

SNR and ENOB are common parameters used to characterize and evaluate data converters when set up with a sinusoidal input over full Nyquist bandwidth. However, these and other legacy metrics are deprecated for direct-sampling applications because the RF data converters employed in such designs are not required to operate over the full Nyquist bandwidth. Instead, the NSD, IM3, and ACLR parameters are more relevant to the evaluation of devices used in direct-sampling designs. In such use cases, it is more important to quantify the amount of data-converter noise falling into the band(s) of interest. Thus, different RF applications need different sets of parametric specifications to accurately evaluate system design performance. For both narrow-band and more traditional wide-band applications, the accurate measurement (with use-appropriate metrics) of in-band noise, spurious signals, and distortion is required to select the right RF data-handling solution.

With the release of Zynq UltraScale+ RFSoCs, featuring integrated multichannel direct-sampling RF-ADCs, a family of Xilinx devices is now available to fulfill the most demanding RF processing requirements, including the implementation of a complete software-defined radio (SDR) on a single device—another industry-first achievement for Xilinx.

For more information, go to: www.xilinx.com/RFSoC.

References

1. Xilinx® Zynq® UltraScale+™ RFSoC ZCU111: [RF Data Converter Evaluation Tool](#) (website download page).
2. Carusone, Tony Chan; Johns, David A.; Martin, Kenneth W.: [Analog Integrated Circuit Design](#) (2nd ed., 2012). Hoboken, NJ: John Wiley & Sons, Inc.
3. National Instruments / White Paper, [Understanding Frequency Performance Specifications](#) (2017).
4. National Semiconductor / Kulchycki, Scott: [Software Defined Radio: Don't Talk to Me about ENOBs, Part 1](#); [Part 2](#). *EETimes RF & Microwave Designline* (2010).
5. Huawei Technologies Co., Ltd. / Public Policy Position: [5G Spectrum](#) (2017).
6. Analog Devices / Beavers, Ian: [Noise Spectral Density: A New ADC Metric?](#)
7. ETSI / Technical Specification, 3GPP TS 38.101-1 v15.2.0 Release 15: "[5G; NR; User Equipment \(UE\) Radio Transmission and Reception](#)" (2018).
8. Xilinx Data Sheet [DS926](#), *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics*

APPENDIX

Derivation of the Signal-to-Noise Equation $SNR = 6.02N + 1.76\text{dB}$:

Consider the quantization errors V_Q in an ideal ADC converter, as shown in Figure 15.

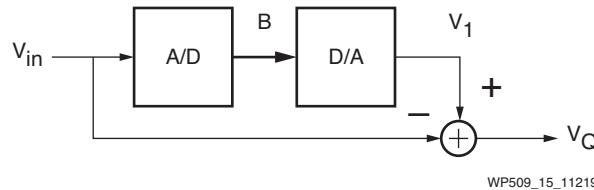


Figure 15: A Setup to Investigate Quantization Noise

$$V_Q = V_1 - V_{in} ;$$

$$V_1 = V_{in} + V_Q$$

where V_1 is the quantized signal and V_{in} is the input signal of an ideal ADC.

Assume V_{in} to be a ramp input signal; thus, the result V_1 is a staircase due to the output from the DAC, as shown in Figure 16.[Ref 2]

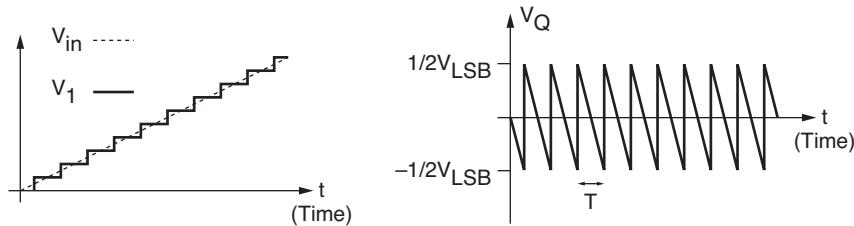


Figure 16: Relationship between V_1 , V_{in} , and V_Q , based on setup in Figure 15

V_Q is the result of the difference between V_{in} and V_1 , and the RMS value of the noise signal $V_{Q(rms)}$ is given by:

$$\begin{aligned} V_{Q(rms)} &= \sqrt{\left[\frac{1}{T} \int_{-T/2}^{T/2} V_Q^2 dt \right]} \\ &= \sqrt{\left[\frac{1}{T} \int_{-T/2}^{T/2} V_{LSB}^2 \left(\frac{-t}{T} \right)^2 dt \right]} \\ &= \sqrt{\left[\frac{V_{LSB}^2}{T^3} \left(\frac{T^3}{3} \Big|_{-T/2}^{T/2} \right) \right]} \end{aligned} \quad \text{Equation 12}$$

The RMS quantization noise measured over the full Nyquist bandwidth from DC to $fs/2$ is given by:

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \quad \text{Equation 13}$$

For an ideal data converter, SNR is given by:

$$SNR = 20\log_{10}\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) \quad Equation\ 14$$

Assume the input (V_{in}) is a sinusoidal wave. Peak amplitude is $V_{ref}/2$.

$$\begin{aligned} SNR &= 20\log_{10}\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) \\ &= 20\log_{10}\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right) \end{aligned} \quad Equation\ 15$$

Substituting $V_{LSB} \equiv \frac{V_{ref}}{2^N}$ into Equation 15,

$$\begin{aligned} &= 20\log_{10}\left(\frac{\frac{V_{ref}/(2\sqrt{2})}{V_{ref}/(\sqrt{12})}}{\frac{2^N}{(\sqrt{12})}}\right) \\ &= 20\log_{10}\left(2^N \times \frac{\sqrt{12}}{\sqrt{8}}\right) \\ &= (6.02N + 1.76) \text{ dB} \quad \text{over the Nyquist bandwidth.} \end{aligned} \quad Equation\ 16$$

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/20/2019	1.0	Initial Xilinx release.

Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>.

Automotive Applications Disclaimer

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.