WP498 (v1.1) May 29, 2018

Integrated SD-FEC in Zynq UltraScale+ RFSoCs for Higher Throughput and Power Efficiency

By: Ambrose Finnerty and Martin Lee

By introducing the industry's first integrated and configurable soft-decision forward error correction (SD-FEC) IP block, the Xilinx® Zynq® UltraScale+™ RFSoC enables more efficient, higher throughput, lower power LDPC and Turbo codec solutions for a wide range of data communications applications.

ABSTRACT

Within data communications, in both Wireless and Cable applications, maintaining transmission reliability is a vital component in providing the required quality of the overall system. A high-performance SD-FEC (i.e., >1Gb/s) is a key building block used to enable these systems to function within non-ideal environments. With the Zynq UltraScale+ RFSoC, Xilinx is introducing an integrated SD-FEC IP block that is fully compliant with a range of industry LDPC and LTE Turbo code standards.

Challenges in Reliable Data Transmission

Modern data communication generates huge amounts of data that is often moved between nodes across different types of physical channels. An example of a generic data communication system is shown in Figure 1.

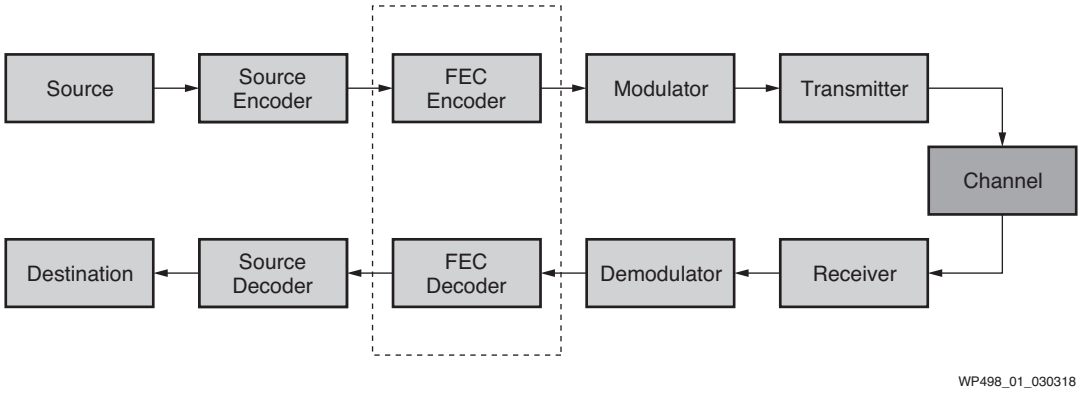

Figure 1: **Typical Data Communication System Diagram**

In all instances, these data channels are not perfect and are subject to varying degrees of quality, leading to errors being present in the received data. Typical channels, including 4G/5G wireless [Ref 1], DOCSIS cable [Ref 2], and Microwave Backhaul [Ref 3], are imperfect, so system engineers have to design these systems to meet pre-defined performance criteria as evaluated by such metrics as bit error rate (BER).

The use of robust forward error correction (FEC) algorithms, such as low-density parity check (LDPC) [Ref 4] and Turbo SD-FECs [Ref 5], enable system engineers to design advanced communication systems that approach the Shannon capacity [Ref 6] of the channel. The implementation of these SD-FEC coding algorithms is not trivial and often requires special domain knowledge.

FPGAs are often used to implement these SD-FEC algorithms because an FPGA's high-performance programmable logic, memory, DSP, I/Os, and SerDes are ideally suited to the demanding number of variable precision arithmetic operations and high memory bandwidth requirements. However, as the system requirements are pushed further to support multi-gigabit data rates, performance, power, and cost become significant design factors, and soft implementations can be sub-optimal compared to integrated solutions.

These SD-FEC algorithms are very computationally intensive and require a lot of resources when implementing them in the FPGA's programmable logic. With the introduction of an integrated SD-FEC IP inside some of the Zynq UltraScale+ RFSoC devices [Ref 7], Xilinx has enabled:

- Performance and throughput bottleneck to be alleviated
  - ~3Gb/s peak LDPC decode throughput
- Large reduction in resources
  - Savings of ~100k LUTs per SD-FEC instance
- Massive power savings
  - 80% power reduction by moving to an integrated solution

Zynq UltraScale+ RFSoCs offer all of this while retaining FPGA flexibility and programmability. Thus, designers can focus on product differentiation and the overall optimization of their system.

Evolution to Soft-Decision FEC and Iterative Decoding

FEC requirements can be divided into different categories: voice, video conferencing, replayed video, and non-real-time data (see Table 1). In LTE [Ref 8] for example, Quality of Service (QoS) is an important part of network planning and design when deploying 4G/LTE fixed broadband wireless for data and voice services.

Table 1: **BER for Different Services**

Service	BER Tolerance	Delay Tolerance	Notes
Voice	$\sim 10^{-3}$	100ms	Guaranteed bit rate
Video Conferencing	$\sim 10^{-4}$	150ms	Guaranteed bit rate
Replayed Video	$\sim 10^{-5}$	300ms	Non-guaranteed bit rate
Non-real-time Data	$< \sim 10^{-7}$	>300ms	Non-guaranteed bit rate

For a long time, the use of concatenated Reed-Solomon (RS) and convolutional coding with Viterbi decoding [Ref 9] have been used successfully. The adoption of soft decision [Ref 10] decoding made this scheme even more efficient as it gives an extra ~3dB coding gain [Ref 11]. A 3dB coding gain means a signal can travel twice the distance in a channel for the same performance.

However, with the evolution to more complex modulation schemes, such as multi-level QAM (up to 4096-QAM for DOCSIS3.1), useful BER for such systems is increased for a given energy per bit to noise power spectral density ratio (Eb/No) [Ref 12]. Therefore, the demodulated bits are more susceptible to channel degradations. Moving to more capable SD-FEC schemes enables these systems to meet their performance requirements.

To meet the native BER needs across varying QoS requirements (voice, data, video, etc.), as shown in Table 1, iterative decoding [Ref 13] schemes have become popular.

Turbo and LDPC codes are iterative codes and generally require more operations per bit to get the best performance compared to the Viterbi decoding for convolutional codes. They enable systems to push towards the theoretical Shannon limit [Ref 14]. These coding schemes have reached maturity and are being adopted in many applications, including 4G/5G wireless and DOCSIS 3.1, where they are now considered practical to implement.

Xilinx Introduces SD-FEC in Zynq UltraScale+ RFSoCs

To provide coverage for a wide variety of applications, integrated SD-FEC blocks have been introduced in the Zynq UltraScale+ RFSoC devices. The SD-FEC blocks are integrated with and without multi-giga-sample RF data converters [Ref 15] into an SoC architecture, including an ARM® Cortex™-A53 processor. These Xilinx devices offer a feature-rich platform including DSPs, general-purpose processor (GPPs), programmable logic, and optimized RF signal-processing blocks (i.e., DUCs and DDCs).

Combined with the high-speed RF data converters, the SD-FEC enabled Zynq UltraScale+ RFSoCs provide a highly flexible solution for applications like a Cable/DOCSIS 3.1 Remote PHY, offering the opportunity to create a full duplex solution in a single device.

Similarly for 5G New Radio wireless baseband systems, requirements for high data throughput, low-latency, and improved coding performance results in greater general programmable logic resources to implement the required SD-FEC algorithms within a programmable logic based solution. More resources, i.e., LUTs, memories, and routing, in conjunction with faster designs translate into greater power consumption and ultimately a higher solution cost. Having eight SD-FEC integrated blocks available in a single device makes the overall system throughput achievable in a single Zynq UltraScale+ RFSoC.

Along with the RF data converters and SD-FEC, Xilinx has a history of integrating many IP blocks, including PCIe, Interlaken, and Ethernet MAC into the Xilinx devices. In the case of the SD-FEC, integrating this IP block brings the following advantages.

- Reduces programmable logic resources
- Saves power
- Reduces development time
  - Pre-verified IP—functionally and timing
  - Software and tools supported flows
- Predictably greater performance compared to a soft implementation
  - High throughput with low latency
- Configurability leading to flexibility

All of these advantages lead to a lower cost solution.

Xilinx SD-FEC along with the RFSoC architecture target, but not exclusively, the following applications:

- 4G/5G wireless (both baseband and backhaul)
  - Turbo codes used in LTE and LDPC in Wi-Fi and 5G New Radio
- Cable access
  - LDPC codes used in DOCSIS 3.1 Remote PHY
- Microwave links

SD-FEC IP Overview

A high-level view of Xilinx integrated SD-FEC IP is shown in Figure 2.

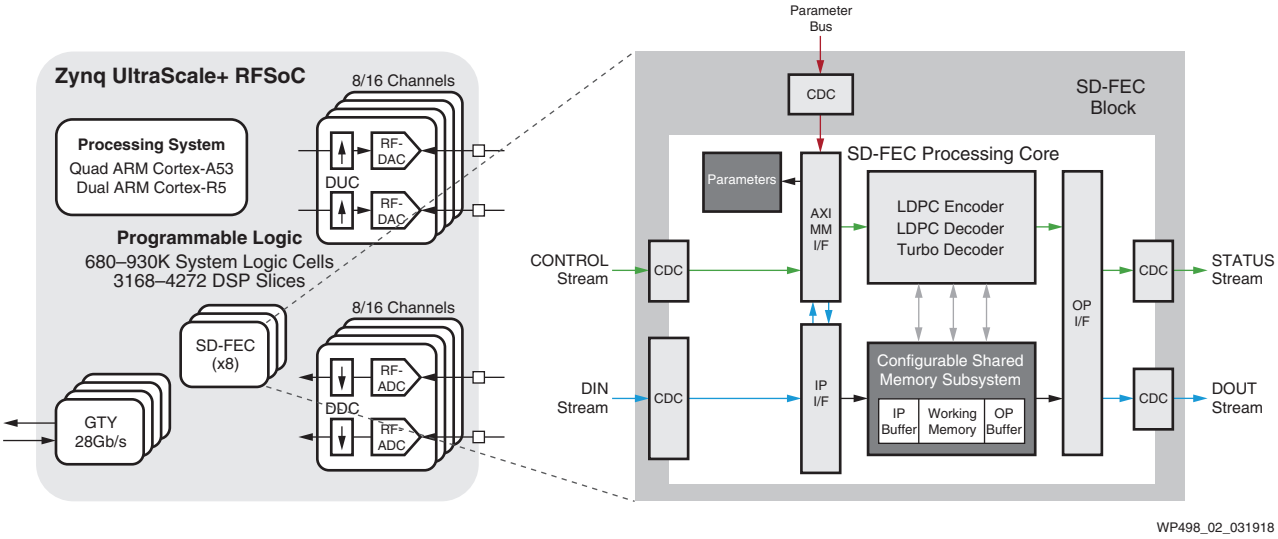

Figure 2: **SD-FEC Block Diagram**

The SD-FEC block has three modes of operation with only one mode enabled at any one time:

- LDPC encoding
- LDPC decoding
- Turbo decoding (LTE)

These three modes were selected because the underlining algorithms have reached a maturity that designers are comfortable with in terms of attributes and known implementation trade-offs.

LDPC Description

LDPC encode or decode is supported over a range of customer specified Quasi-Cyclic (QC) codes. Even though the SD-FEC is an integrated IP, the SD-FEC block is highly configurable, and up to 128 codes can be stored in the parameter memory. Codes can be selected on a block-by-block basis, and the ability to add custom codes makes the block extremely flexible. The SD-FEC is a soft-decision decoder with iterative decoding and has the ability to early terminate and save power.

Turbo Description

Only Turbo decode is supported for 4G LTE-Advanced and LTE-Pro applications. Similar to the LDPC decoder, iterative decoding is supported with early termination available.

Throughput

The peak throughput for the SD-FEC is:

- ~1.8Gb/s Turbo decode at 6 iterations
- ~3.0Gb/s for LDPC decode at 8 iterations
- ~20.0Gb/s for LDPC encode

Throughputs vary across codes and applications, i.e., DOCSIS 3.1 to 5G New Radio. Refer to the *Soft-Decision FEC Integrated Block* product guide [Ref 16] for more information on specific throughput capabilities and other performance information, including BER performance plots across supported codes and applications.

System Throughput

Some devices in the Zynq UltraScale+ RFSoC family contain eight SD-FEC integrated blocks, which enables system throughputs for the following use cases. See Table 2.

Table 2: **Peak System Throughput**

Mode	# SD-FEC Decoders	# SD-FEC Encoders	Peak Throughputs Decoder	Peak Throughputs Encoder
Turbo	4	N/A	>7.0Gb/s	N/A
LDPC	6	2	>18.0Gb/s	>40.0Gb/s
LDPC	0	8	N/A	>162.0Gb/s

The maximum throughput achievable with the SD-FEC depends on the chosen code, code rate, and number of iterations of the decoder when running 667MHz F_{MAX}. Table 2 shows the peak system configurations allowed. Subsets of these are also supported, e.g., four LDPC decoders with four LDPC encoders.

Practical Use Case with SD-FEC (5G Wireless)

Zynq UltraScale+ RFSoCs are ideal for 5G wireless applications and provide a complete platform solution. See Figure 3.

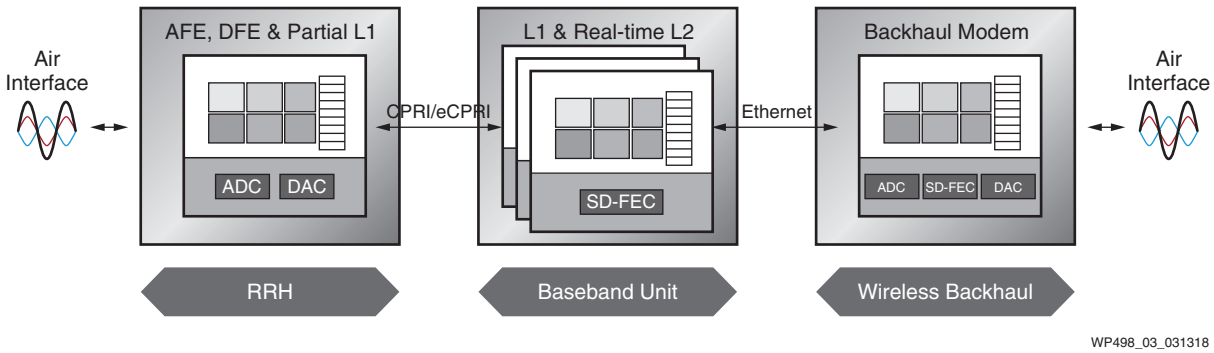

Figure 3: **Zynq UltraScale+ RFSoC Enables a 5G Wireless Platform Solution**

For wireless backhaul, the Zynq UltraScale+ RFSoC family has a device with both integrated RF-ADCs/DACs and SD-FEC blocks. Additionally for the Remote Radio Head (RRH), devices with the RF-ADCs/DACs but no SD-FEC capabilities can meet the customer's needs.

Finally, within the baseband unit (BBU), there is no analog requirement but there is a large encode and decode requirement in layer 1 (L1). Within the Zynq UltraScale+ family, Xilinx has provided an SD-FEC only device, i.e., a device with no integrated data converters. This device is ideally placed to meet the processing requirements within the baseband unit of a 5G wireless system. In particular, the solution is scalable, allowing a single device to meet the overall system throughput for both LDPC encoding and LDPC decoding in L1.

Wireless Baseband Unit (BBU)

To understand the value the integrated SD-FEC offers to a 4G/5G wireless baseband unit solution, it is necessary to equate the SD-FEC advantages to a use case.

Reduces Programmable Logic Resources

It is widely accepted that LDPC, and Turbo decoders in particular, require a large amount of resources when implemented as soft IP blocks in programmable logic. The resources are pushed further when implementing an SD-FEC solution. Encoders are less resource intensive but still can be quite considerable. See Table 3.

Table 3: **Programmable Logic Resource Usage for Soft IP Solution**

Soft IP	LUTs	Flip-Flops	Block RAM
LDPC Encoder	~14.5k	~12.5k	~24
LDPC Decoder	~58.5k	~60.5k	~125
Turbo Decoder(1)	~107k	~171.5k	~246

1. Turbo decoder IP resources scaled to accommodate for levels of parallelism in both architectures.

The SD-FEC supports all the above modes in one integrated IP block, meaning a direct comparison to the above resources does not provide the complete picture—a true reflection shows even greater resource savings when comparing all SD-FEC modes to a similar soft implementation.

Single instances of these blocks might not seem too costly, but for most systems—and this is true for 4G/5G baseband L1 applications—the only way to achieve the system throughput requirements is through multiple instances of these Turbo decoders and LDPC decoders and encoders. The instantiation of multiple instances uses substantial amounts of the programmable logic. But using an integrated solution frees these resources and makes them available for other L1 or L2 processing.

For this reason, it is not uncommon to use multiple PCBs to build the complete L1 system for a pre-5G and/or 5G system, especially where multiple carriers might be required, i.e., one PCB per carrier due to the requirement for multiple FPGAs to implement all the FEC encoding and decoding. See Figure 4.

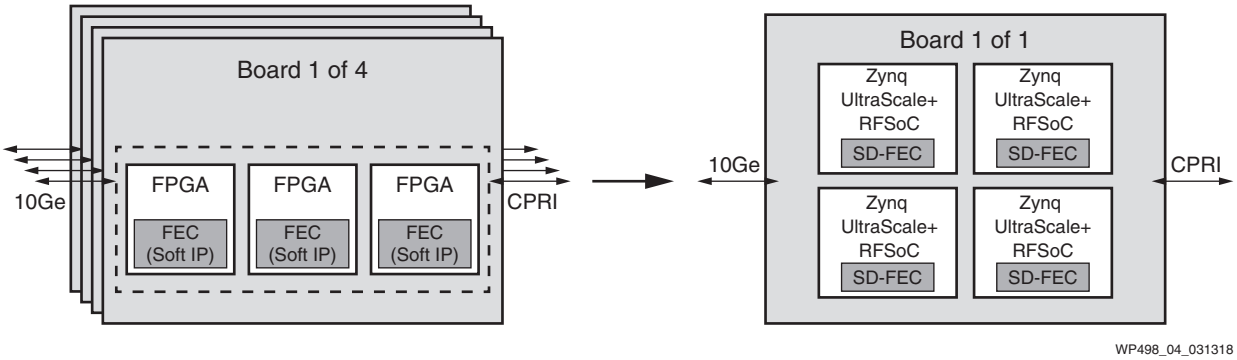

Figure 4: **SD-FEC Enables Reduction in PCB Count**

However, using the Zynq UltraScale+ RFSoC, with eight integrated SD-FEC blocks, enables massive reductions in the amount of resources required, ultimately reducing the overall number of devices required to perform all the FEC processing. In some cases, this can result in using fewer PCBs for the complete solution, giving an overall smaller solution footprint and lowering the cost of deployment.

Saves Power

Within most applications today, power and thermal requirements are huge considerations and need to be designed for from the outset of a project. The Zynq UltraScale+ RFSoCs, built with a proven 16nm architecture, integrate RF-data converters, and multiple SD-FEC blocks, lend themselves very favorably to providing power savings versus alternative solutions in the market.

In the case of the 5G baseband use case, the Zynq UltraScale+ RFSoC enabled solution reduces the overall system power. The reduction in the number of devices and PCBs required to build the complete solution dramatically reduces the overall power.

From a throughput level, it is important to compare a soft IP to the integrated SD-FEC block in the Zynq UltraScale+ RFSoC. For example, in a design that requires an LDPC decode for a maximum throughput of 2Gb/s, building it on a non-RFSoC device that is similarly scaled to the ZU21DR in the Zynq UltraScale+ RFSoC family, i.e., ~1M system logic cell (425k LUTs), two LDPC decoder IPs are required, running at ~300MHz, using 120k LUTs or 28% of the programmable logic resources. For the FEC portion alone, the dynamic power consumption is in the region of 6.3W.

Working to the same requirement of 2Gb/s in the ZU21DR device using 1 SD-FEC block and no programmable logic, the dynamic power consumption greatly decreases to ~1.2W, i.e., ~80% power saving. See Figure 5.

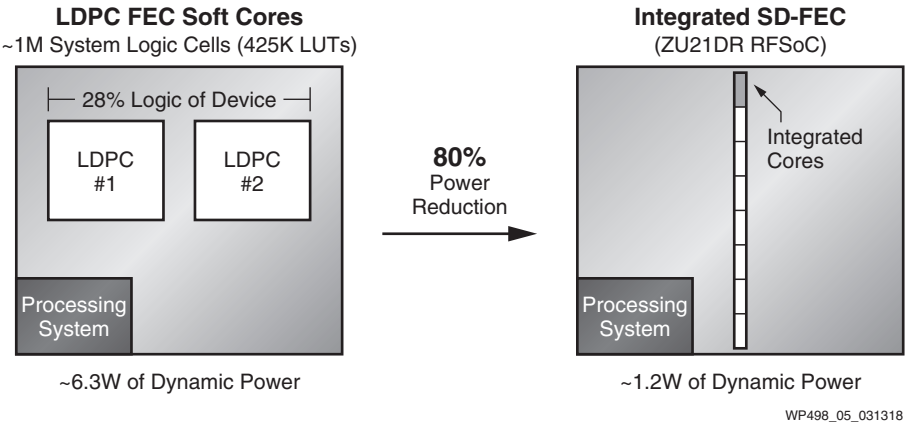

Figure 5: **Power Comparison of Integrated SD-FEC versus Soft LDPC Decoder**

This example is for a simple use case comparing only a soft LDPC decode implementation to the integrated SD-FEC block, but as mentioned earlier, this is not a like-for-like comparison because the SD-FEC supports further modes in a single block—but it is a useful comparison for visualization purposes.

Reduces Development Time

The integrated SD-FEC block means that the functions are implemented in ASIC-style gates inside the device. This by definition is more area and power efficient, but also means that the SD-FEC is a pre-verified block. Standard compliant functionality and timing are guaranteed within the block, meaning no block-level verification or timing closure is needed. The reduced R&D effort leads to quicker implementation of the FEC portions of the application and simplifies the overall design. This enables users to meet their aggressive time to market (TTM) schedules.

Predictably Greater Performance Compared to a Soft Implementation

Since the SD-FEC block is an ASIC-like solution, a higher F_{MAX} can be achieved for the block compared to a soft IP core implementation in the FPGA's programmable logic.

The SD-FEC core clock can run at 667MHz for all device speed grades. Overall throughput for an individual SD-FEC block is directly proportionate to the speed at which the block runs, so it is possible to achieve higher and predictable throughput compared to a soft implementation, where achieving such high clock rates is much more difficult. Most soft implementations are likely to achieve 300–400MHz F_{MAX} depending on the device speed grade. In the case of the slowest speed grades, the SD-FEC with F_{MAX} of 667MHz can provide 2X the performance of a soft implementation.

Configurability Leads to Flexibility

The SD-FEC integrated block is highly configurable, allowing Turbo decode, LDPC encode, or LDPC decode. In the case of LDPC encode and decode, preset codes are available to support 5G New Radio, DOCSIS 3.1, and Wi-Fi, but it is also possible to program the SD-FEC block for custom LDPC codes.

This code configurability leads to a very flexible solution, allowing the SD-FEC to support emerging standards at a much earlier stage than an ASIC solution, which needs to wait until the standard has been finalized. The configurability allows both prototyping and production solutions to be developed ahead of a final standard definition.

This configurability within the SD-FEC block itself is extended further by having the additional flexibility in the programmable logic to pre-process the data prior to feeding the decoders but also to enable an SD-FEC controller for dynamic code configuration within the programmable logic. This is particularly advantageous with 5G New Radio due to the large volume of LDPC codes defined in the current revision of the 3GPP standard [Ref 17]. The Xilinx SD-FEC IP wrapper core available in Vivado IP Catalog provides a programmable logic 5G controller for these applications.

Lower Cost Solution

Cost is the constant concern for all programs, with the pressure always to minimize the total cost, and constantly pushing to reduce the system costs from one revision to the next. The Zynq UltraScale+ RFSoC platform enables cost savings by way of integration.

The integration of the RF data converters reduces the need for discrete data converters on the PCB along with the JESD requirements, dramatically reducing the number of components required on final PCBs for deployment.

The 5G baseband use case from earlier in this white paper illustrates the dramatic reduction in FPGA resources and the R&D effort enabled by the integrated SD-FEC block. The integration also reduces the requirement for multiple FPGAs to implement L1 baseband FEC algorithms. In some applications, it can also reduce the need for additional PCBs, further simplifying the system design, but also reducing the overall cost of the solution as a result.

The reduction in development and shortening of the time to market for those applications can further reduce the overall cost of the program.

Conclusion

Xilinx has delivered the industry's first integrated, configurable SD-FEC block in a Zynq UltraScale+ RFSoC. The SD-FEC offers huge advantages in multiple applications in the communications space, both in wireless and cable applications.

In Practical Use Case with SD-FEC (5G Wireless), it was shown how the SD-FEC enables resource and component savings. These resource reductions lead to large power savings for individual FEC algorithm implementations. They can even scale to even larger savings at the system level, where large throughput requirements lead to multiple SD-FEC blocks being required for the complete solution.

The ASIC-like SD-FEC block is pre-verified and achieves greater throughput, lower latency, and lower power than a soft implementation. The ability to support Turbo decoding for LTE and LTE-A applications make it a low power solution for 4G and pre-5G systems.

With LDPC support for both decode and encode, it is possible to support applications like 5G baseband and backhaul platforms in the wireless market. In addition to the RF-ADCs/DACs found in the Zynq UltraScale+ RFSoC (ZU28DR) family, the SD-FEC provides an attractive solution for remote PHYs in the DOCSIS 3.1 standard.

All the advantages highlighted in this white paper show how the Zynq UltraScale+ RFSoC architecture, incorporating multiple SD-FEC integrated blocks, can provide huge benefits to applications in the wireless and cable markets where performance, flexibility, power, time to market, and cost are key.

References

1. Gibson, Jerry D. 2013. *Mobile Communications Handbook, Third Edition: Edition 3*, CRC Press.
2. CableLabs website: http://www.cablelabs.com/innovations/docsis3-1/.
3. Xilinx website: https://www.xilinx.com/applications/wireless-communications/wireless-backhaul.html.
4. Johnson, Sarah J. "Introducing Low-Density Parity-Check Codes." School of Electrical Engineering and Computer Science. The University of Newcastle Australia: https://pdfs.semanticscholar.org/657c/5be8e9af37dea31e357cda636e123ba03411.pdf.
5. Studer, C., C. Benkeser, S. Belfanti, and Q. Huang, 2011. "Design and Implementation of a Parallel Turbo-Decoder ASIC for 3GPP-LTE." IEEE Journal of Solid-State Circuits. http://www.csl.cornell.edu/~studer/papers/11JSSC-turbo.pdf.
6. Viswanathan, M. *Simulation of Digital Communication Systems using MATLAB*. https://www.gaussianwaves.com/2008/04/channel-capacity/.
7. Xilinx website: https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html.
8. Dahlman, Erik, et al. 2013. *4G: LTE/LTE-Advanced for Mobile Broadband, Second Edition*. Academic Press.
9. Hagenauer, J., P. Hoeher, Nov. 1989. "A Viterbi Algorithm with Soft-decision Outputs and Its Applications. Proc." IEEE GLOBECOM, pp. 47.11-47.17, Dallas, TX.
10. Jose R., Ameenudeen Pe. "Analysis of Hard Decision and Soft Decision Decoding Algorithms of LDPC Codes in AWGN." http://ieeexplore.ieee.org/document/7154744/?arnumber=7154744&punumber%3D7140196%26filter%3DAND(p_IS_Number:7154658)%26pageNumber%3D4
11. "Coding gain" entry. Wikipedia. https://en.wikipedia.org/wiki/Coding_gain.
12. "E_b/N_o" entry. Wikipedia. https://en.wikipedia.org/wiki/Eb/N0.
13. Guruswami, V. 2006. "Iterative Decoding of Low-Density Parity Check Codes." https://www.cs.cmu.edu/~venkatg/pubs/papers/ldpc.pdf.
14. "Noisy-channel coding theorem" entry. Wikipedia. https://en.wikipedia.org/wiki/Noisy-channel_coding_theorem.
15. Xilinx white paper. *All Programmable RF-Sampling Solutions*. https://www.xilinx.com/support/documentation/white_papers/wp489-rfsampling-solutions.pdf.
16. Xilinx user guide. *Soft-Decision FEC Integrated Block v1.1, LogiCore IP Product Guide*. https://www.xilinx.com/cgi-bin/docs/ipdoc?c=sd_fec;v=latest;d=pg256-sdfec-integrated-block.pdf
17. NR; "Multiplexing and channel coding (Release 15)", 3GPP TS38.212 v1.1.1 (2017-11), R1-1719225.zip. http://www.3gpp.org/ftp//Specs/archive/38_series/38.212/

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/29/2018	1.1	Updated Throughput with reference to Xilinx user guide. Updated Configurability Leads to Flexibility.
03/29/2018	1.0	Initial Xilinx release.

Disclaimer

Automotive Applications Disclaimer