RF Data Converter Interface

User Guide

UG1309 (v1.4) October 27, 2021

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
10/27/2021 Version 1.4	
Chapter 1: Introduction	Added Zynq UltraScale+ RFSoC DFE device.
Window Menu Options and Window Menu Options	Updated MultiView option description and the MultiView RF-ADC Time Domain figure.
RF-DAC Settings	Updated Decoder Mode, Inverse Sinc Settings, and Current.
Clock Distribution (Gen 3) and Clock Distribution (Gen 3)	Removed Output Divider (M) option and updated Tile Status Based on Clock Distribution figure.
Selecting the Hardware Target and Bitstream	Revised hardware target figures.
RF-ADC Settings	Added AutoCal (Gen 3 only).
RF-DAC Settings	Specified Gen 3 only for Nyquist zone Mix Mode.
System Monitor	Added new section.
RF-DAC Data Pattern	Revised introductory paragraph to provide additional information on the provided files.
Appendix B: FFT Metrics	Revised the dBFS and FspurxH23 metrics.
RF-DAC Data Pattern	Added note on DAC vector length.
12/23/2020 Version 1.3	
General updates	Updated throughout to add Gen 3 information and clarify content for the different devices (Gen 1, 2, and 3). Removed content that is not related to the GUI and is covered in other documentation.
Chapter 1: Introduction	Added references to ZCU216 documentation. Updated Feature Support table with ZCU208 and ZCU216 information.
Software Installation	Added Select Destination figure.
Settings Menu Options	Revised Communication Interface figure.
Clock Settings	Added clock information for Gen 3 devices.
RF-DAC Output Settings—Gen 1 and 2	Added note and Gen 3 information.
Tile PLL Settings	Added note.
Converter Settings	Updated Converter Settings figure.
RF-ADC Settings	Added Calibration Frozen and Attenuation functions.
RF-DAC Settings	Added information for Gen 3.
Clock Distribution (Gen 3)	Added new section.
Interrupts	Added new section.
FIFO Data	Added new section.
Selecting the Hardware Target and Bitstream	Updated the overview figure.
Configuring the Sample Clock	Updated configuring the sample clock figures. Removed Sample Clocks Configuration, Generating a Signal, Acquiring a Signal, ZCU111 and ZCU1275 Setup, and Bitstream Generation sections.

Section	Revision Summary
RF Analyzer Tool Menu Options	Added new section.
RF Analyzer Tool Tabs	Added new section.
Appendix A: LVM and TDMS File Format	Renamed appendix. Customization and Testing and Loopback Test information removed. FFT Metrics and Appending Files information moved to appendices.
08/16/2019 Version 1.2	
Working with the RF Analyzer	Added sub-topics to include detail about installation, generation, and acquisition.
12/14/2018 Version 1.1	
Chapter 1: Introduction	Added information about supported features.
File Menu Options	Added information about the **Bitstream** file menu option.
Settings Menu Options	Updated information about the **Communication** and **Analysis** settings menu options.
RF-DAC Output Settings—Gen 1 and 2	Updated the section and DAC Current Mode screen capture.
Power Advantage Tool—Gen 1, 2, and 3	Added new section.
RF Evaluation Tool Tabs	Updated the MemType section and added information about the size limitation in the DDR mode.
FFT Page	Added information about Zoom Tools.
Chapter 3: RF Analyzer	Added new chapter.
Appendix C: Appending Files	Added new section.
10/19/2018 Version 1.0	
Initial release.	N/A

Table of Contents

Introduction

This document describes the RF Data Converter graphical user interface (GUI) used to drive and analyze the Zynq® UltraScale+™ RFSoC product family.

This general user interface is common to the RF Data Converter Evaluation Tool and the RF Analyzer Tool. It can be used to guide signal generation through RF-sampling digital-to-analog converters (RF-DACs), data capturing through RF-sampling analog-to-digital converters (RF-ADCs), and rapid data analysis using the fast Fourier transform (FFT) and other standard RF data converter metrics. This document primarily focuses on the usage of the GUI.

For the hardware evaluation board and reference design of the Zynq UltraScale+ RFSoC first generation, see the *ZCU111 Evaluation Board User Guide* (UG1271) and *Zynq UltraScale+ RFSoC RF Data Converter Evaluation Tool (ZCU111) User Guide* (UG1287). For the Zynq UltraScale+ RFSoC third generation, see the *ZCU216 Evaluation Board User Guide* (UG1390), *Zynq UltraScale+ RFSoC ZCU208 and ZCU216 RF Data Converter Evaluation Tool User Guide* (UG1433), and *ZCU208 Evaluation Board User Guide* (UG1410).

Use the *Zynq UltraScale+ RFSoC Product Tables and Product Selection Guide*(XMP105) to identify the specific devices that support the different generations of the Zynq UltraScale+ RFSoC family.

When this GUI is used as a component of the RF Analyzer, board control functions are not available. Board control functions, such as onboard clock configuration, are available with the RF Evaluation tool.

The highlights of the RF Data Converter user interface are:

- Ability to control all RF-ADC and RF-DAC channels operating at the same time with a user-friendly graphical interface.
- Ability to configure RFDC clocking subsystem on targeted hardware.
- Direct API function access.
- Save and restore of configurations and preferences that enables quick settings.
- Synchronized data transmission and capturing enabled with multi-tile synchronization (MTS).
- Import and export of data waveform with LVM (ASCII) and TDMS (binary) file format.
- Data length of transmission and capturing of up to 64M samples (DDR mode).
- Enable single or multi-channel views in frequency and time domains for RF analog signals.

The following table compares the features that this software GUI supports with the Evaluation Tool and RF Analyzer.

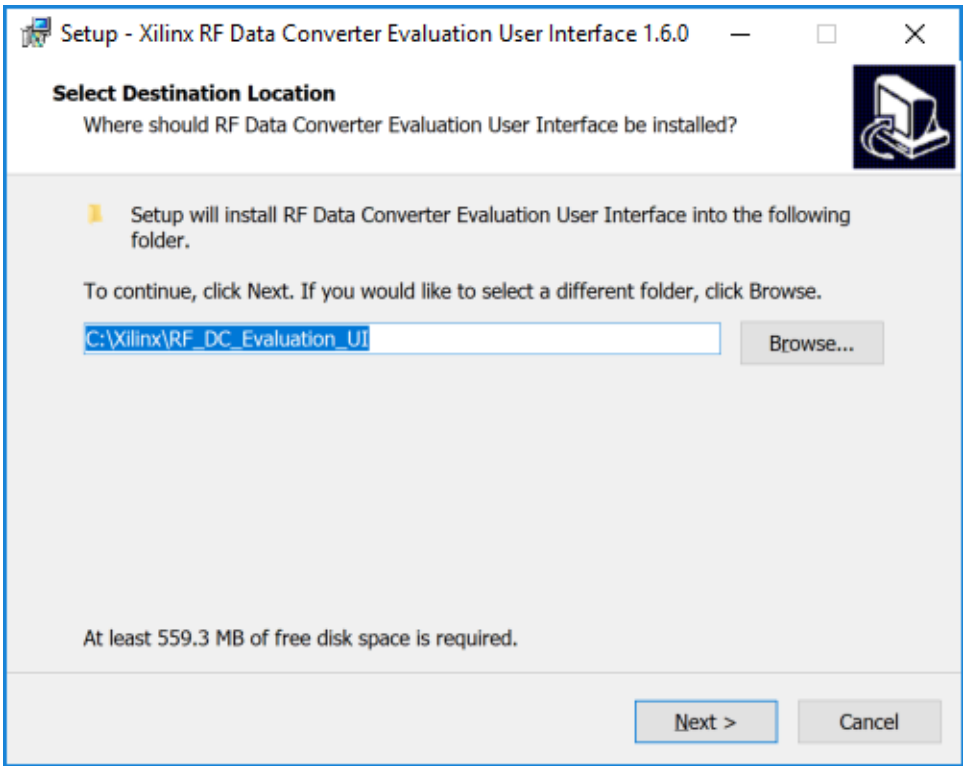
Table 1: **Feature Support**

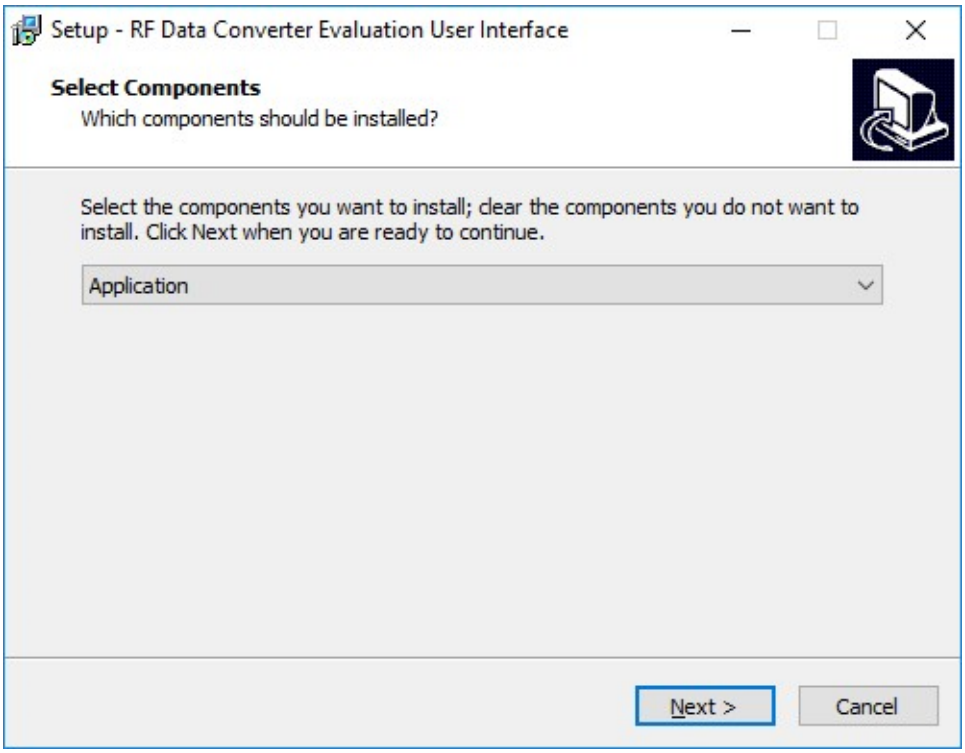
Feature	Evaluation Tool	RF Analyzer
Communication interface	Ethernet	JTAG-UART
Board support	ZCU111 ZCU208 ZCU216	Any Zynq UltraScale+ RFSoC and Zynq UltraScale+ RFSoC DFE device
Sample memory	DDR memory and block RAM	Block RAM only
External component support	External PLL, RF-DAC Power supply (on ZCU111)	None
Multi-tile synchronization (MTS) support	Yes	Yes
Multi-band support	Yes	Yes with pre-built bitstreams
Tile clock forwarding	ZCU208 ZCU216	All devices greater or equal to third generation (ZU4x or greater)
RFDC data stream import/export from/to file	Yes	Yes
Configuration commands dump	Yes	Yes
RFDC samples record options	On-chip or external DDR memory	On-chip only

RF Evaluation Tool

Software Installation

1. The Vivado® Design Suite might need to be installed on the host.
2. Run the installer supplied with the tool through to completion. This installer might request the LabVIEW run-time engine. If necessary, use this link to download the 32-bit version of the LabVIEW Run-time Engine 2018 SP1 Patch.





RF Evaluation Tool Menu Options

File Menu Options

- **File → Load/Save configuration:** Configuration covers all the displayed settings of the Zynq® UltraScale+™ RFSoC such as, real or I/Q mode, mixer settings, and enable or bypass internal PLL. All these settings can be saved and restored. This feature enables quick configuration as well as configurations that can be shared with others. Configuration files are located in the `\Config\` directory by default, with the file extension of `.cfg`.
- **File → Load/Save preferences:** Preferences are the user-defined settings of the GUI. It includes tabs used for data generation, data capture, and user options in the GUI that are not linked to the device under test (DUT) configuration such as, mapping in the MultiView mode, number of samples, and tone frequency. You can save the preferred settings of GUI or restore any of them. Preferences files are located in the `\Config\` directory by default, with the file extension of `.prf`.
- **File → Hardware target:** RF Analyzer only. Opens the bitstream download screen.
- **File → Export ADC Data:** This command exports the RF-ADC data captured of all the opened RF-ADC channels with LVM or TDMS file format (chosen in **Settings → Data File Format**). The default directory is `\Data\ADC\`.

- **File → Exit:** Exit the software.

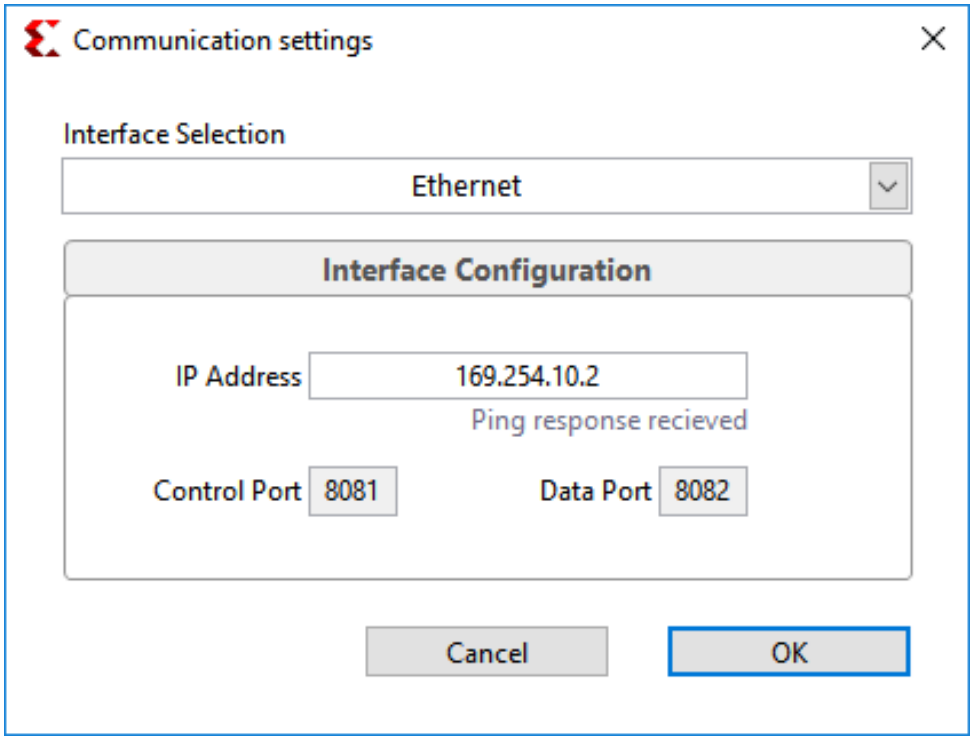
Edit Menu Options

- **Edit:** Standard Windows edit menu.

Settings Menu Options

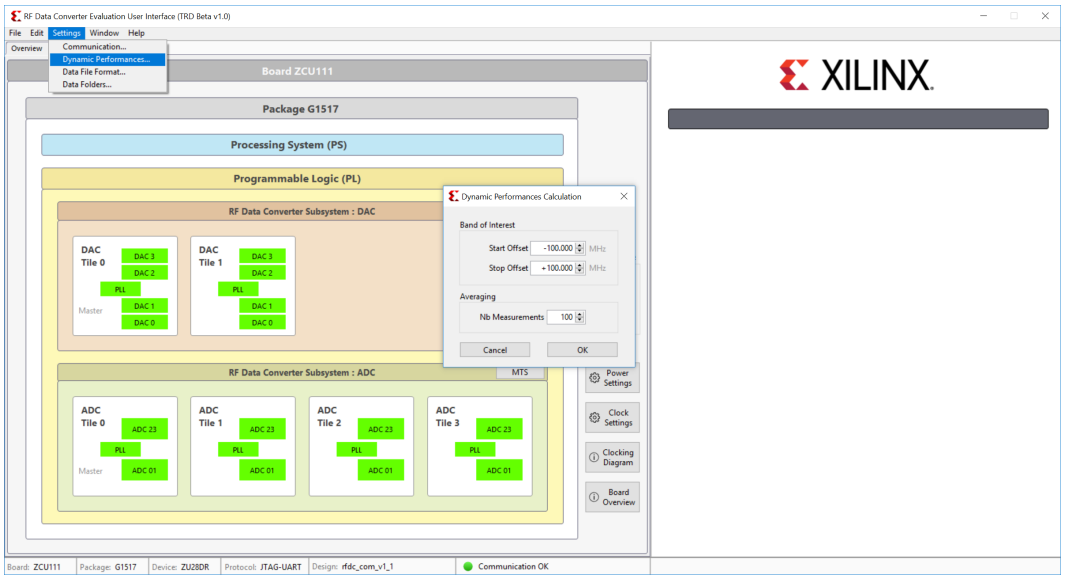
- **Settings → Communication:** Displays the current communication interface. Ethernet is used for the RF Evaluation Tool.

Figure 1: **Communication Interface**



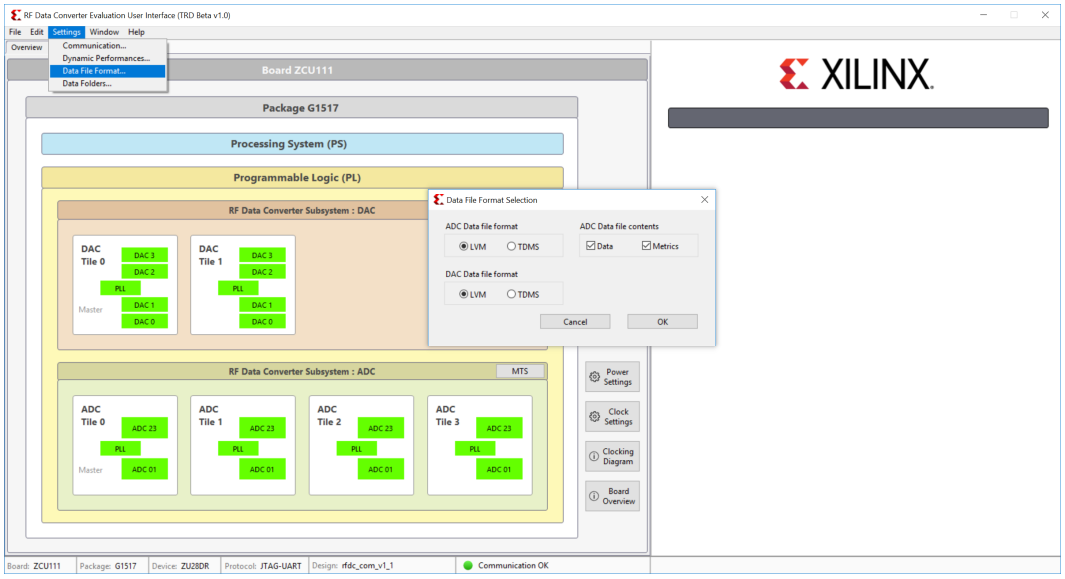
- **Settings → Dynamic Performances:** Some RF-ADC metrics are based on the frequency range. On the RF-ADC FFT page, there is a marked-out calculation table, the SNR, ENOB, SFDRxH23, and FspurxH23 are calculated based on the Band of Interest set here. In loop mode, some metrics are calculated over a number of measurements that can be set under Averaging.

Figure 2: **Band of Interest**



- **Settings → Data File Format:** Indicate your preferred file format between the .lvm and .tdms formats. For the RF-ADC output, you can individually select whether **Data** or **Metrics** is exported.

Figure 3: **Data File Format**

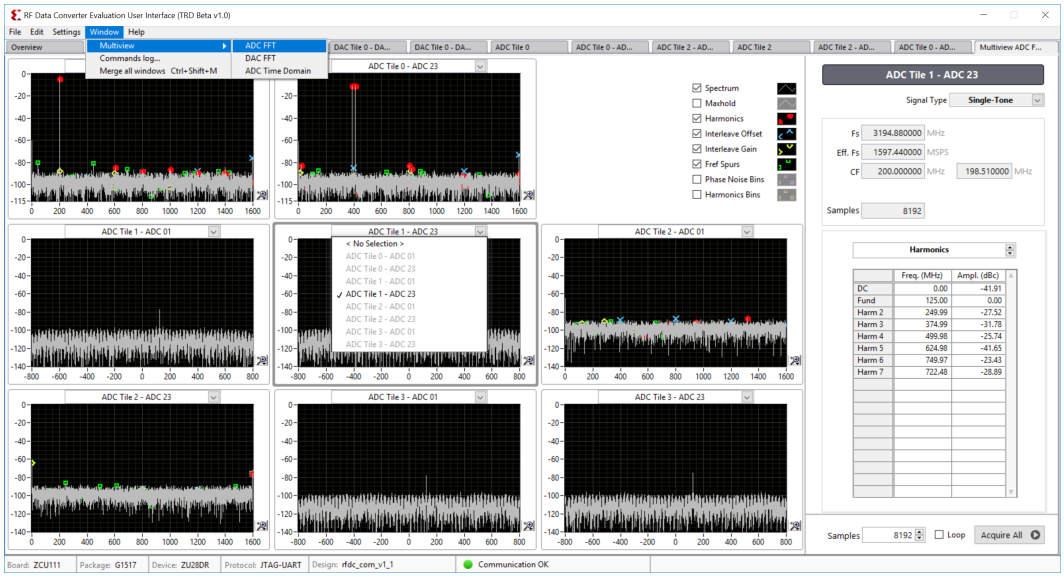


- **Settings → Data Folders:** Select your preferred folders for the test vector of RF-DAC, saved data from RF-ADC, and onboard clocking frequency configuration files. By default, these are located in `\Data\`, with ADC, DAC, and Clocking as the respective folder names.

Window Menu Options

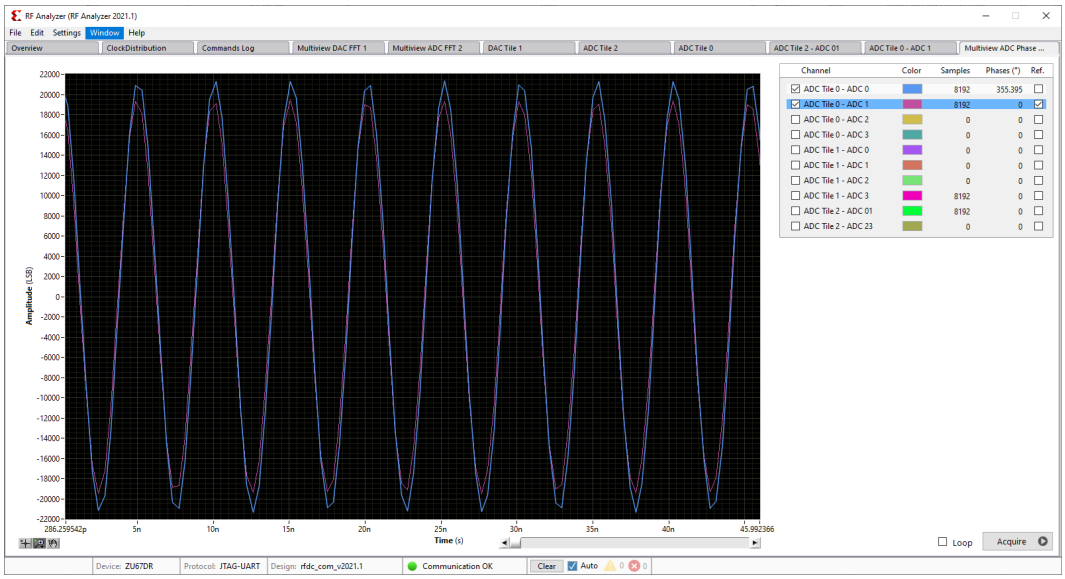
- **Window → MultiView:** The MultiView option makes it possible to view several of the RF-ADC or RF-DAC FFT diagrams on a single page with customized channels. Click **Generate/Acquire All** to update all the windows.

Figure 4: **MultiView RF-ADC FFT**



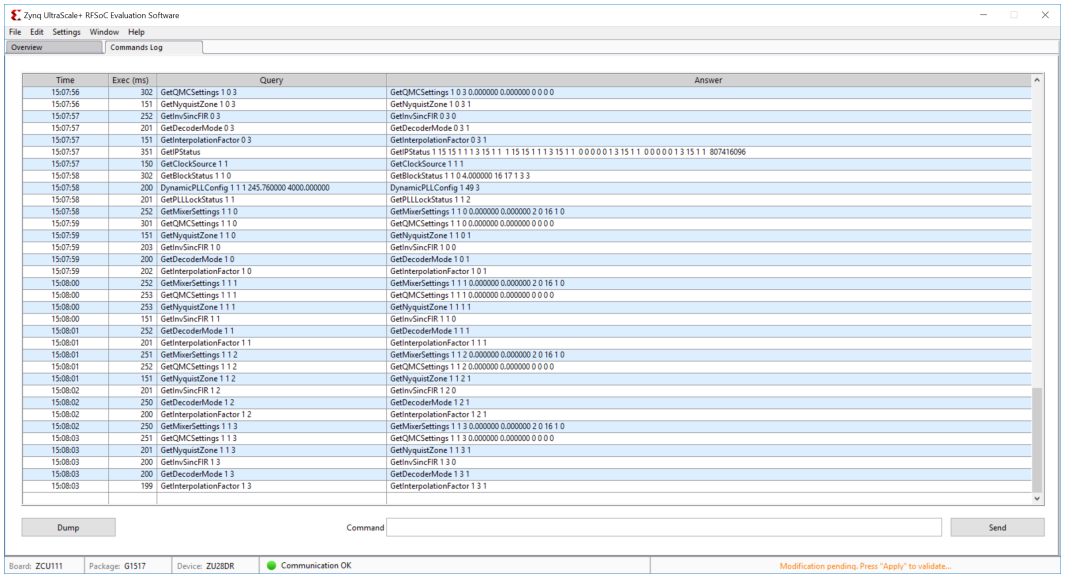
To display all the RF-ADC channel signals in the time domain, select the **ADC Time Domain** option. This feature is particularly useful in the MTS mode. The phase between channels is displayed, relative to the reference channel.

Figure 5: **MultiView RF-ADC Time Domain**



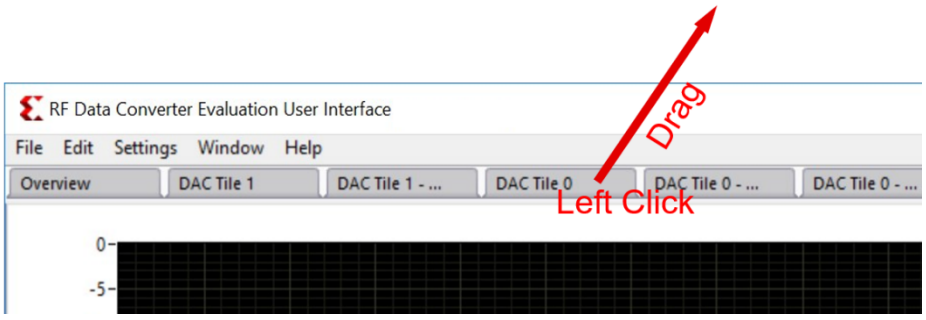
- **Window → Commands log:** This opens the commands log window where the history for all the commands can be seen, the API can be run, and feedback can be viewed. If an error occurs with the GUI, it appears on the command log. The command log window can also be used to create a dump file which lists out all the previously used commands. This can be useful in debugging if an error occurs with a sent command.

Figure 6: **Command Window**



- **Window → Merge all windows:** Opened tabs for DACs or ADCs can be moved to separate windows with a left-click and drag on the tab area as shown in the following figure. This command merges all the separate windows into one.

Figure 7: **Create Separate Windows**



- **Window → Attach:** Opened tabs can be moved to separate windows. This command merges back selected separate windows.

Help Menu Options

- **Help → About:** Provides general information about the RF Data Converter evaluation tool. Use this option to check the version, which is used when building the `.lvm` file.

RF Evaluation Tool Tabs

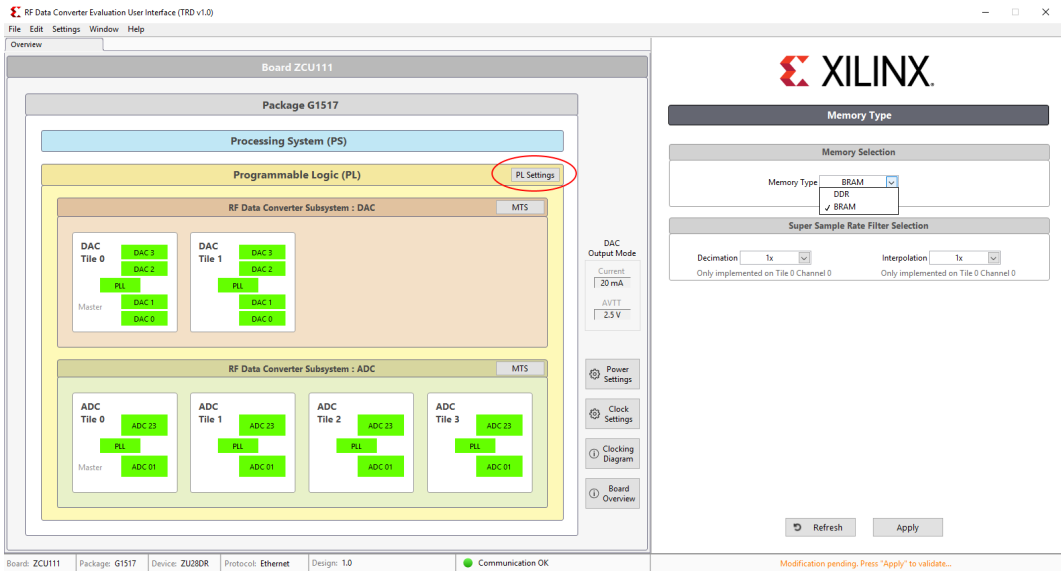
The Overview page is the home page of the RF Data Converter evaluation tool GUI. It displays the top framework of all the converters grouped by tile. This page is displayed upon start-up and cannot be closed.

Overview

Generation 1 and 2

In the overview tab, select **MemType** to choose the memory type, **BRAM** (on Zynq® UltraScale+™ RFSoC) or **DDR** (on the ZCU111 evaluation board). The DDR is bigger in size than the block RAM.

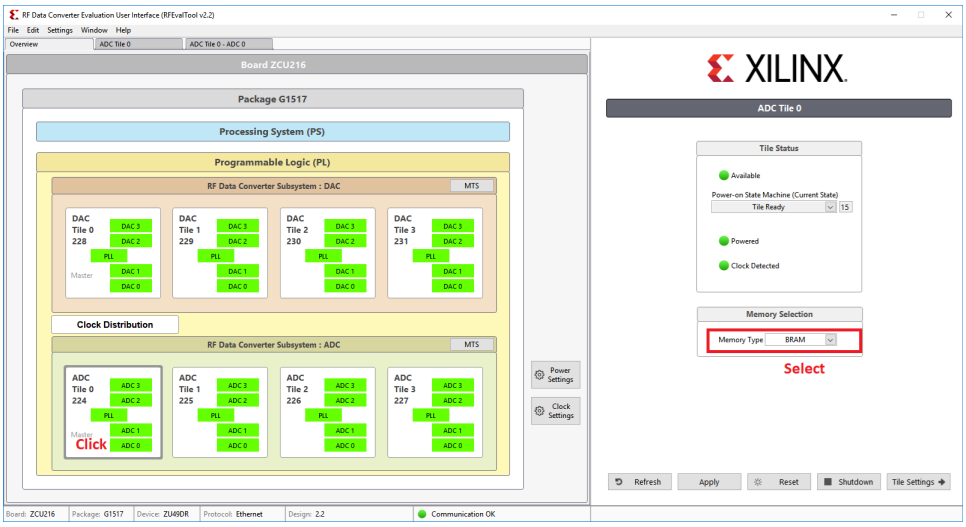
Figure 8: **Overview Page—Gen 1 and 2**



Generation 3

In the overview tab, click on an DAC or ADC tile and then choose the memory type, **BRAM** (on Zynq® UltraScale+™ RFSoC) or **DDR** (on the Gen 3 evaluation board). The DDR is bigger in size than the block RAM.

Figure 9: **Overview Page—Gen 3**



Clock Settings

There are different on-chip clock distribution architecture limitations in different RFSoC generations. The user guides for each board show which RF PLLs/tiles are driven from off-chip and which RF PLLs/tiles get clocks from the on-chip clock distribution system.

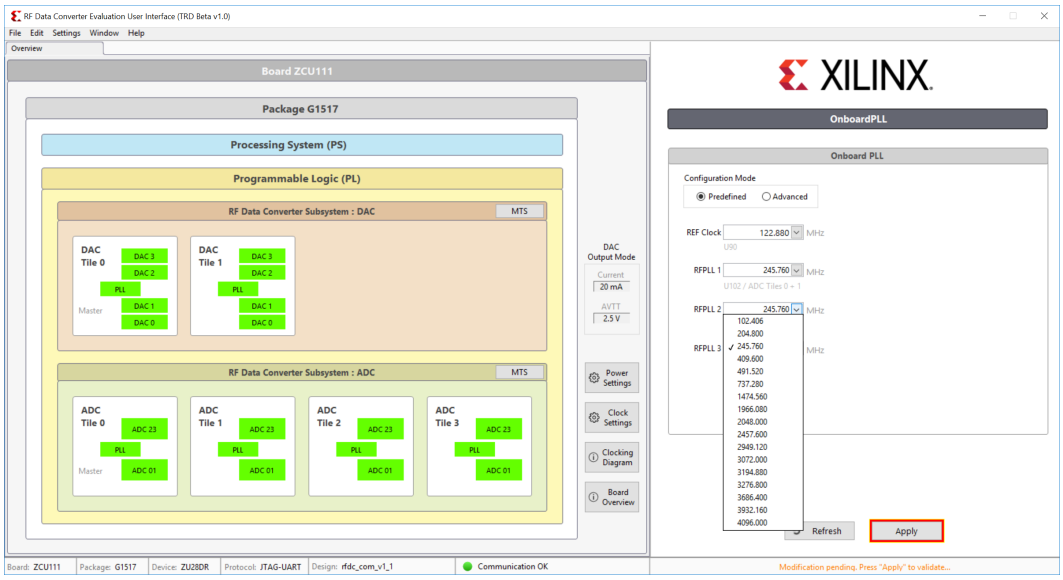
Gen 1 and 2: see the *ZCU111 Evaluation Board User Guide* (UG1271) for more information.

Gen 3: see the *ZCU208 Evaluation Board User Guide* (UG1410) or *ZCU216 Evaluation Board User Guide* (UG1390).

Gen 1 and 2 Predefined Mode

In the overview tab, select **Clock Settings** to open the onboard PLL GUI in the right panel. This GUI allows you to control and set the input and output frequencies for the PLLs that are integrated onto the ZCU111 evaluation board. In the Predefined mode, available frequencies are provided in the drop-down list for RF-ADC and RF-DAC. Choose your options and click **Apply**. The GUI programs the onboard RFPLLs. If your desired frequency does not appear in the predefined list, then you must use the advanced configuration mode to customize the sample rates.

Figure 10: **Clock Settings Predefined—Gen 1 and 2**

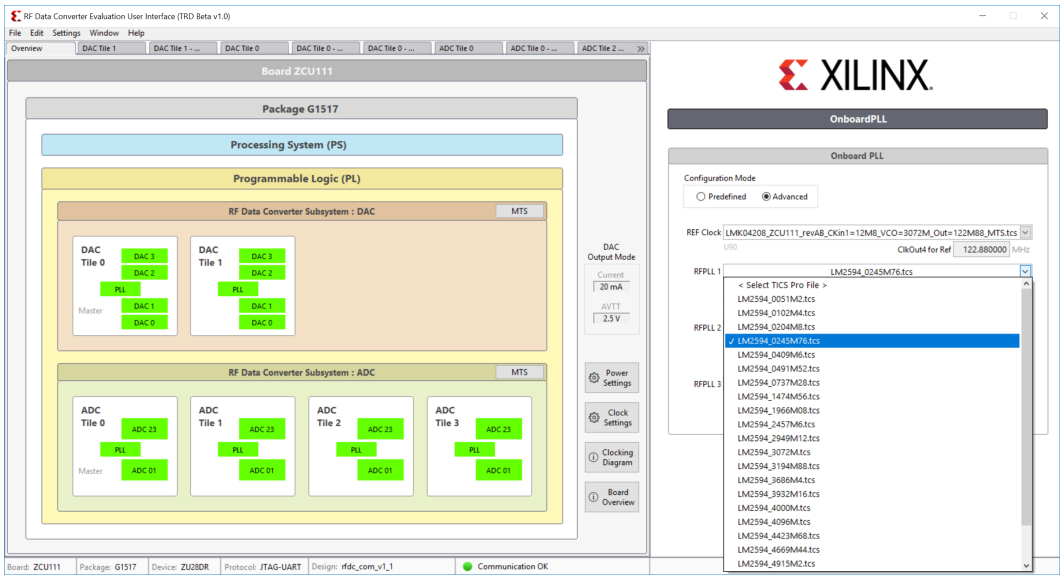


Gen 1 and Gen 2 Advanced Mode

The Advanced mode accepts the configuration file for the individual clock ICs on your clocking plug-in board. You can choose the `.tcs` file shipped along with this tool or generate your own configuration files using TICS Pro Software.

Click **Advanced** to select the desired clock configuration.

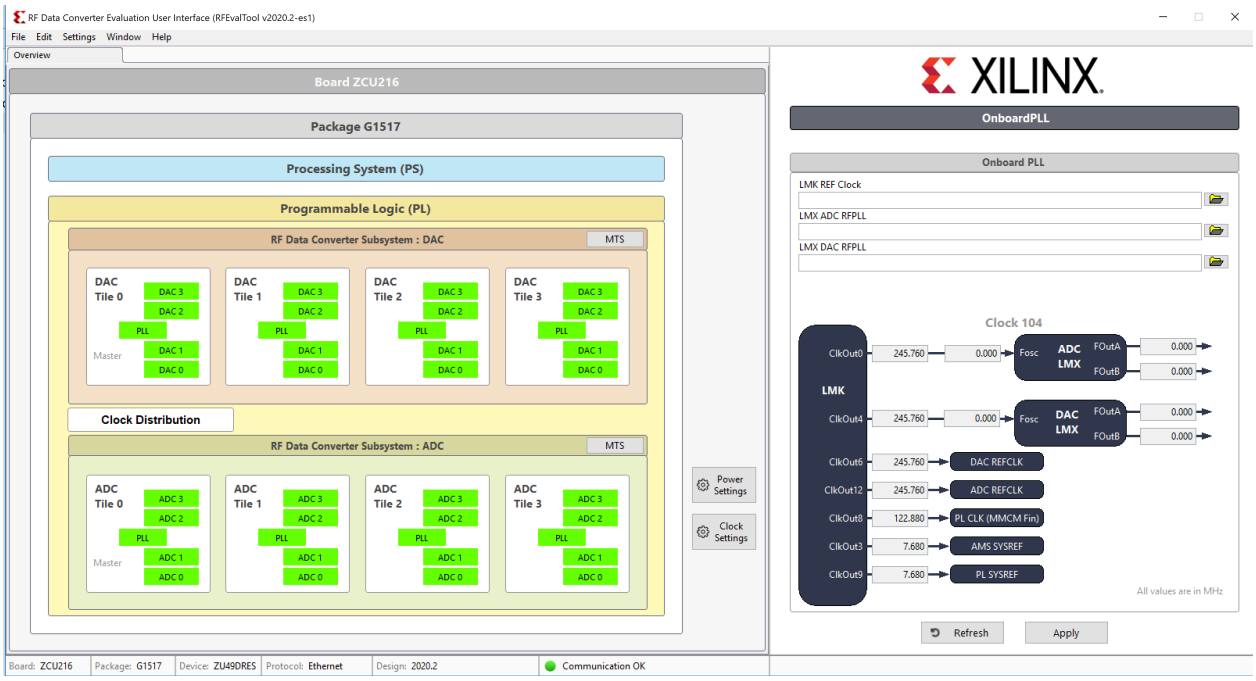
Figure 11: **Onboard PLL Advanced**



Gen 3

In the overview tab, select **Clock Settings** to open the onboard PLL GUI in the right panel. This GUI allows you to control and set the input and output frequencies for the PLLs mounted on the CLK104 (daughter board of the ZCU216 and ZCU208 boards). Choose your options and click **Apply**. The GUI programs the onboard RFPLLs.

Figure 12: **Onboard PLL —Gen 3**

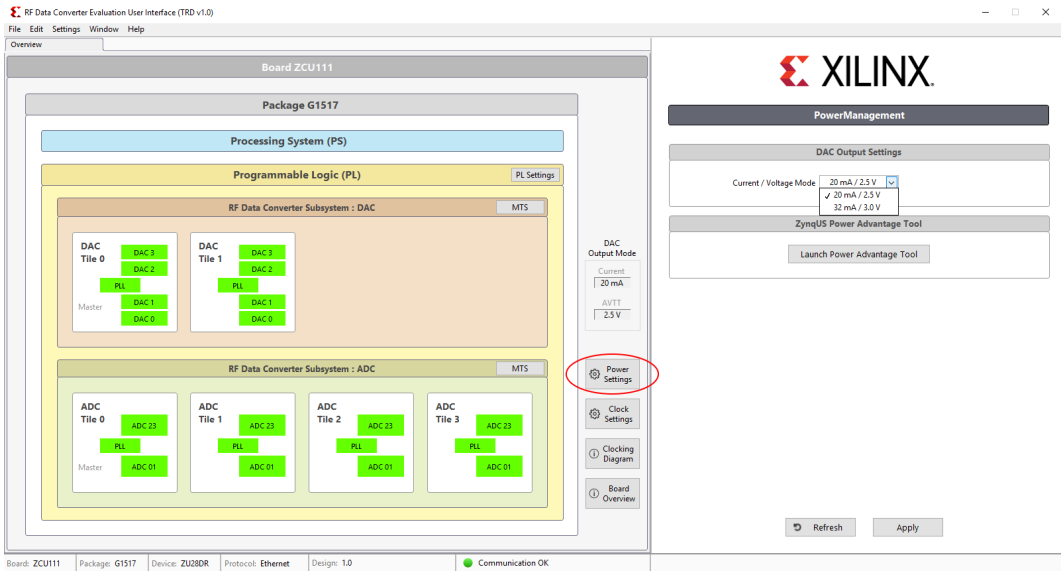


RF-DAC Output Settings—Gen 1 and 2

***Note*:** In Gen 3, the variable output power (VOP) provides fine control for the DAC output. For more information, see *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).

RF-DAC output current settings are only available with the RF evaluation tool. In the overview tab, click the **Power Settings** button to open the RF-DAC output settings page in the right panel. Choose from the available 20 mA/2.5V and 32 mA/3.0V options. Power supply for this current mode control (DAC_AVTT) is programmable on the board through the power management unit (PMU). Click **Apply** to program the onboard PMU for either 2.5V or 3.0V, and switch to the corresponding RF-DAC output current mode.

Figure 13: **RF-DAC Current Mode**



Related Information

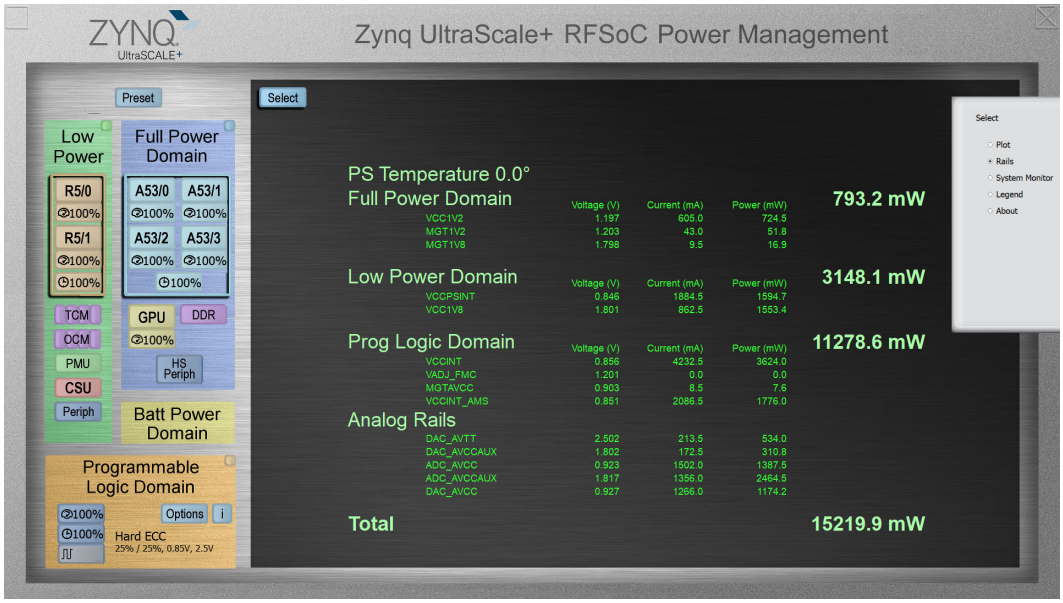
RF-DAC Settings

Power Advantage Tool—Gen 1, 2, and 3

The power advantage tool is integrated in this software to provide power related information for reference. This power advantage tool displays voltage, current, and power information for each rail that is monitored by the onboard power management unit. The power advantage tool communicates with the evaluation software through the JTAG interface. To retrieve the power information, connect the JTAG port to the host. For Gen 3, if the installation path of the evaluation tool is not standard, it must be changed in the .ini file to enable the power advantage tool.

Figure 14: **Power Advantage Tool**

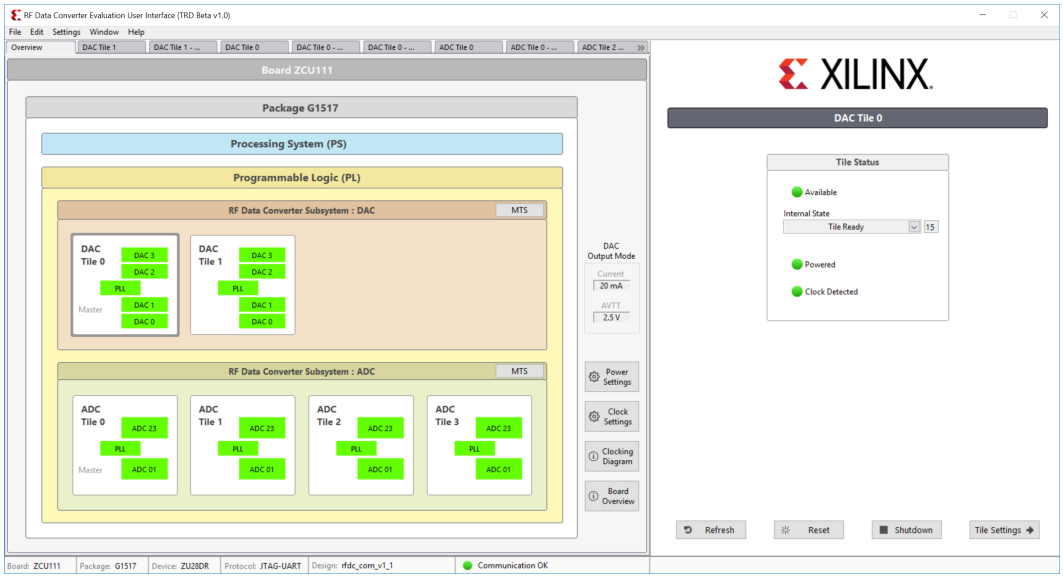
Figure 15: **Zynq UltraScale+ RFSoC Power Management**



RF-ADC/RF-DAC Tile

In the overview tab, selecting any of the RF-ADC or RF-DAC tile opens the individual tile page as illustrated in the following figure. In this tab, you can reset, shut down, start up a tile, and also view the current tile status by clicking **Refresh**. When a tile is in operation, selecting **Tile settings** opens up the configuration tab for it. Refer to the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for more information on the commands and power up state machine status.

Figure 16: **Tile Status**

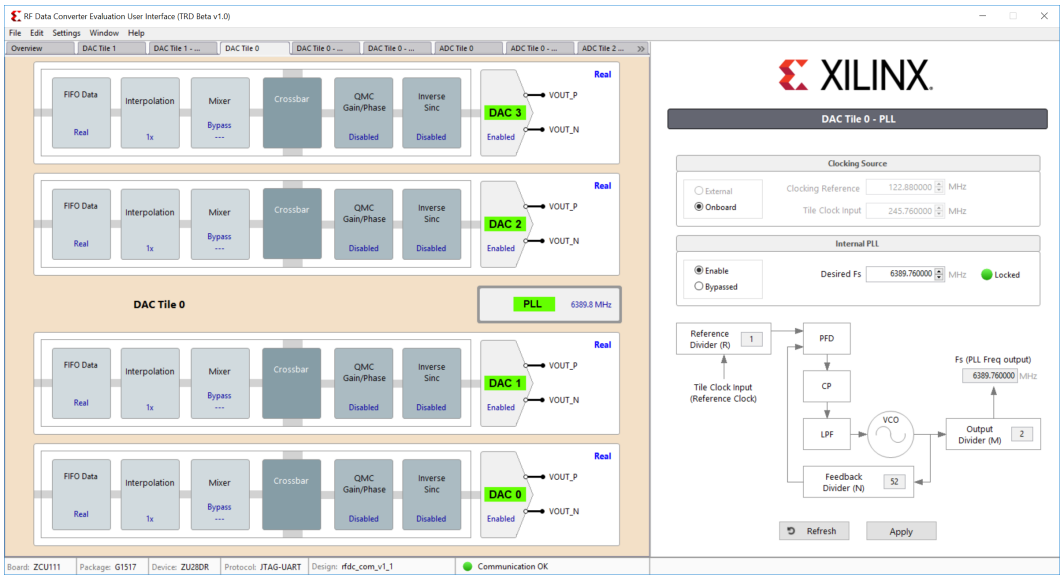


Tile PLL Settings

***Note*:** See Clock Distribution (Gen 3) for clock and PLL settings in Gen 3.

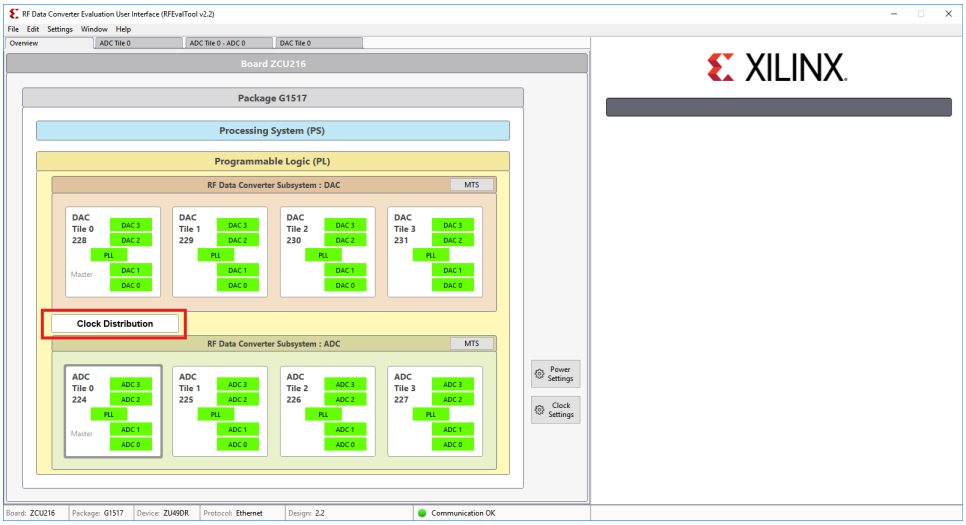
For Gen 1 and 2, in the tile settings page, click on the **PLL** box to open the PLL settings in the right panel.

Figure 17: **Clock Source—Gen 1 and 2**



For Gen 3, to select clock sources and options for on-chip clock distribution, use the **Clock Distribution** button shown in the following figure.

Figure 18: **Clock Source—Gen 3**

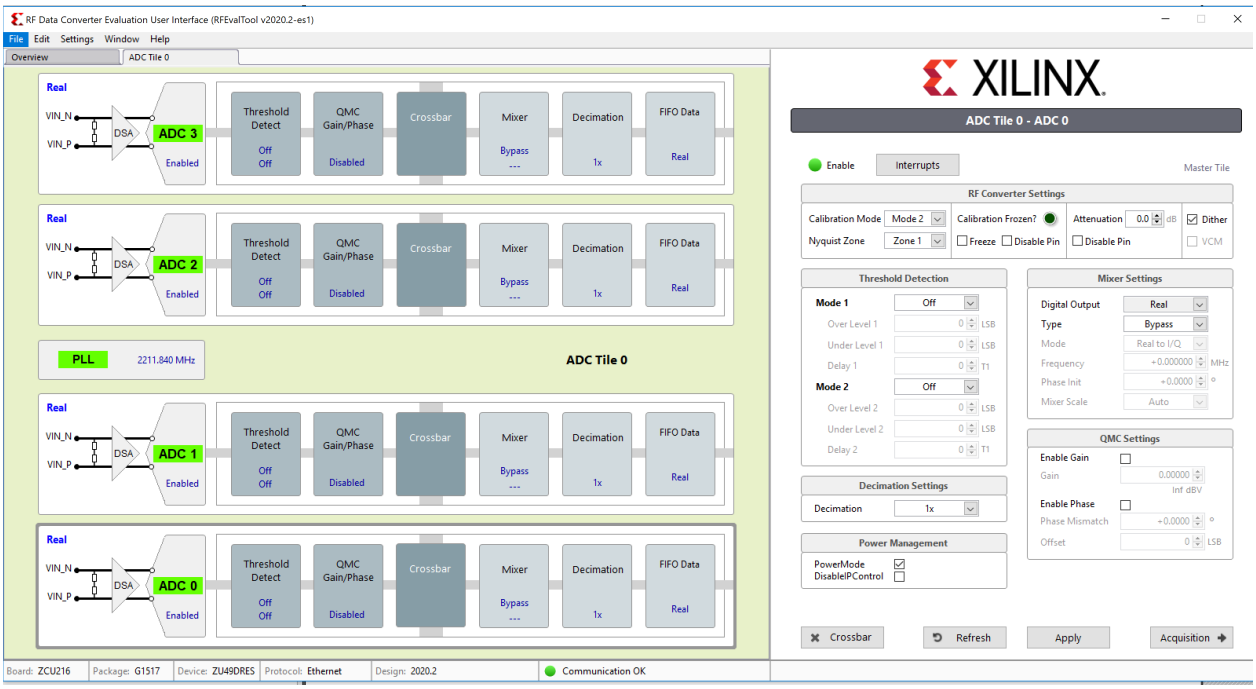


Ensure that the input clock rate is correct for the internal PLL, enabled or bypassed. When bypassing the internal PLL, the input clock functions as a sampling clock of the converters in the tile, and is usually several GHz. When the internal PLL is enabled, ensure that the input frequency is within the range specified by the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926). A reference frequency can also be typed in when the internal PLL is disabled. This helps the GUI calculate the reference spurs on the FFT page.

Converter Settings

In each RF-ADC/RF-DAC tile, the available converter channels and associated internal function blocks are cascaded in the block diagram, and the text shows the current settings. Click any function block to open the config page in the right panel. FIFO and Crossbar have their own separate pages.

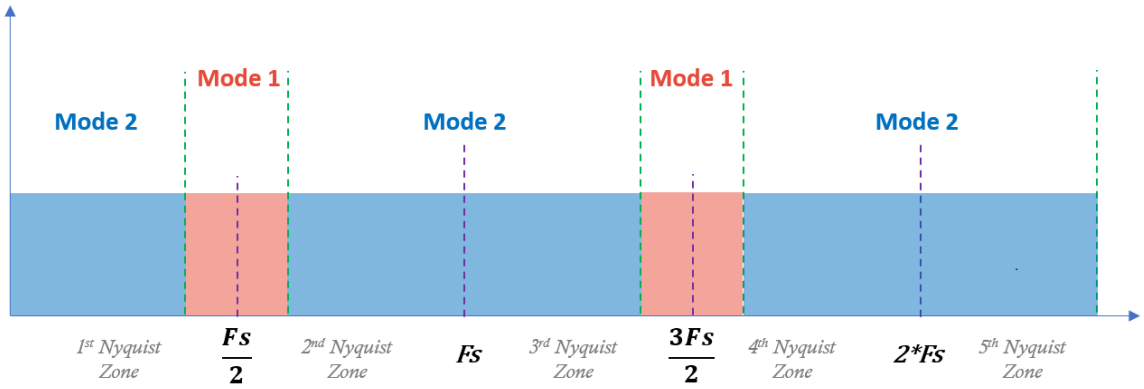
Figure 19: **Converter Settings**



RF-ADC Settings

- **Calibration Mode:** Selects between different calibration optimization schemes depending on the features of the input signals. For more information on calibration mode, see the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).

Figure 20: **Calibration Mode**



- **Nyquist Zone:** Choose the Nyquist zone in which the input signal located. This is related to interleaving calibration and must be indicated correctly. Zone 1 is for odd numbered zones and Zone 2 is for even numbered zones.
- **Threshold Detection:** Use this to set the embedded threshold detection parameter.
- **Decimation Settings:** Use this to select the decimation factor.

  Note: If you select Off, you will not receive any data.

  Xilinx® recommends that the same decimation factor is used for all data converters in the tile to avoid potential timing issues at the interface.
- **Calibration Frozen:** Use this to freeze the interleaving calibration for each channel. The green light indicates a frozen status. The freeze function freezes or unfreezes the interleaving calibrations. The disable pin function can disable the calibration freeze real-time port control.

The following functions are for Gen 3 only.

- **Attenuation:** Attenuation value of on-chip DSA in dB for each RF-ADC channel. The disable pin can disable the DSA pin control.
- **Power Management:** Use to power down or power up a single channel within a tile.

RF-DAC Settings

- **Decoder Mode:** Choose which performance to optimize: noise floor or linearity. Low noise mode is recommended for broadband modulated signals.
- **Nyquist Zone:** Choose which Nyquist zone the signal will be located in: Normal Mode for Nyquist zone one and Mix Mode for Nyquist zone two. See this link for more information.
- **Interpolation Settings:** Choose your interpolation factor. If you select Off, some digital blocks will be powered down and the outputs will not be active.

- **Inverse Sinc Settings:** Enabling Inverse Sinc compensates sinc roll-off at high frequencies. For Gen 1, this function is only effective when the signal is located in Nyquist zone one. For Gen 3, this feature can be applied for first or second Nyquist zones.

The following functions are for Gen 3 only.

- **DataPath:** The drop-down box used to choose datapath modes. The four available modes are Full Nyquist DUC, IMR low pass, IMR high pass, and DUC bypass. For more information on datapaths, see *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).
- **Current:** The VOP current value. This value is also displayed on the diagram of each channel. Only available for Gen 3 or later parts.
- **Power Management:** Use to power down or power up a single channel within a tile.

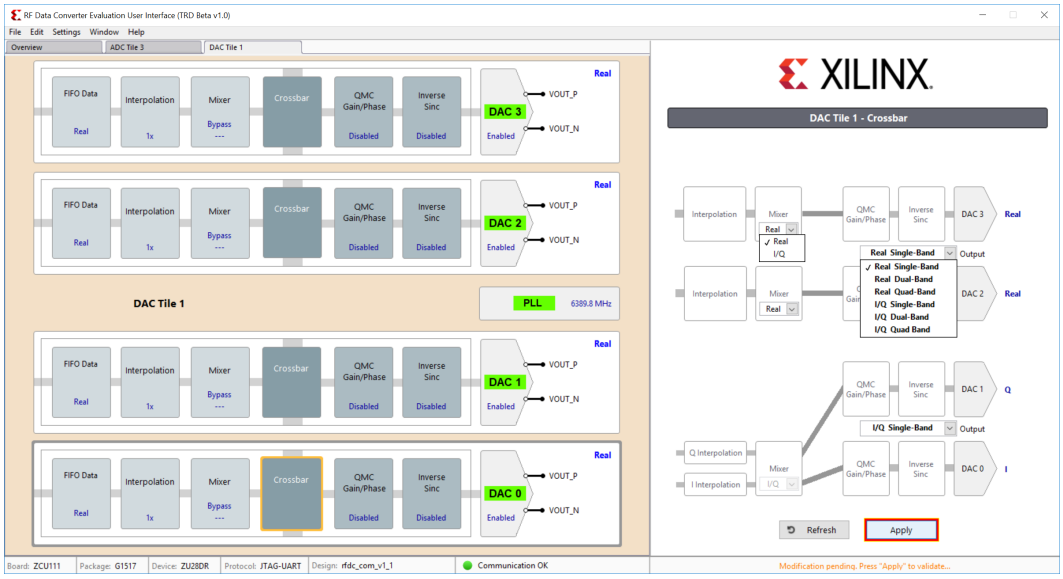
Settings Common to RF-ADC and RF-DAC

- **Mixer Settings:** Xilinx recommends setting the Crossbar page first, and then set other parameters of the mixer and NCO because the mixer is bypassed in the real-to-real mode.
- **QMC Settings:** QMC module contains gain, phase, and DC-offset adjusting. These are used to compensate unmatched I and Q signal path when converters interface to external modulators or demodulators. DC offset takes effect with DC coupling only. Phase offset takes effect with complex mode only. Gain takes effect in all modes.
- **FIFO:** Show the FIFO clock rates and number of words on PL and converter side for information only.

Crossbar

Click the **Crossbar** button at the bottom of the converter settings page, or, alternatively, the **Crossbar** box in the left panel to display the crossbar page. This page determines the real or complex mode of the mixer and multi-bands operating mode. Complex mode activates a pair of channels to support both in-phase(I) and quadrature(Q) signal. Because of the complex mixer (and NCO) architecture, the real-to-complex (R2C) or complex-to-complex (C2C) mode is allowed, but complex-to-real (C2R) mode is not allowed. This means that there is no C2R mode available for RF-ADC and no R2C mode available for RF-DAC. Correct operating modes are ensured by this tool. In complex mode, even channels are always used for I signals, and odd channels are used for Q signals.

Figure 21: **Crossbar**

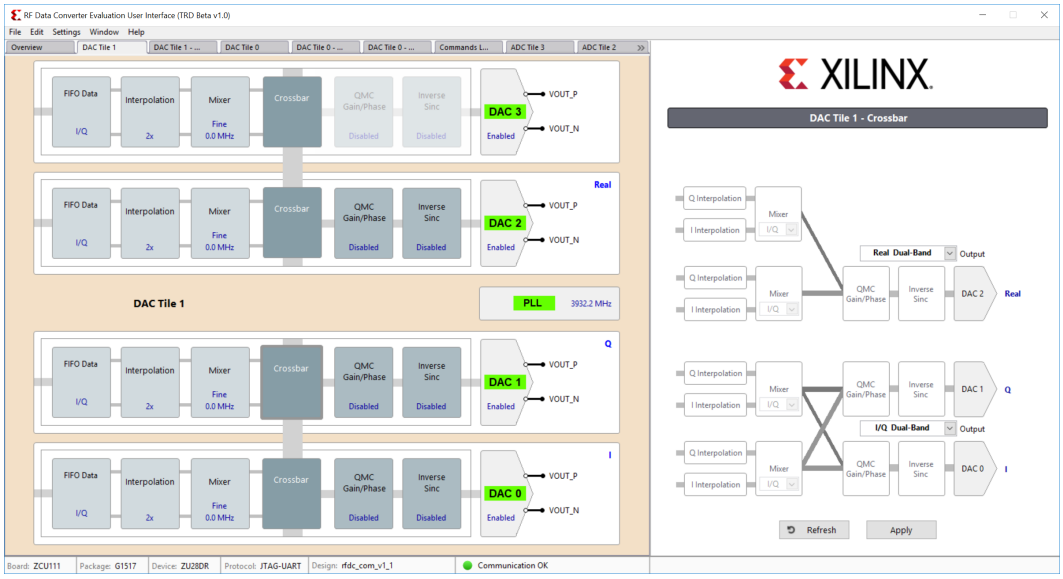


Multi-Bands

Multiple bands enable one RF-DAC or RF-ADC analog channel and share multiple DUC or DDC channels to transmit or receive the multi-band carrier signals. For RF-DAC, multiple baseband signals can be up-converted in separate DUC chains and then combined at the crossbar before being sent to the analog RF-DAC block.

In RF-ADC, the multi-band/carrier inputs from one RF-ADC are split into multiple DDC paths for down-conversion. The carriers from different bands are separated and located at low frequencies (in general at zero). In the multi-band operation, a converter is enabled on channel 0 (dual bands at channel 0 and 1) or channel 2 (dual bands at channel 2 and 3). Multi-bands operations support both real and complex output. All these configurations can be enabled at the crossbar page. The following figure illustrates the dual bands configuration of C2C and C2R.

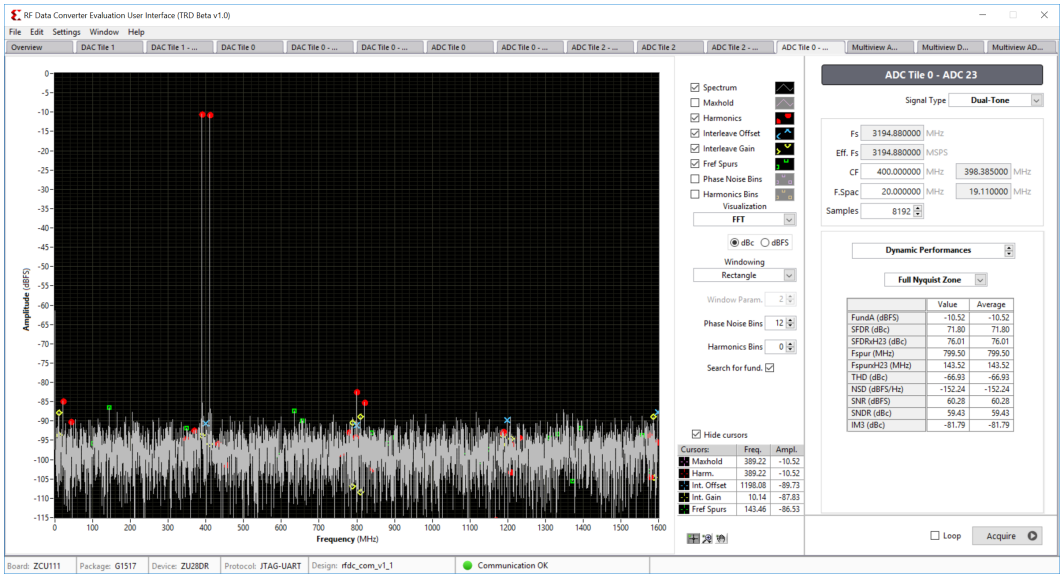
Figure 22: **Multi-Bands**



FFT Page

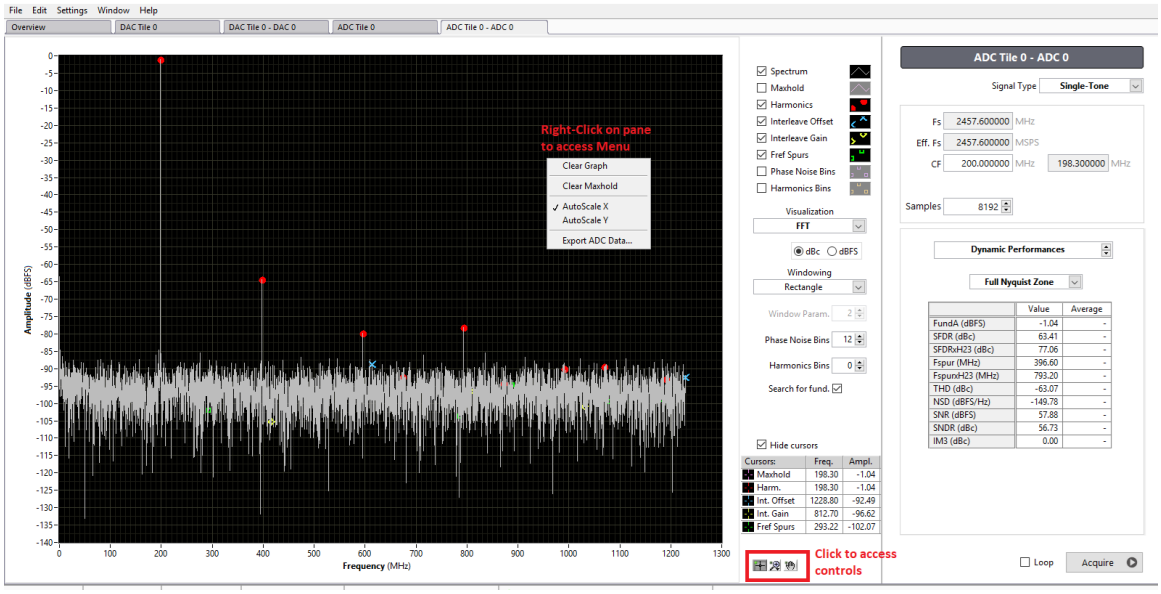
Click **Acquisition** in the ADC settings page, or **Generation** in the DAC settings page, to open the FFT page. In the RF-DAC FFT page, the single tone and dual tone generator is embedded in the software. To generate a complex modulated signal, load a test vector file. There are variations of sub-menus in this page, including signal characteristics, customizing FFT plot, windowing function, test vector input, and output. When decimation or interpolation is enabled in the RF-ADC or RF-DAC data path, with a value more than 1 (bypass), Eff.Fs and Fs show different values in this table. Fs indicates the sampling frequency of observed RF-ADC or RF-DAC, Eff.Fs indicates the sampling frequency of original data stream (base band) after decimation or before interpolation. The X-axis (frequency) of the FFT plot reflects back the Eff.Fs. The following figure shows the RF-ADC FFT page.

Figure 23: **RF-ADC FFT Page**



The following figure shows the Zoom Tools on the FFT page. Use the default Zoom Tools or edit the axis range to directly configure the start and/or end values for best plot observation.

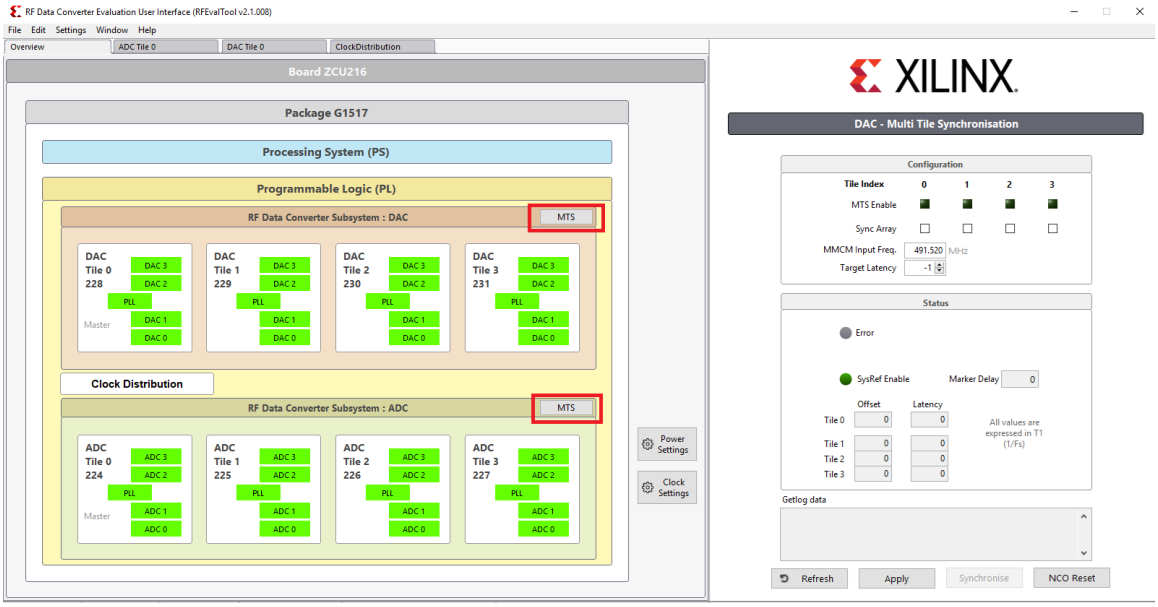
Figure 24: **FFT Zoom Tool**



Multi-Tile Synchronization

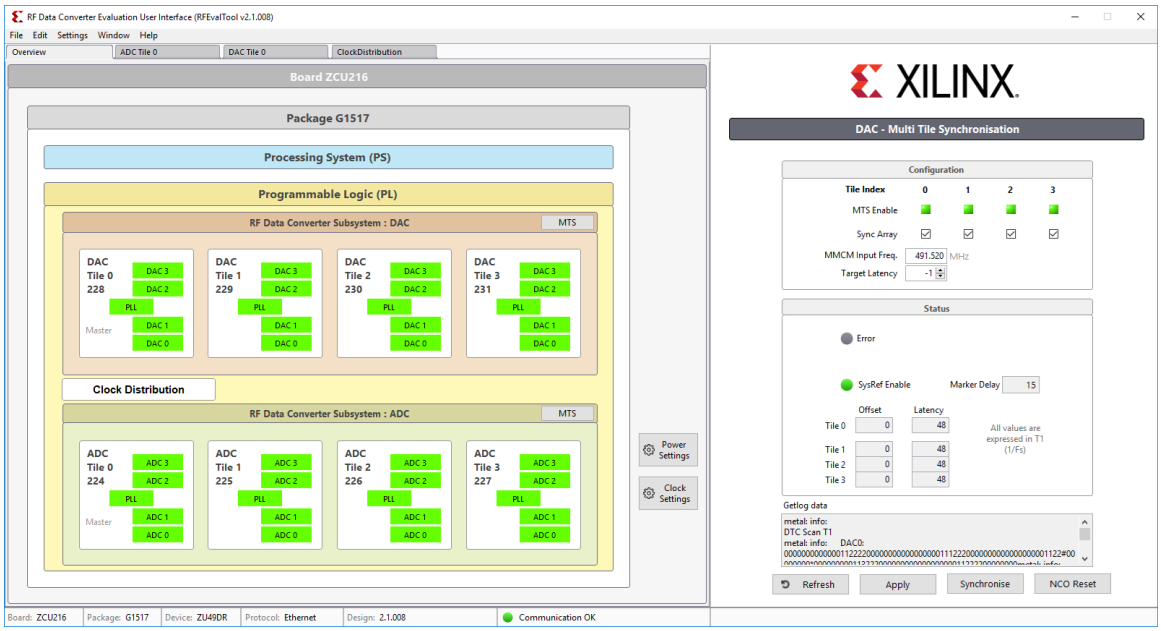
The multi-tile synchronization (MTS) feature enables multiple converter channels working with an aligned and deterministic latency across tiles and chips. MTS is supported as a standard feature with the RF evaluation tool. In the overview page, there is an MTS tab on the right corner of the ADC and DAC group. Click the **MTS** tab to open the function window.

Figure 25: **MTS**



The external clocking coming from the board must be set up according to the MTS rules. For more information, see the "Clock Settings" chapter in *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269). To enable the MTS function, check **enable → Apply**. This enables the internal clock scheme to support MTS. After MTS is enabled, select **Synchronise** to implement the alignment and display the measured latency of each tile. An offset value also shows how many T1 (period of sampling clock) offset have been applied to align the tiles. The error lamp lights up red if there are any errors during MTS.

Figure 26: **MTS Successful**

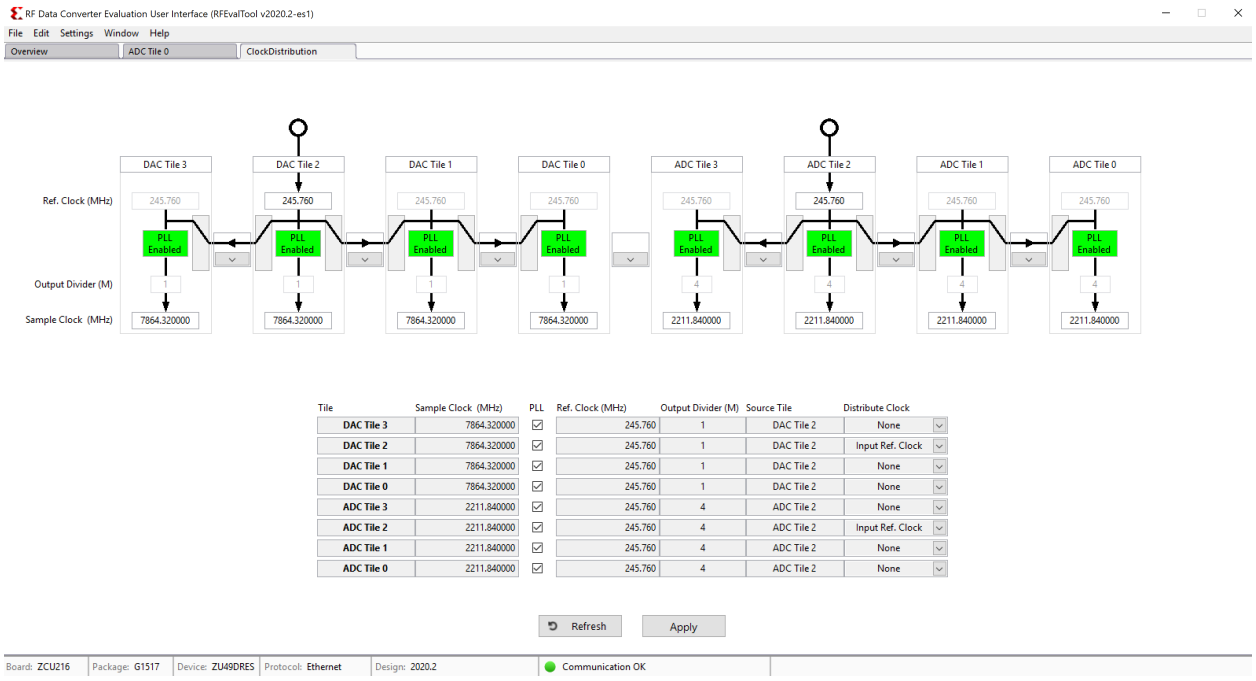


Clock Distribution (Gen 3)

The Zynq UltraScale+ RFSoC Gen 3 supports on-chip clock distribution. For more information, see *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).

Click the **Clock Distribution** button in the overview page to display the page shown in the following figure.

Figure 27: **Clock Distribution**



***Note*:** The settings on this page should comply with the limitations of the on-chip clock distribution system and PLL.

Each tile has four input fields and a check box for an in-tile PLL, as described here.

- **Sample Clock (MHz):** Select the desired sampling rate of converters, which can be generated by the in-tile PLL or a forwarded sampling clock from the source tile.
- **PLL Checkbox:** Enable or disable the PLL in this tile.
- **Reference Clock (MHz):** Enter the reference or a sampling clock frequency, can be from an external input or a forwarded clock from the source tile.

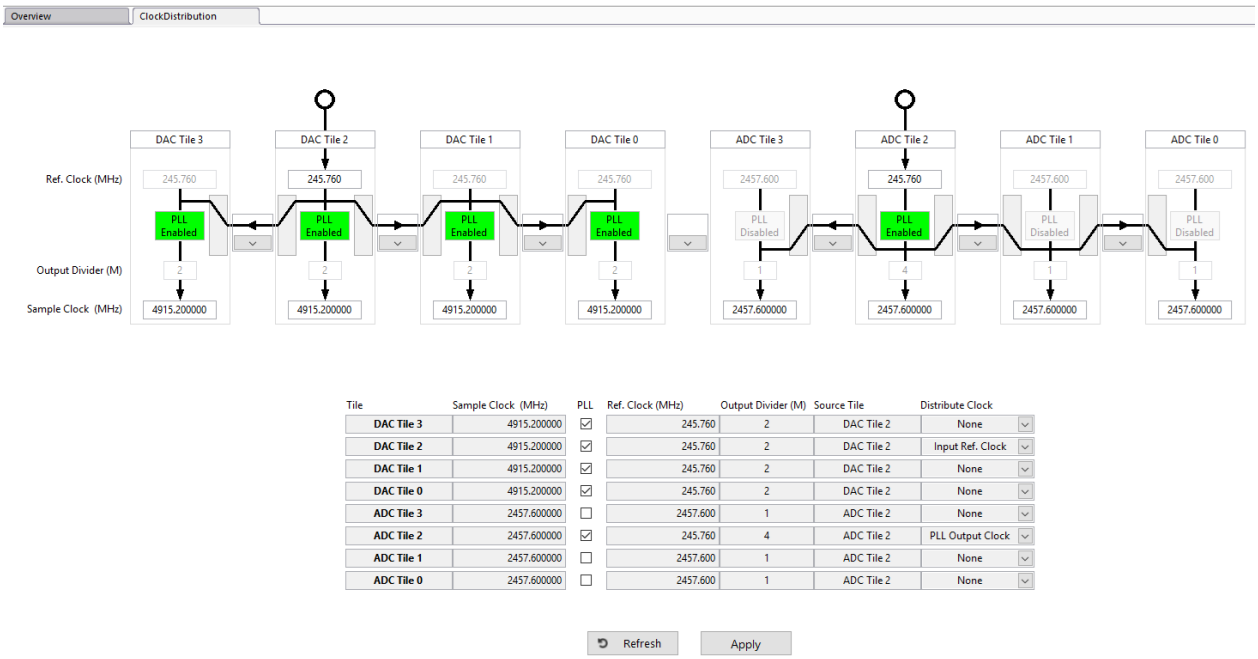
  ***Note*:** This frequency can be a reference for the in-tile PLL or the frequency of the sampling clock if it is used directly.

- **Source Tile:** Use the drop-down list to select which tile the clock (reference) comes from. Select the tile itself for the external clock input to this tile, or the source tile for a forwarded clock (reference or sampling clock). Select the tile itself for a source tile.
- **Distribute Clock:** Select options to distribute the clock (acting as source tile) and which clock is distributed:

  1. None: select to not distribute the clock.
  2. Input clock: select to distribute the input clock from an external input. This clock can be a low-frequency reference clock or a high-frequency sampling clock.
  3. PLL output clock: select to distribute the clock generated by the in-tile PLL.

An example configuration is shown in the following figure.

Figure 28: **Example Clock Distribution Configuration**



In this example, two external input clocks (both at 245.76 MHz) are fed to the ADC_Tile_226 and DAC_Tile_230, respectively. All desired RF-ADC clocks are 2457.6 MHz and desired RF-DAC clocks are 4915.2 MHz.

For the RF-ADC group, Tile_226 distributes its *PLL output clock* to other RF-ADC tiles. For the RF-DAC group, Tile_230 distributes its input reference to all other RF-DAC tiles.

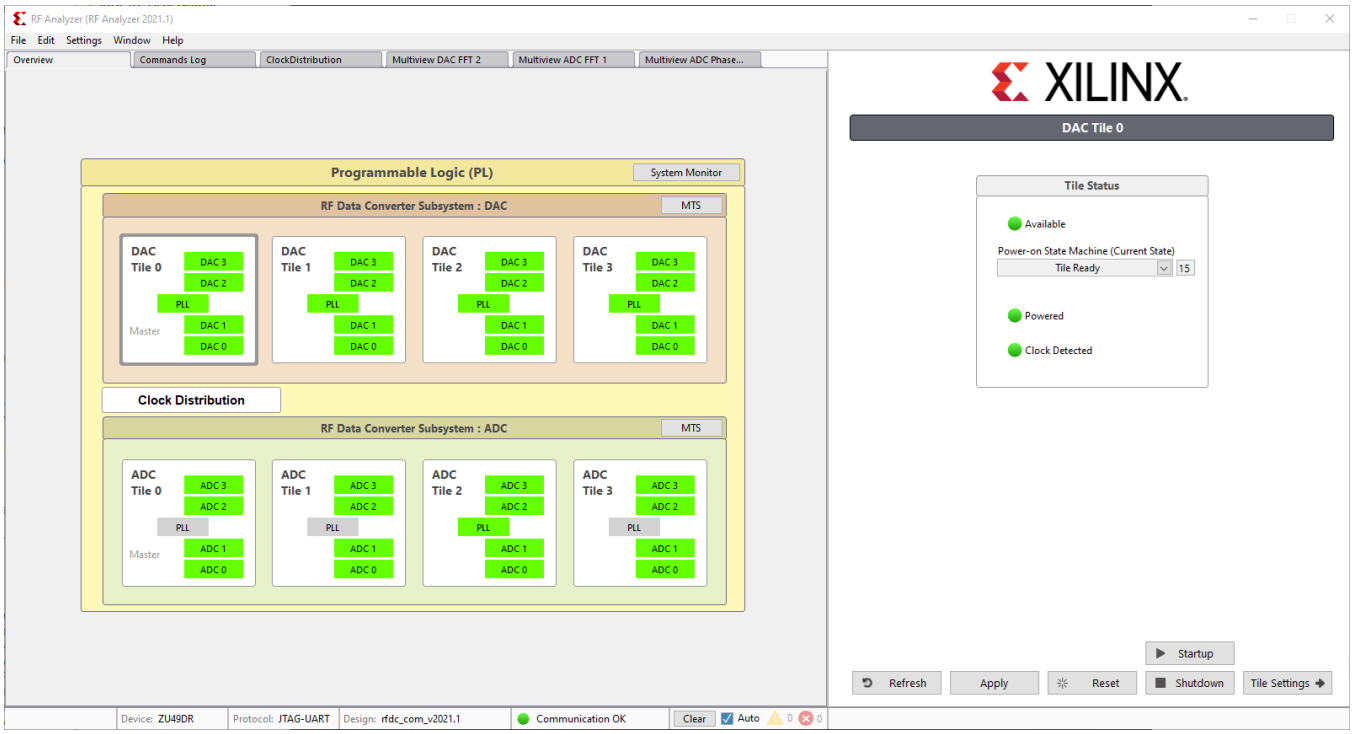
All RF-DAC tiles enable their PLLs to generate the desired sampling clock at 4915.2 MHz.

When the Apply button is clicked, the GUI updates these configurations to the chip, restarts all tiles, reads back status, and updates the GUI. This might take a while and a percentage bar shows the progress.

See the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for more information. The API prevents incompatible clocking configurations.

The following figure shows the tile status based on the clock distribution configurations in this example.

Figure 29: **Tile Status Based on Clock Distribution**

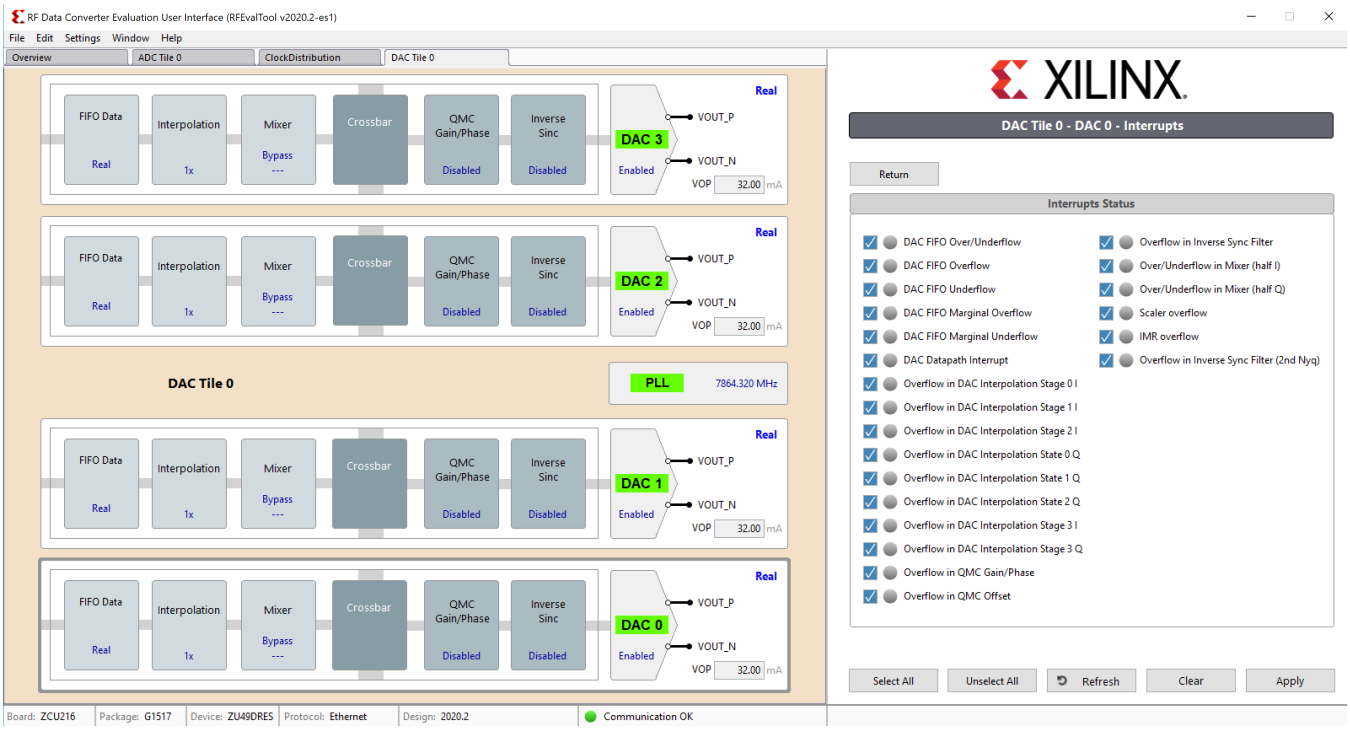


For RF-ADC, only Tile 0 (Tile_226) PLL is enabled, and PLLs in other tiles are disabled. The green channel status shows they are in operation status because these tiles are forwarded the sampling clock from Tile 0. For RF-DAC, all PLLs are enabled because Tile 0 (Tile_230) forwarded its reference to other tiles. The status of RF-ADCs and RF-DACs reflect the settings in the Clock Distribution page in this example. The PLL status can also be checked in the PLL page for each tile. For Gen 3, the PLL page shows the status only and all the clock configurations rely on this Clock Distribution page, which is different from the PLL page in Gen 1 and Gen 2.

Interrupts

Click the **Interrupts** button to display the page shown in the following figure (this example is for RF-DAC).

Figure 30: **Interrupts Status Page**



The check box at the beginning of each row enables or disables (masks) the corresponding interrupts status. Click the **Apply** button to apply the selected interrupts status.

The **Refresh** button reads back the current status and the green light shows which corresponding interrupt bit is set.

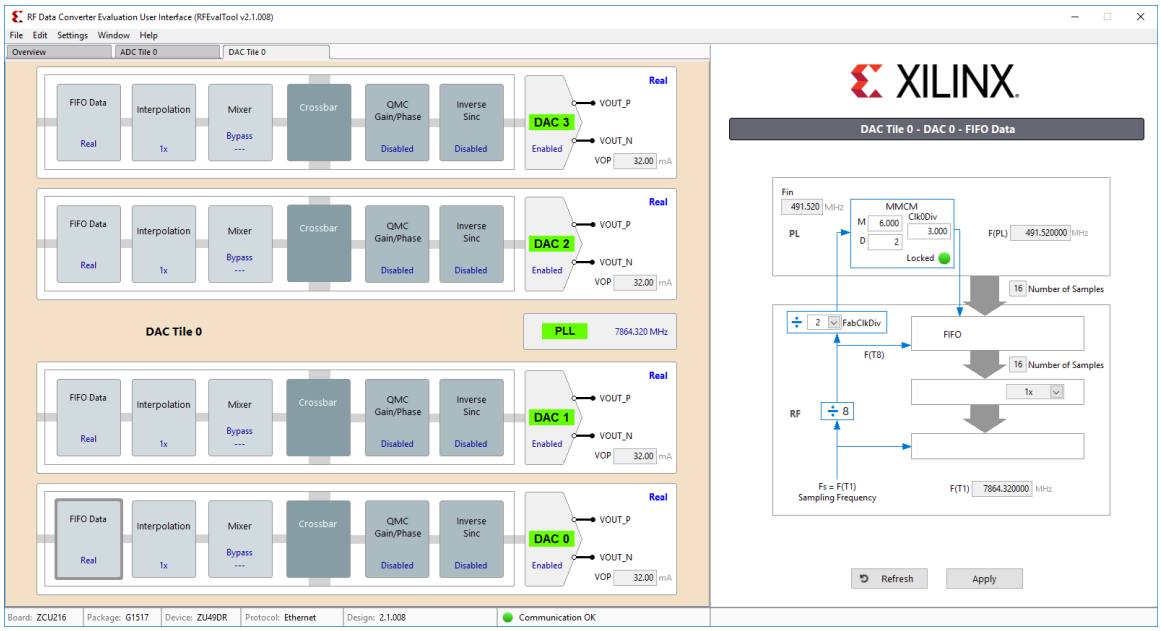
The **Clear** button attempts to clear all interrupt bits and read back the status.

RECOMMENDED: *It is good practice to check the interrupts status and solve the root cause if an interrupt bit has been set before generating or receiving data. For example, the FIFO or datapath overflow can corrupt data and provide an incorrect result.*

FIFO Data

Click **FIFO Data** in any RF-ADC or RF-DAC channel to see the clock relationship of the converter tile, PL interface, and related MMCM configuration.

Figure 31: **FIFO Data**



***Note*:** The clock scheme is tile based, which means all converter channels in one tile share the same clock scheme.

***Note*:** In an MTS enabled bitstream, all RF-ADC tiles share one MMCM module in ADC Tile-0. All RF-DAC tiles share one MMCM module in DAC Tile-0. Values in the FIFO Data page of other tiles are invalid.

The following values are configurable in the FIFO Data page.

- **FabCLKDiv:** In a non-MTS bitstream, the converter sampling clock (Fs, also called T1) is divided by 8 or 4 and then divided by FabCLKDiv. The output goes to the MMCM module as an input reference.
- **M, D, and ClkDiv:** In the MMCM module, the MMCM generates a read or write clock for the FIFO on the PL side, which is shown as F(PL) in the FIFO Data page. The following formula can be used to calculate the PL FIFO clock.

  $$F(PL)=Fin*M/D/ClkDiv$$

***Note*:** The VCO in the MMCM has a limited frequency range requirement. See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926) for the VCO frequency range for different devices.

The proper values for the FIFO related clock configurations are set automatically based on user configuration in the clock distribution page and converter configurations. Generally, these values do not need to be changed.

XILINX

Chapter 3

RF Analyzer

Overview

The RF Analyzer provides an easy and fast way to evaluate the performance of RF-ADCs and RF-DACs in the Zynq® UltraScale+™ RFSoC. The bitstream is independent of the evaluation board and external devices, thus the following board related configurations are not available in the GUI.

- Power settings
- External clock settings
- Programmable logic (PL) settings

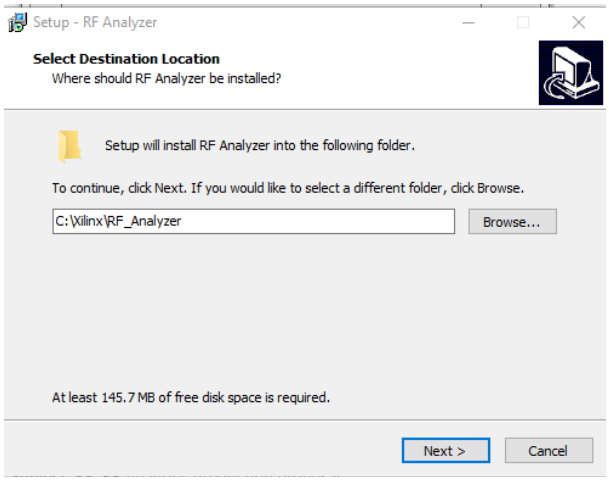
Working with the RF Analyzer

The RF Analyzer requires that either the 2020.1 HW server (or later version) or the Vivado® Design Suite (2020.1 or later version) is installed on the host. Ensure that the external clocks are stable before downloading the bitstream based on the actual hardware design. The corresponding converter tiles might show an error if there are no valid clocks available when the converter IP starts up.

Note: When using the RF Analyzer with Xilinx® evaluation boards, the System Controller User Interface (SCUI) tool can be used to configure the onboard clocks. See the *ZCU111 System Controller – GUI Tutorial* (XTP517) for details.

Installing the RF Analyzer

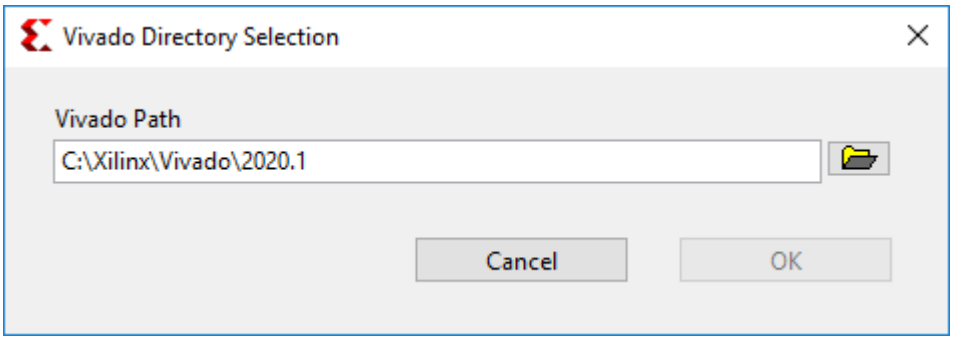
1. Double-click `Setup_RF_Analyzer_<version>.exe` (you might have to right-click and select **Run as Administrator**).
2. Select the folder where the RF Analyzer is to be installed and then follow the instructions on the following screens.



Setting the Vivado Path

When the RF Analyzer starts up for the first time, it looks for the Vivado Design Suite. If there is no Vivado Design Suite or HW server directory specified in the `RF_Analyzer.ini`, a window asking for the path of Vivado Design Suite pops open.

1. In the Vivado Directory Selection, browse to the folder where the Vivado Design Suite or HW server is installed.

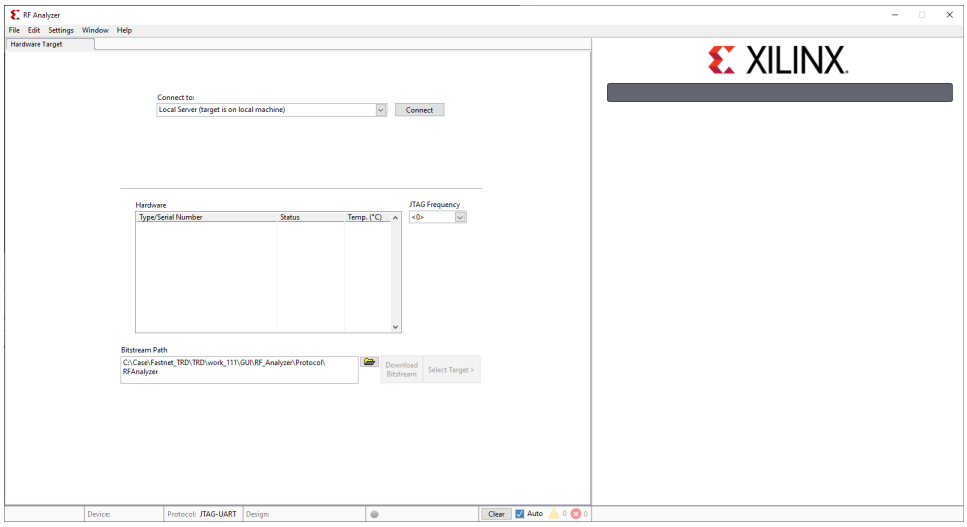


2. Click OK. This directory is recorded in the `RF_Analyzer.ini` for further applications.

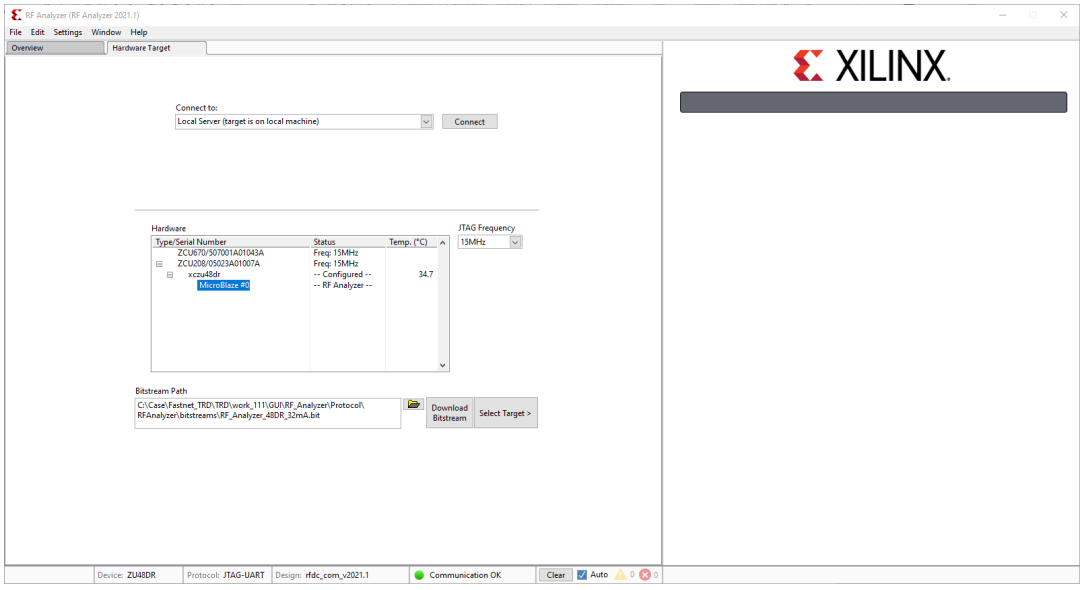
Selecting the Hardware Target and Bitstream

If you have set up the cable for JTAG access, you can use the RF Analyzer start screen to configure and work with the hardware target. This is the same communication method that is used by the Vivado tools.

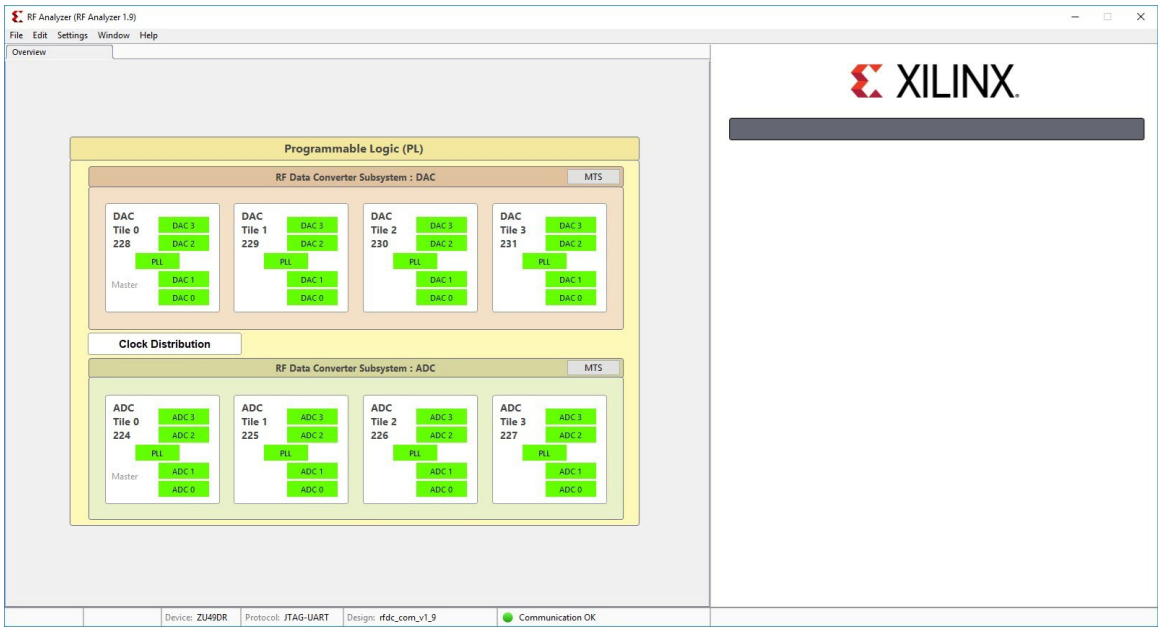
Figure 32: **RF Analyzer Start Screen**



1. In the Connect to: dialog box, select the connection type as Local or Remote. Click **Connect**.
2. In the Hardware dialog box, you can see the automatically detected cables and JTAG chain.
3. In the Bitstream Path dialog box select the bitstream. A pre-built bitstream for each supported part is available in the install folder under `\Protocol\RF_Analyzer\bitstreams\`. These bitstreams provide the maximum RF configuration flexibility. You can also use your own bitstream by customizing and generating the RF DC IP in the Vivado® Design Suite (see the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for information on generating the RF Data Converter IP core).



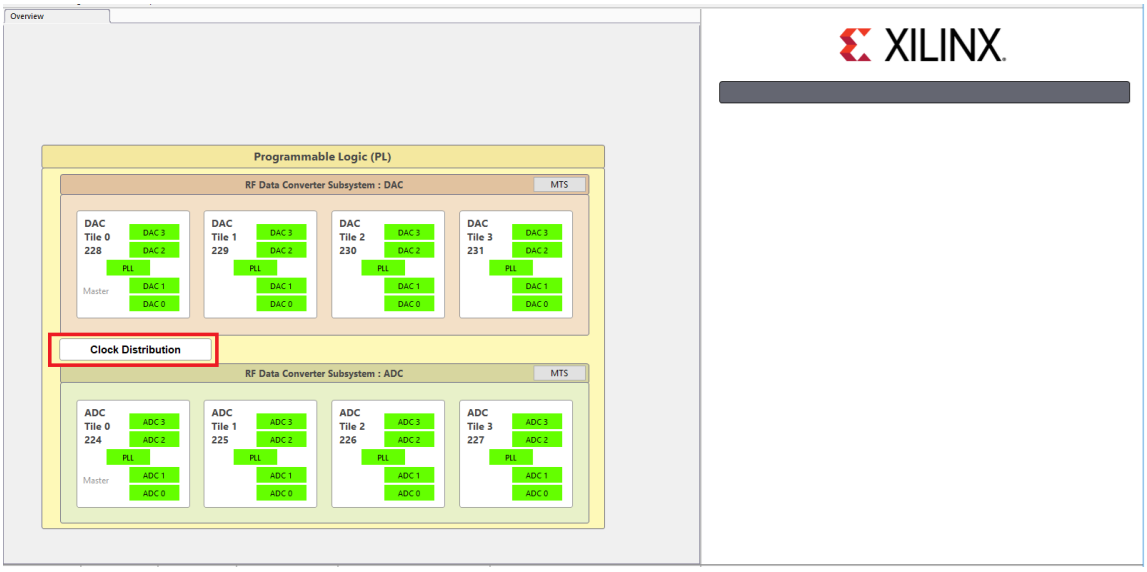
After the bitstream download is complete, select MicroBlaze™ as the target. The RF Analyzer sets up a connection with the Zynq® UltraScale+™ RFSoC, and refreshes the status of the GUI. The following overview page shows up if there are no errors. Device information and the green communication OK bulb appears on the status bar at the bottom of the overview page. The active RF-ADC or RF-DAC tiles might be different based on your actual hardware configuration.



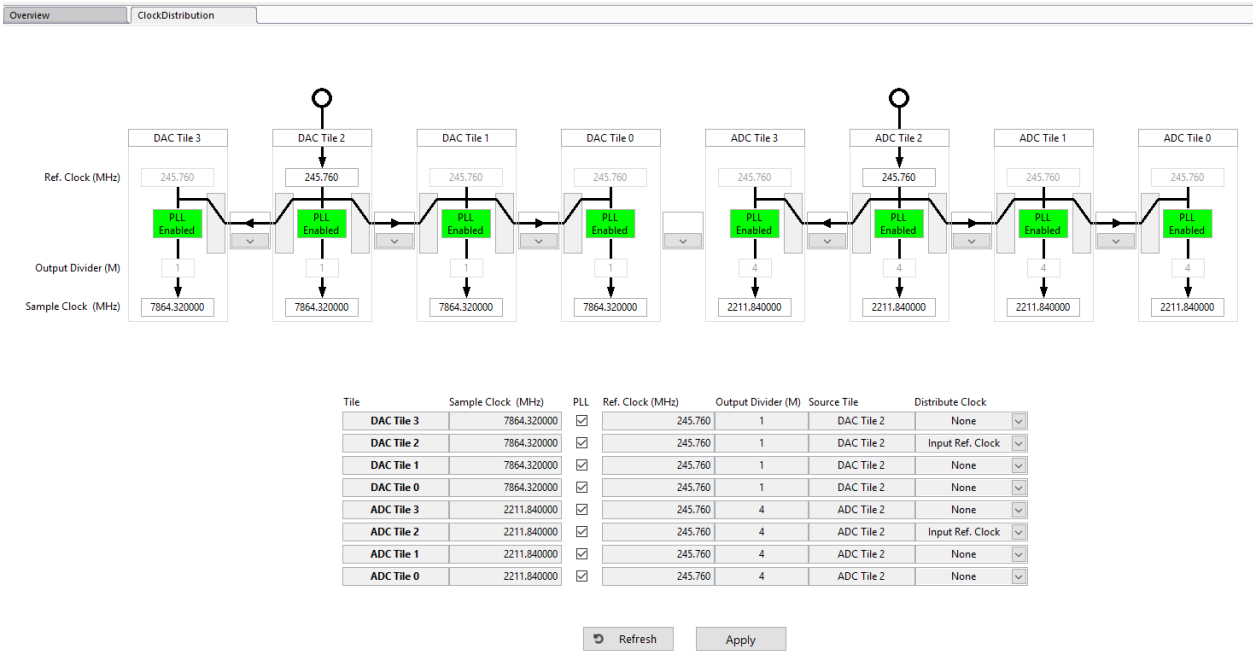
Configuring the Sample Clock

The RF Analyzer acquires the absolute values of tile input clocks and sampling clocks from the IP configuration. Consequently, if the board clocks are different to the initial IP configuration, it is important to configure the sampling clocks before other operations.

1. Click **Clock Distribution**.



2. Select the PLL and configure the clocks based on the board setup.



See *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for information on the permitted clocking configurations for your RFSoC device.

RF Analyzer Tool Menu Options

File Menu Options

- **File → Load/Save configuration:** Configuration covers all the displayed settings of the Zynq® UltraScale+™ RFSoC such as, real or I/Q mode, mixer settings, and enable or bypass internal PLL. All these settings can be saved and restored. This feature enables quick configuration as well as configurations that can be shared with others. Configuration files are located in the `\Config\` directory by default, with the file extension of `.cfg`.
- **File → Load/Save preferences:** Preferences are the user-defined settings of the GUI. It includes tabs used for data generation, data capture, and user options in the GUI that are not linked to the device under test (DUT) configuration such as, mapping in the MultiView mode, number of samples, and tone frequency. You can save the preferred settings of GUI or restore any of them. Preferences files are located in the `\Config\` directory by default, with the file extension of `.prf`.
- **File → Hardware target:** RF Analyzer only. Opens the bitstream download screen.
- **File → Export ADC Data:** This command exports the RF-ADC data captured of all the opened RF-ADC channels with LVM or TDMS file format (chosen in **Settings → Data File Format**). The default directory is `\Data\ADC\`.
- **File → Exit:** Exit the software.

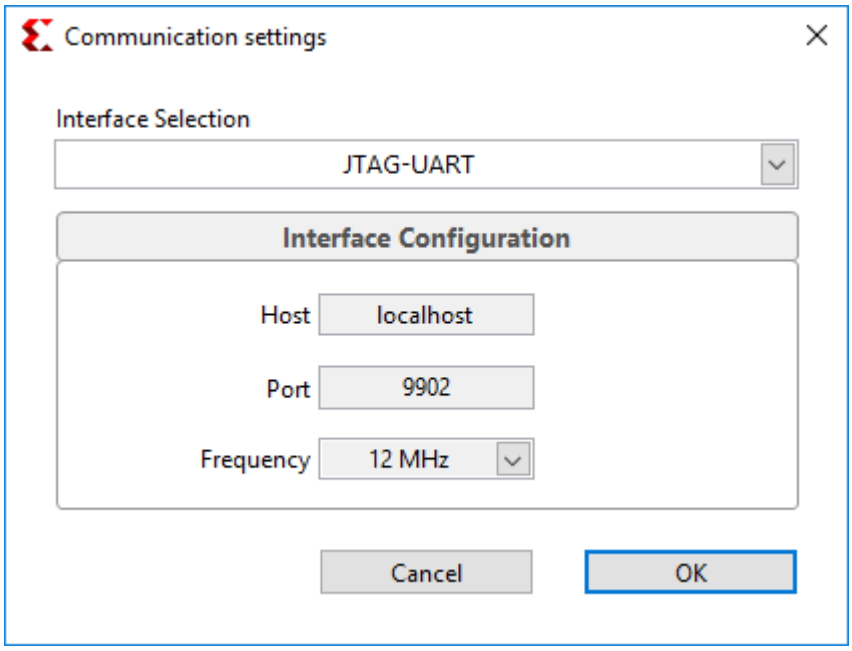
Edit Menu Options

- **Edit:** Standard Windows edit menu.

Settings Menu Options

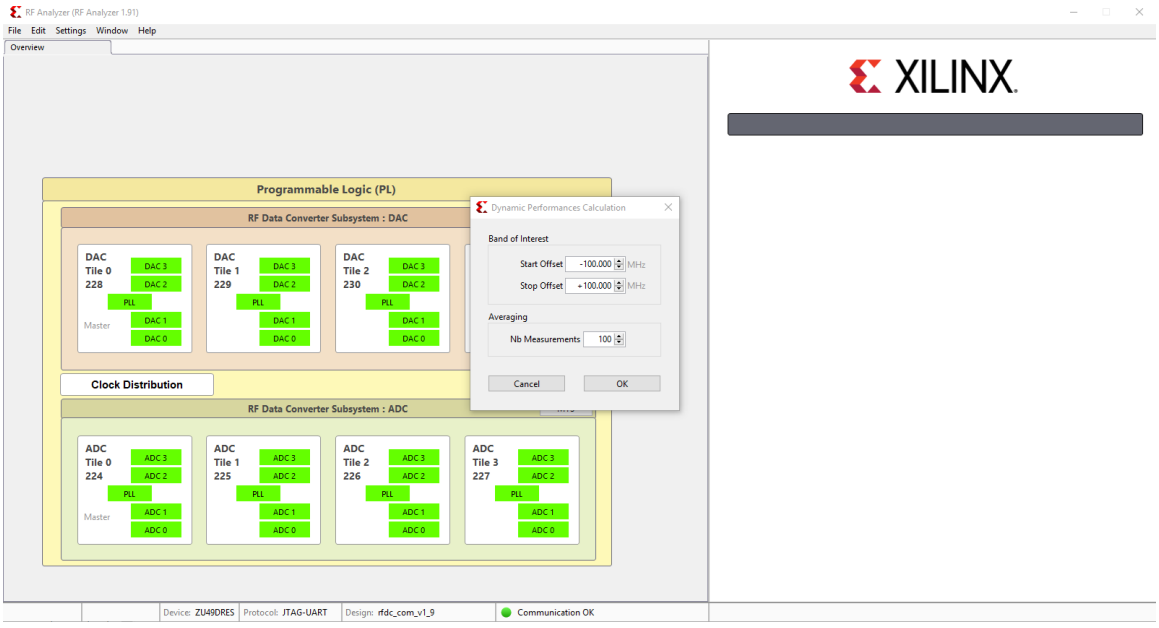
- **Settings → Communication:** Displays the current communication interface. JTAG-UART is used for the RF Analyzer.

Figure 33: **Communication Interface**



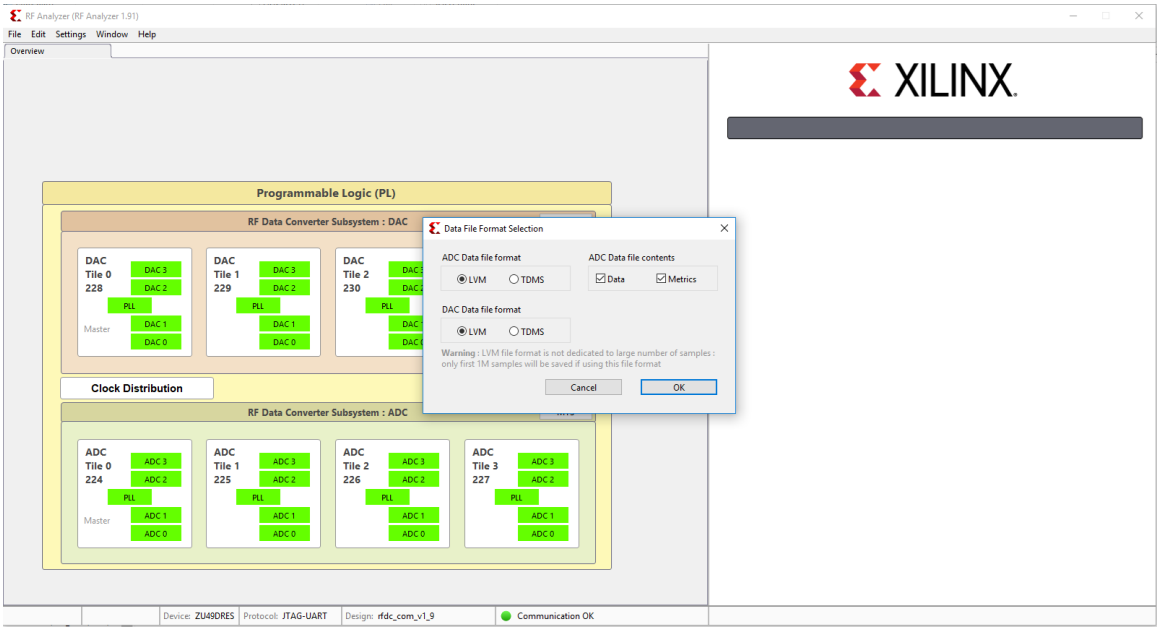
- **Settings → Dynamic Performances:** Some RF-ADC metrics are based on the frequency range. On the RF-ADC FFT page, there is a marked-out calculation table, the SNR, ENOB, SFDRxH23, and FspurxH23 are calculated based on the Band of Interest set here. In loop mode, some metrics are calculated over a number of measurements that can be set under Averaging.

Figure 34: **Band of Interest**



- **Settings → Data File Format:** Indicate your preferred file format between the .lvm and .tdms formats. For the RF-ADC output, you can individually select whether Data or Metrics is exported.

Figure 35: **Data File Format**

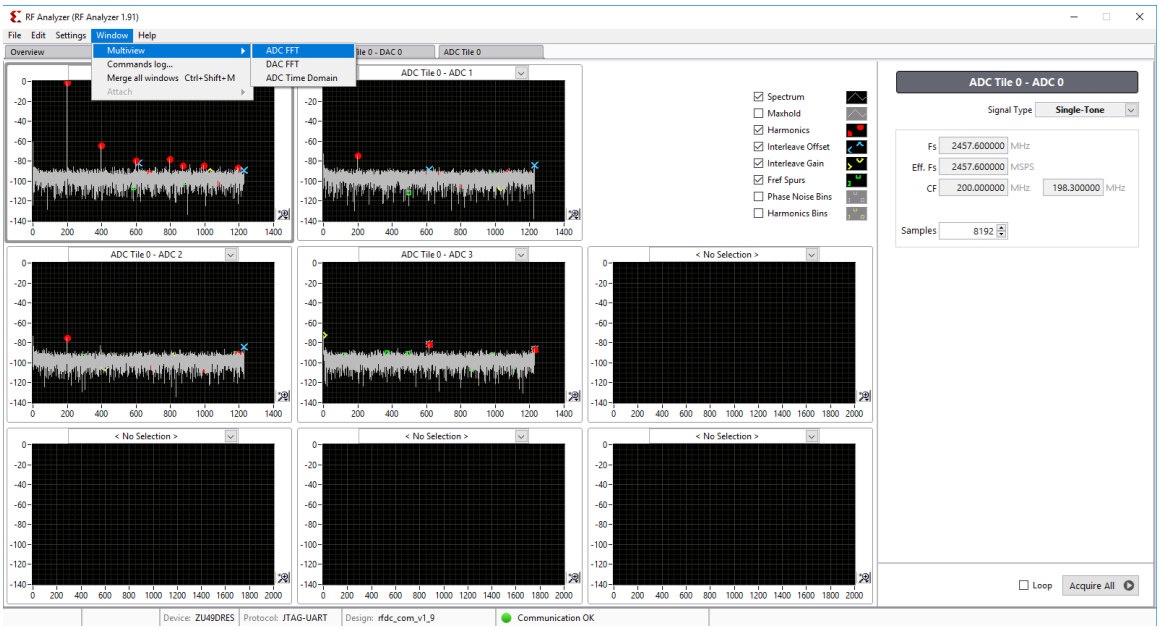


- **Settings → Data Folders:** Select your preferred folders for the test vector of RF-DAC, saved data from RF-ADC, and onboard clocking frequency configuration files. By default, these are located in `\Data\`, with ADC, DAC, and Clocking as the respective folder names.

Window Menu Options

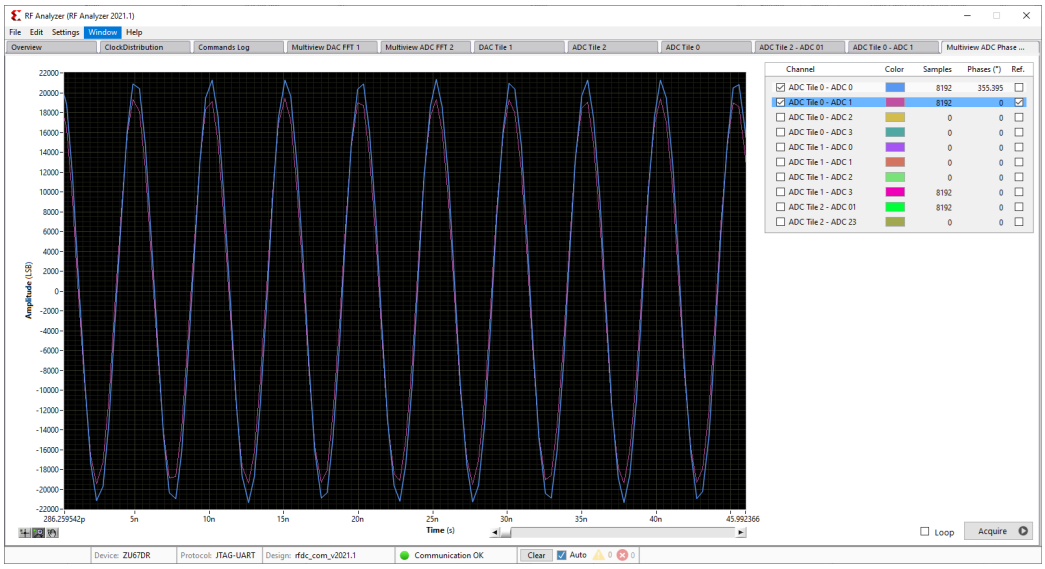
- **Window → MultiView:** The MultiView option makes it possible to view several of the RF-ADC or RF-DAC FFT diagrams on a single page with customized channels. Click **Generate/Acquire All** to update all the windows.

Figure 36: **MultiView RF-ADC FFT**



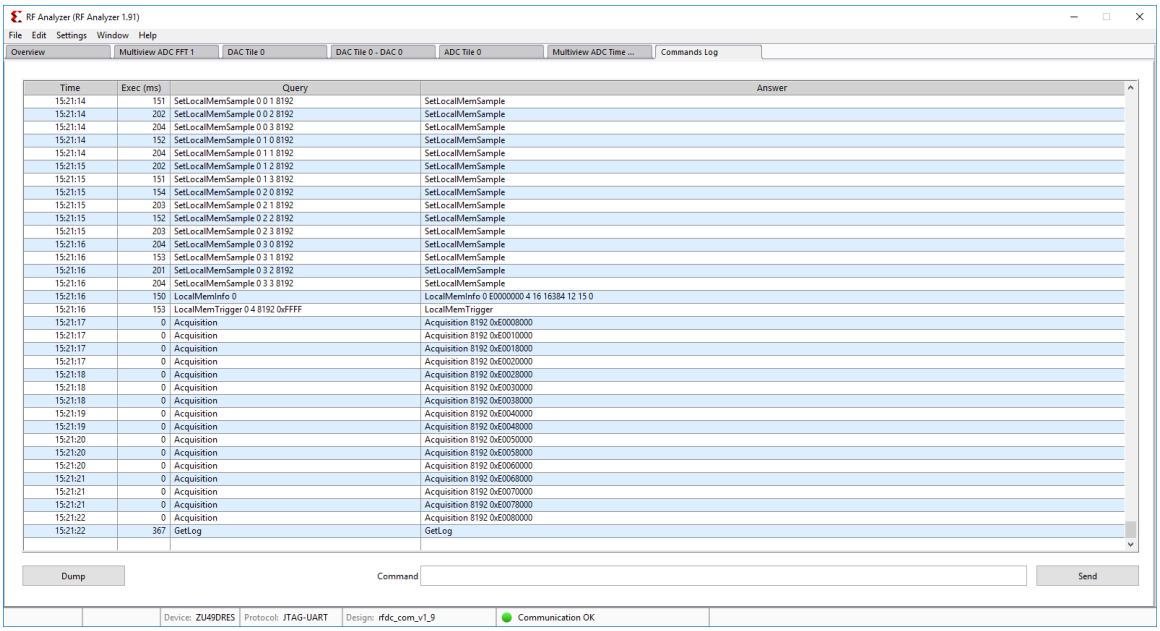
To display all the RF-ADC channel signals in the time domain, select the **ADC Time Domain** option. The phase between channels is displayed, relative to the reference channel.

Figure 37: **MultiView RF-ADC Time Domain**



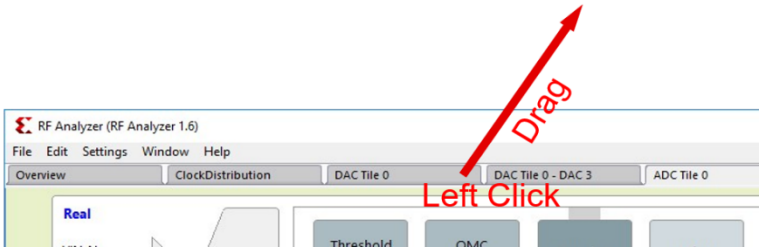
- **Window → Commands log:** This opens the commands log window where the history for all the commands can be seen, the API can be run, and feedback can be viewed. If an error occurs with the GUI, it appears on the command log. The command log window can also be used to create a dump file which lists out all the previously used commands. This can be useful in debugging if an error occurs with a sent command.

Figure 38: **Command Window**



- **Window → Merge all windows:** Opened tabs for DACs or ADCs can be moved to separate windows with a left-click and drag on the tab area as shown in the following figure. This command merges all the separate windows into one.

Figure 39: **Create Separate Windows**



- **Window → Attach:** Opened tabs can be moved to separate windows. This command merges back selected separate windows.

Help Menu Options

- **Help → About:** Provides general information about the RF Data Converter evaluation tool. Use this option to check the version, which is used when building the `.lvm` file.

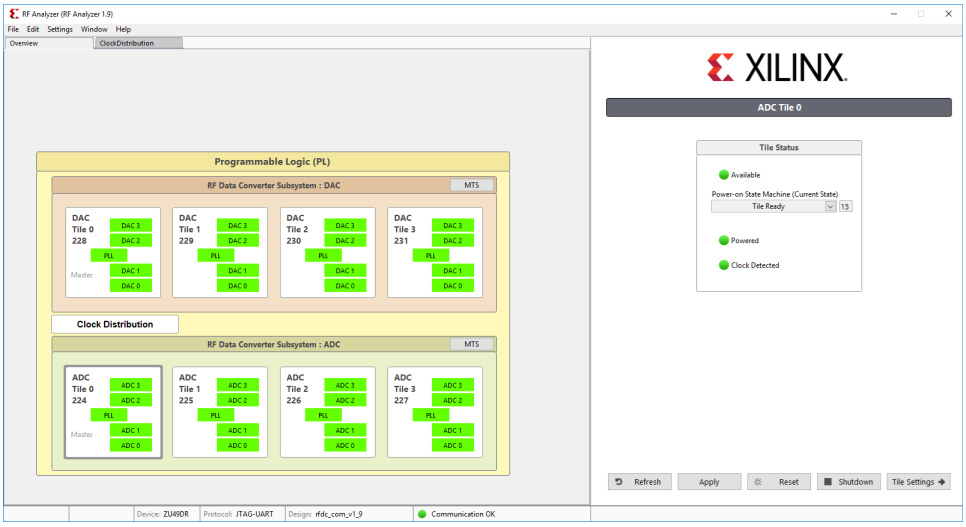
RF Analyzer Tool Tabs

The Overview page is the home page of the RF Data Converter analyzer tool GUI. It displays the top framework of all the converters grouped by tile. This page is displayed upon start-up and cannot be closed.

Overview

The overview page is similar to the RF Evaluation Tool but the memory type is not selectable because DDR (DRAM) storage is not supported.

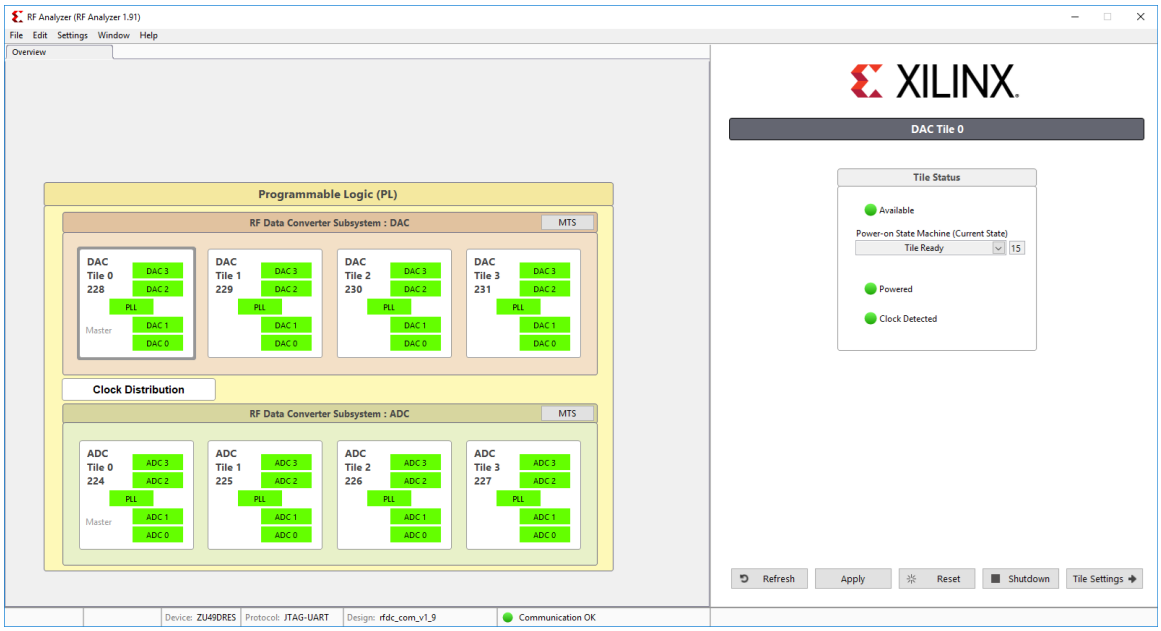
Figure 40: **Overview Page**



RF-ADC/RF-DAC Tile

In the overview tab, selecting any of the RF-ADC or RF-DAC tile opens the individual tile page as illustrated in the following figure. In this tab, you can reset, shut down, start up a tile, and also view the current tile status by clicking **Refresh**. When a tile is in operation, selecting **Tile settings** opens up the configuration tab for it. Refer to the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for more information on the commands and power up state machine status.

Figure 41: **Tile Status**



Tile PLL Settings

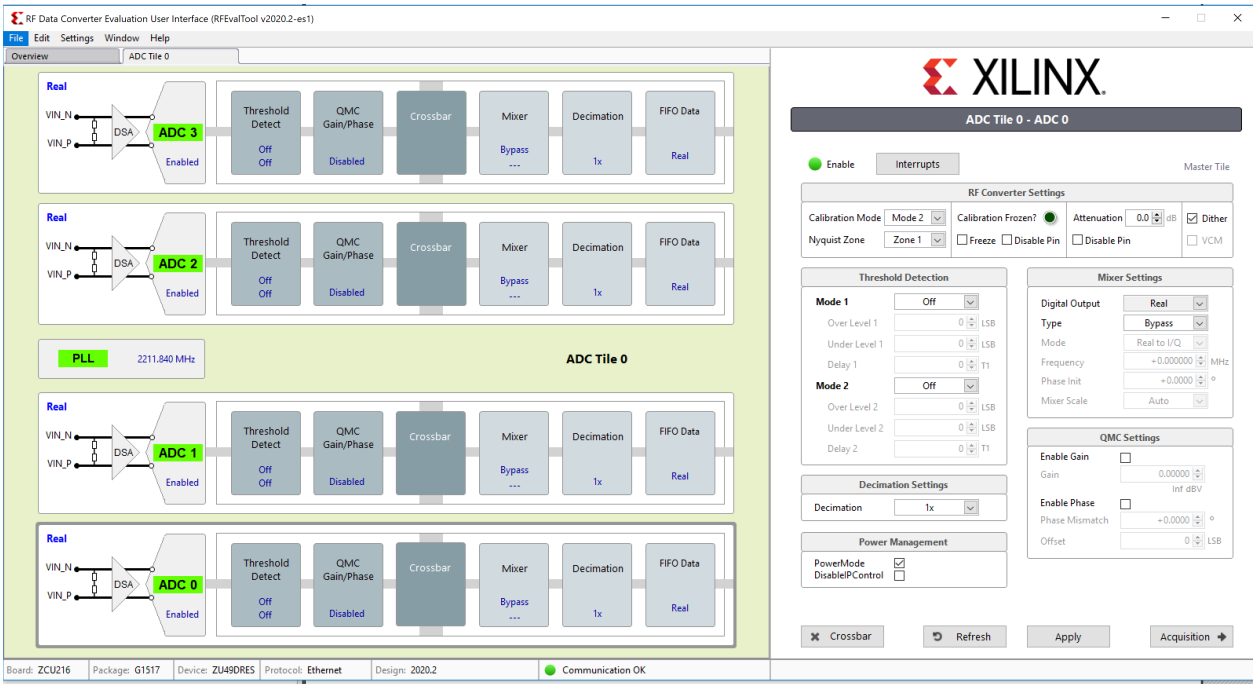
Click on PLL in the tab for a DAC or ADC to see a diagram that illustrates the PLL setup for that tile.

Figure 42: **Tile PLL Settings**

Converter Settings

In each RF-ADC/RF-DAC tile, the available converter channels and associated internal function blocks are cascaded in the block diagram, and the text shows the current settings. Click any function block to open the config page in the right panel. FIFO and Crossbar have their own separate pages.

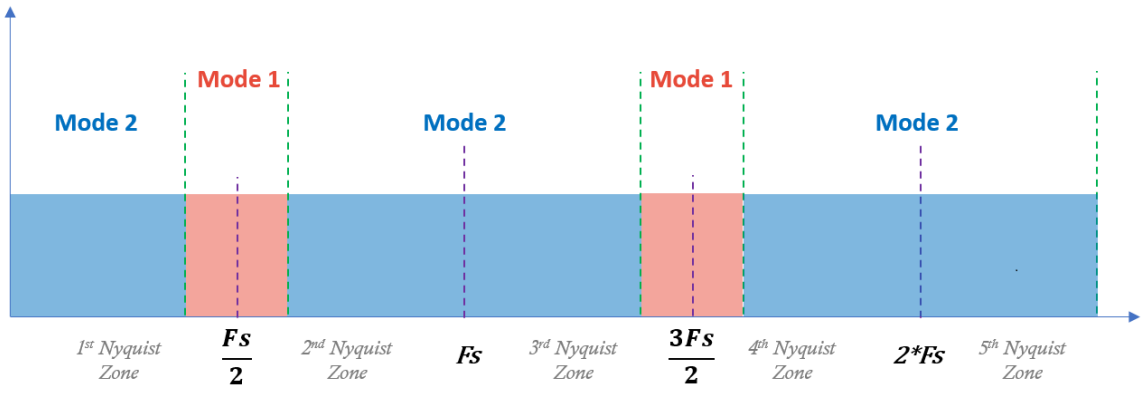
Figure 43: **Converter Settings**



RF-ADC Settings

- **Calibration Mode:** Selects between different calibration optimization schemes depending on the features of the input signals. Mode 1 is optimal for input frequencies $F_{samp}/2$(Nyquist) +/-10%. Otherwise, use Mode 2 or AutoCal (Gen 3 only).

Figure 44: **Calibration Mode**



- **Nyquist Zone:** Choose the Nyquist zone in which the input signal is located. This is related to interleaving calibration and must be indicated correctly. Zone 1 is for odd numbered zones and Zone 2 is for even numbered zones.

- **Threshold Detection:** Use this to set the embedded threshold detection parameter.

- **Decimation Settings:** Use this to select the decimation factor. Xilinx recommends using the same decimation factor for all data converters in the tile to avoid potential timing issues at the interface.

  ***Note*:** Do not select Off or you will not receive any data.

- **Calibration Frozen:** Use this to freeze the interleaving calibration for each channel. The green light indicates a frozen status. The freeze function freezes or unfreezes the interleaving calibrations. The disable pin function can disable the calibration freeze real-time port control.

The following functions are for Gen 3 only.

- **Attenuation:** Attenuation value of on-chip DSA in dB for each RF-ADC channel. The disable pin can disable the DSA pin control.
- **Power Management:** Use to power down or power up a single channel within a tile.

RF-DAC Settings

- **Decoder Mode:** Choose which performance to optimize: noise floor or linearity. Noise floor optimization must be selected for communication applications.
- **Nyquist Zone:** Choose which Nyquist zone the signal will be located in: Normal Mode for Nyquist zone one and Mix Mode (Gen 3 only) for Nyquist zone two. See this link for more information.
- **Interpolation Settings:** Choose your interpolation factor.

  ***Note*:** If you select Off, some digital blocks will be powered down and the outputs will not be active.

- **Inverse Sinc Settings:** Enabling Inverse Sinc compensates sinc roll-off at high frequencies. This function is only effective when the signal is located in Nyquist zone one.

The following functions are for Gen 3 only.

- **DataPath:** The drop-down box used to choose datapath modes. The four available modes are Full Nyquist DUC, IMR low pass, IMR high pass, and DUC bypass.
- **Current:** The VOP current value. This value is also displayed on the diagram of each channel.
- **Power Management:** Use to power down or power up a single channel within a tile.

Settings Common to RF-ADC and RF-DAC

- **Mixer Settings:** Xilinx recommends setting the Crossbar page first, and then set other parameters of the mixer and NCO because the mixer is bypassed in the real-to-real mode.

- **QMC Settings:** QMC module contains gain, phase, and DC-offset adjusting. These are used to compensate unmatched I and Q signal path when converters interface to external modulators or demodulators. DC offset takes effect with DC coupling only. Phase offset takes effect with complex mode only. Gain takes effect in all modes.
- **FIFO:** Show the FIFO clock rates and number of words on PL and converter side for information only.

Crossbar

Click the **Crossbar** button at the bottom of the converter settings page, or, alternatively, the **Crossbar** box in the left panel to display the crossbar page. This page determines the real or complex mode of the mixer and multi-bands operating mode. Complex mode activates a pair of channels to support both in-phase(I) and quadrature(Q) signal. Because of the complex mixer (and NCO) architecture, the real-to-complex (R2C) or complex-to-complex (C2C) mode is allowed, but complex-to-real (C2R) mode is not allowed. This means that there is no C2R mode available for RF-ADC and no R2C mode available for RF-DAC. Correct operating modes are ensured by this tool. In complex mode, even channels are always used for I signals and odd channels are used for Q signals.

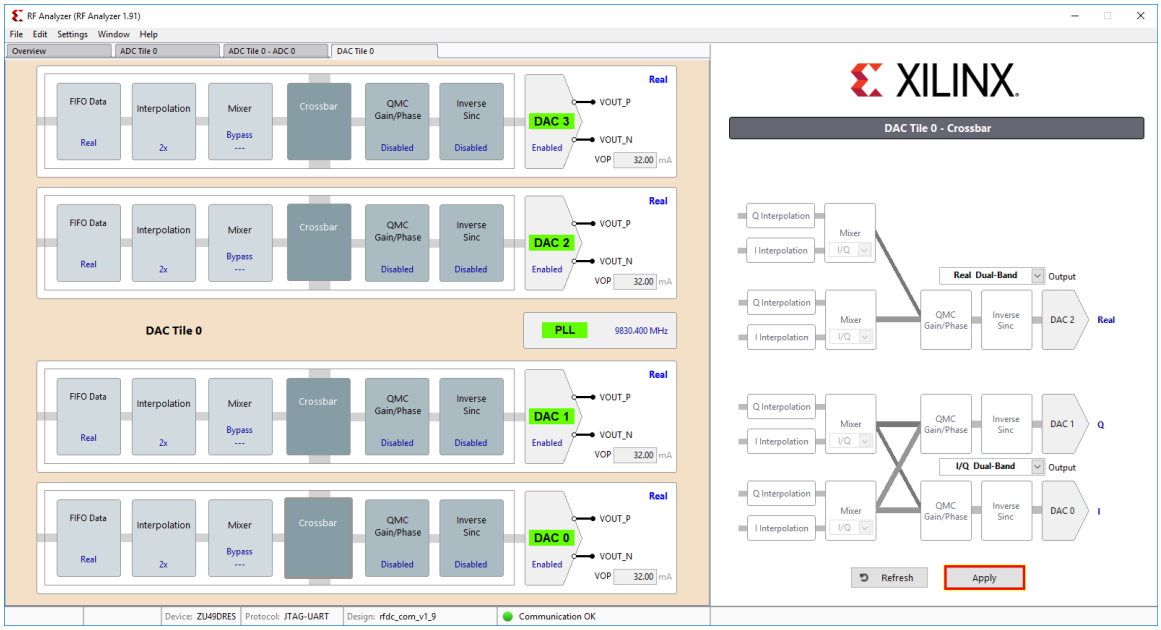
Figure 45: **Crossbar**

Multi-Bands

Multiple bands enable one RF-DAC or RF-ADC analog channel and share multiple DUC or DDC channels to transmit or receive the multi-band carrier signals. For RF-DAC, multiple baseband signals can be up-converted in separate DUC chains and then combined at the crossbar before being sent to the analog RF-DAC block.

In RF-ADC, the multi-band/carrier inputs from one RF-ADC are split into multiple DDC paths for down-conversion. The carriers from different bands are separated and located at low frequencies (in general at zero). In the multi-bands operation, a converter is enabled on channel 0 (dual bands at channel 0 and 1) or channel 2 (dual bands at channel 2 and 3). Multi-bands operations support both real and complex output. All these configurations can be enabled at the crossbar page. The following figure illustrates the dual bands configuration of C2C and C2R.

Figure 46: **Multi-Bands**

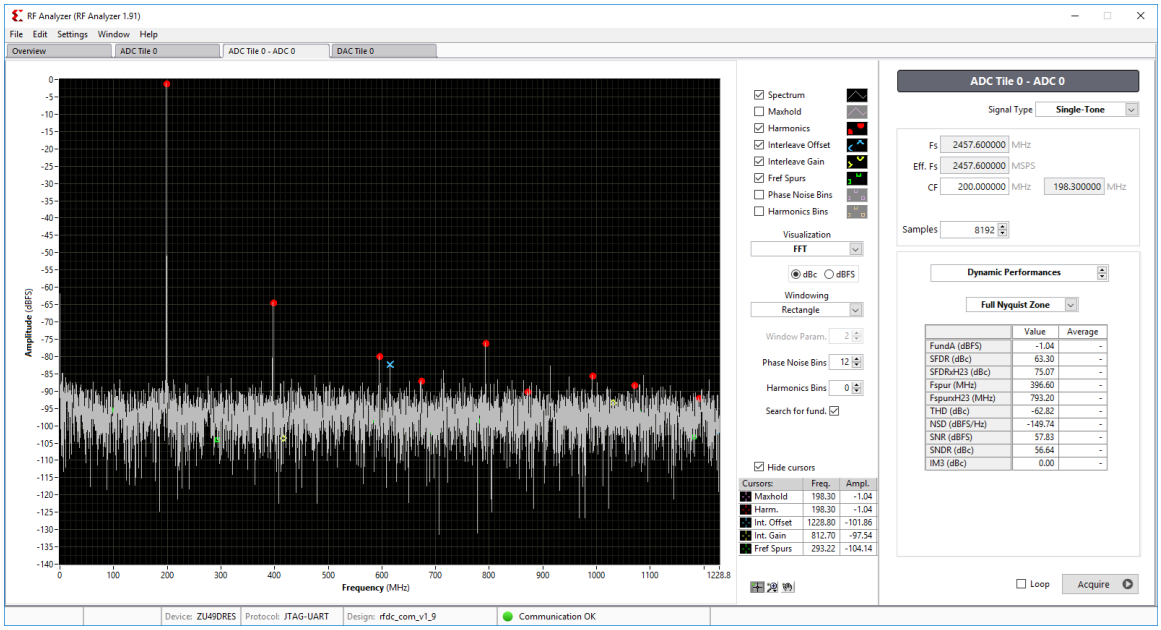


FFT Page

Click **Acquisition** in the ADC settings page, or **Generation** in the DAC settings page, to open the FFT page. In the RF-DAC FFT page, the single tone and dual tone generator is embedded in the software. To generate a complex modulated signal, load a test vector file. There are variations of sub-menus in this page, including signal characteristics, customizing FFT plot, windowing function, test vector input, and output. When decimation or interpolation is enabled in the RF-

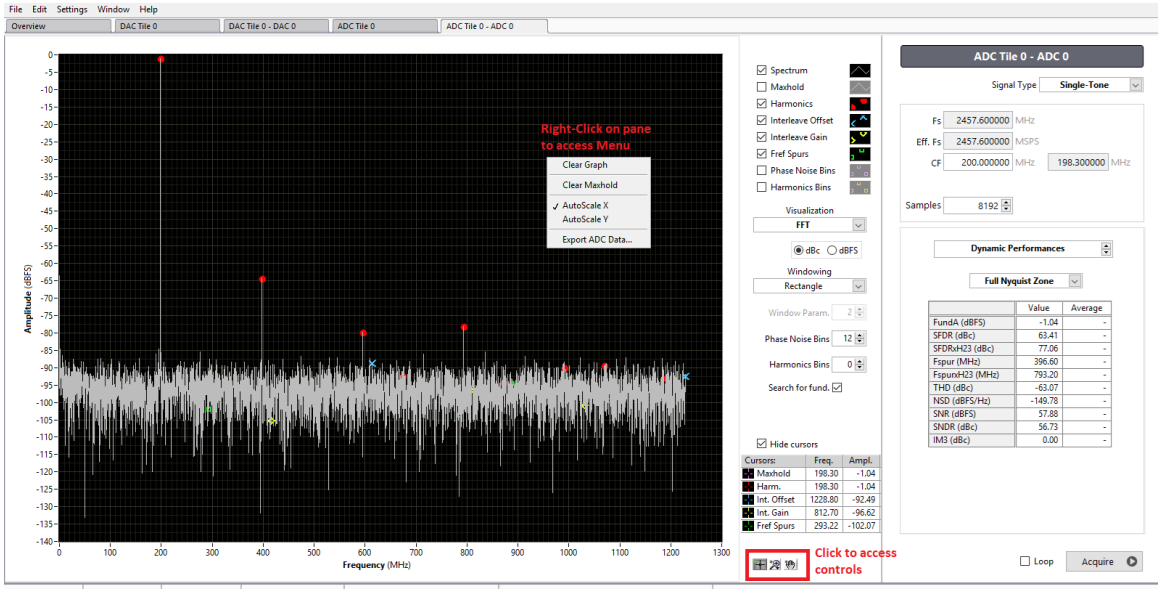
ADC or RF-DAC data path, with a value more than 1 (bypass), Eff.Fs and Fs show different values in this table. Fs indicates the sampling frequency of observed RF-ADC or RF-DAC, Eff.Fs indicates the sampling frequency of original data stream (base band) after decimation or before interpolation. The X-axis (frequency) of the FFT plot reflects back the Eff.Fs. The following figure shows the RF-ADC FFT page.

Figure 47: **RF-ADC FFT Page**



The following figure shows the Zoom Tools on the FFT page. Use the default Zoom Tools or edit the axis range to directly configure the start and/or end values for best plot observation.

Figure 48: **FFT Zoom Tool**



Multi-Tile Synchronization

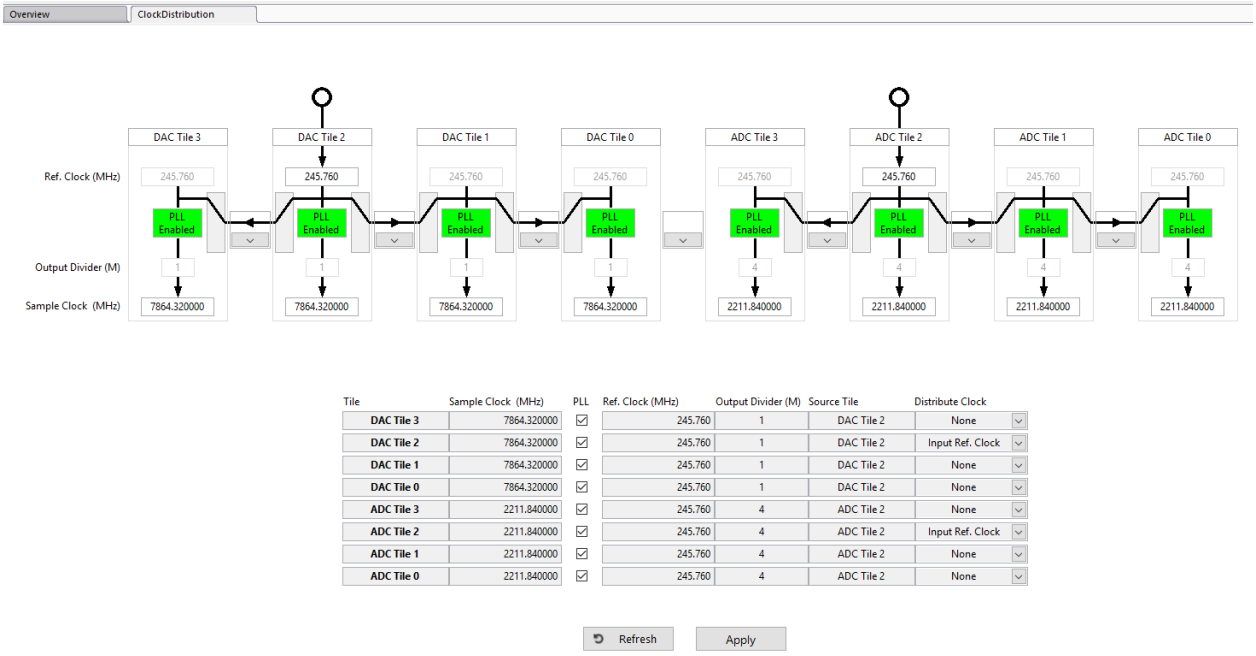
The multi-tile synchronization (MTS) feature enables multiple converter channels working with an aligned and deterministic latency across tiles and chips. MTS is only supported in the RF Analyzer with a custom bitstream.

Clock Distribution (Gen 3)

The Zynq UltraScale+ RFSoC Gen 3 supports on-chip clock distribution. For more information, see *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).

Click the **Clock Distribution** button in the overview page to display the page shown in the following figure.

Figure 49: **Clock Distribution**



Note: The settings on this page should comply with the limitations of the on-chip clock distribution system and PLL.

Each tile has four input fields and a check box for an in-tile PLL, as described here.

- **Sample Clock (MHz):** Select the desired sampling rate of converters, which can be generated by the in-tile PLL or a forwarded sampling clock from the source tile.
- **PLL Checkbox:** Enable or disable the PLL in this tile.
- **Reference Clock (MHz):** Enter the reference or a sampling clock, can be from an external input or a forwarded clock from the source tile.

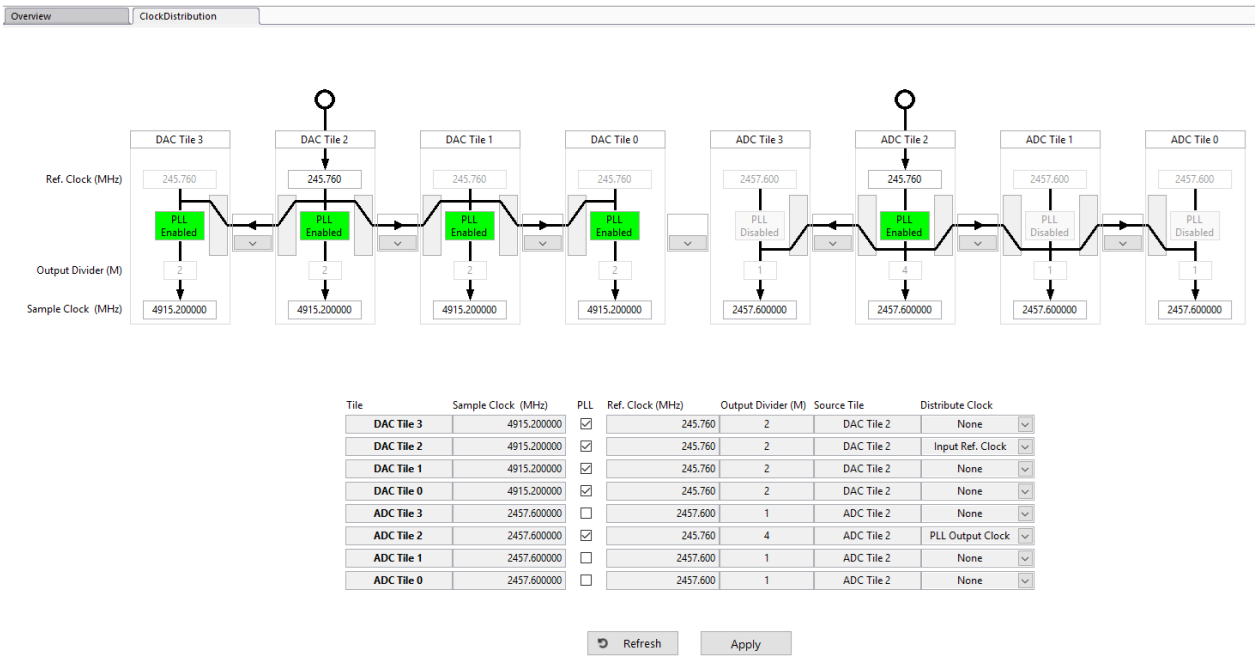
  Note: This frequency can be a reference for the in-tile PLL or the frequency of the sampling clock if it is used directly.

- **Source Tile:** Use the drop-down list to select which tile the clock (reference) comes from. Select the tile itself for the external clock input to this tile, or the source tile for a forwarded clock (reference or sampling clock). Select the tile itself for a source tile.
- **Distribute Clock:** Select options to distribute the clock (acting as source tile) and which clock is distributed:

  1. None: select to not distribute the clock.
  2. Input clock: select to distribute the input clock from an external input. This clock can be a low-frequency reference clock or a high-frequency sampling clock.
  3. PLL output clock: select to distribute the clock generated by the in-tile PLL.

An example configuration is shown in the following figure.

Figure 50: **Example Clock Distribution Configuration**



In this example, two external input clocks (both at 245.76 MHz) are fed to the ADC_Tile_224 and DAC_Tile_228, respectively. All desired RF-ADC clocks are 2457.6 MHz and desired RF-DAC clocks are 4915.2 MHz.

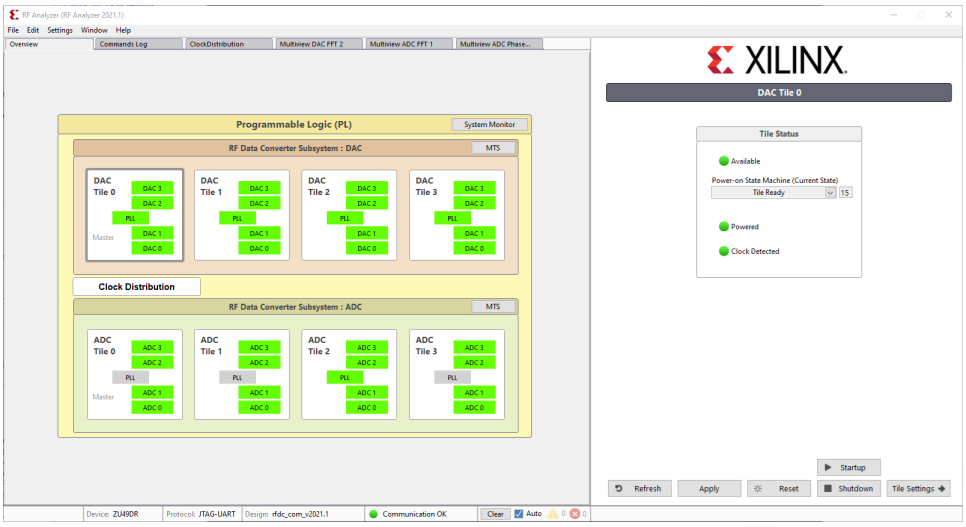
For the RF-ADC group, Tile_224 distributes its *PLL output clock* to other RF-ADC tiles. For the RF-DAC group, Tile_228 distributes its input reference to all other RF-DAC tiles.

All RF-DAC tiles enable their PLLs to generate the desired sampling clock at 4915.2 MHz.

When the Apply button is clicked, the GUI updates these configurations to the chip, restarts all tiles, reads back status, and updates the GUI. This might take a while and a percentage bar shows the progress.

The following figure shows the tile status based on the clock distribution configurations in this example.

Figure 51: **Tile Status Based on Clock Distribution**

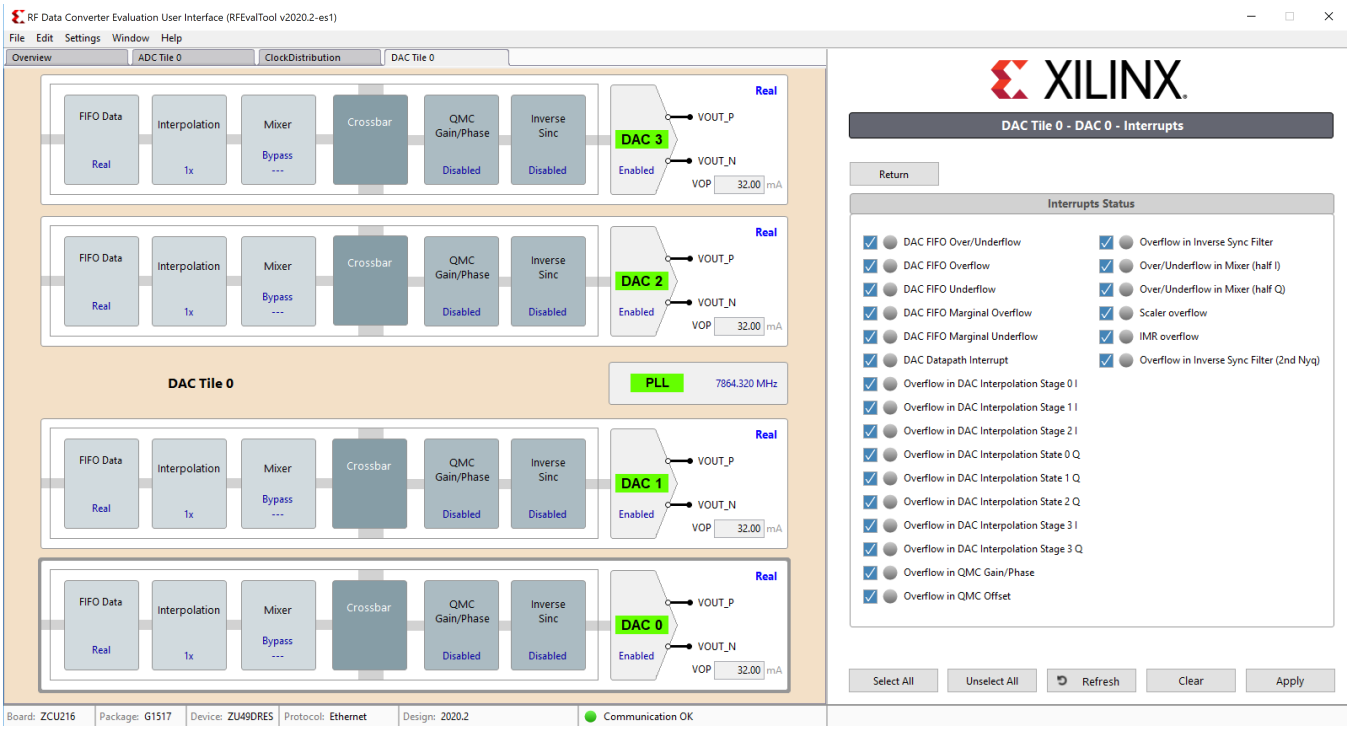


For RF-ADC, only Tile 0 (Tile_224) PLL is enabled, and PLLs in other tiles are disabled. The green channel status shows they are in operation status because these tiles are forwarded the sampling clock from Tile 0. For RF-DAC, all PLLs are enabled because Tile 0 (Tile_228) forwarded its reference to other tiles. The status of RF-ADCs and RF-DACs reflect the settings in the Clock Distribution page in this example. The PLL status can also be checked in the PLL page for each tile. For Gen 3, the PLL page shows the status only and all the clock configurations rely on this Clock Distribution page, which is different from the PLL page in Gen 1 and Gen 2.

Interrupts

Click the **Interrupts** button to display the page shown in the following figure (this example is for RF-DAC).

Figure 52: **Interrupts Status Page**



The check box at the beginning of each row enables or disables (masks) the corresponding interrupts status. Click the **Apply** button to apply the selected interrupts status.

The **Refresh** button reads back the current status and the green light shows which corresponding interrupt bit is set.

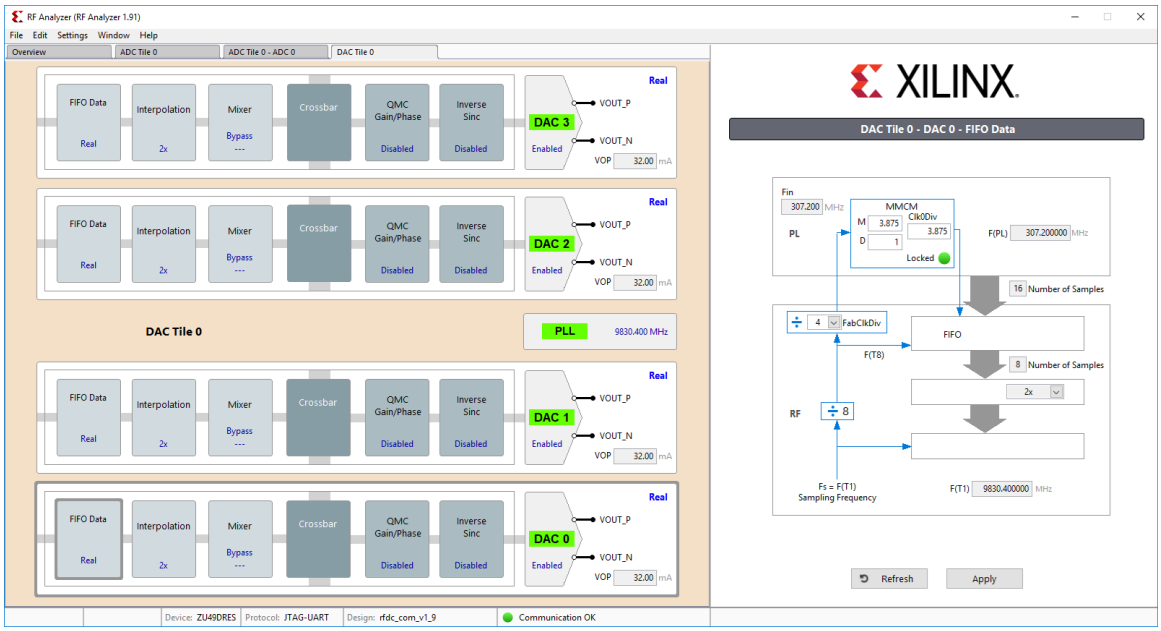
The **Clear** button attempts to clear all interrupt bits and read back the status.

RECOMMENDED: *It is good practice to check the interrupts status and solve the root cause if an interrupt bit has been set before generating or receiving data. For example, the FIFO or datapath overflow can corrupt data and provide an incorrect result.*

FIFO Data

Click **FIFO Data** in any RF-ADC or RF-DAC channel to see the clock relationship of the converter tile, PL interface, and related MMCM configuration.

Figure 53: **FIFO Data**



***Note*:** The clock scheme is tile based, which means all converter channels in one tile share the same clock scheme.

***Note*:** In an MTS enabled bitstream, all RF-ADC tiles share one MMCM module in ADC Tile-0. All RF-DAC tiles share one MMCM module in DAC Tile-0. Values in the FIFO Data page of other tiles are invalid.

The following values are configurable in the FIFO Data page.

- **FabCLKDiv:** In a non-MTS bitstream, the converter sampling clock (Fs, also called T1) is divided by 8 or 4 and then divided by FabCLKDiv. The output goes to the MMCM module as an input reference.
- **M, D, and ClkDiv:** In the MMCM module, the MMCM generates a read or write clock for the FIFO on the PL side, which is shown as F(PL) in the FIFO Data page. The following formula can be used to calculate the PL FIFO clock.

  $$F(PL)=Fin*M/D/ClkDiv$$

***Note*:** The VCO in the MMCM has a limited frequency range requirement. See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926) for the VCO frequency range for different devices.

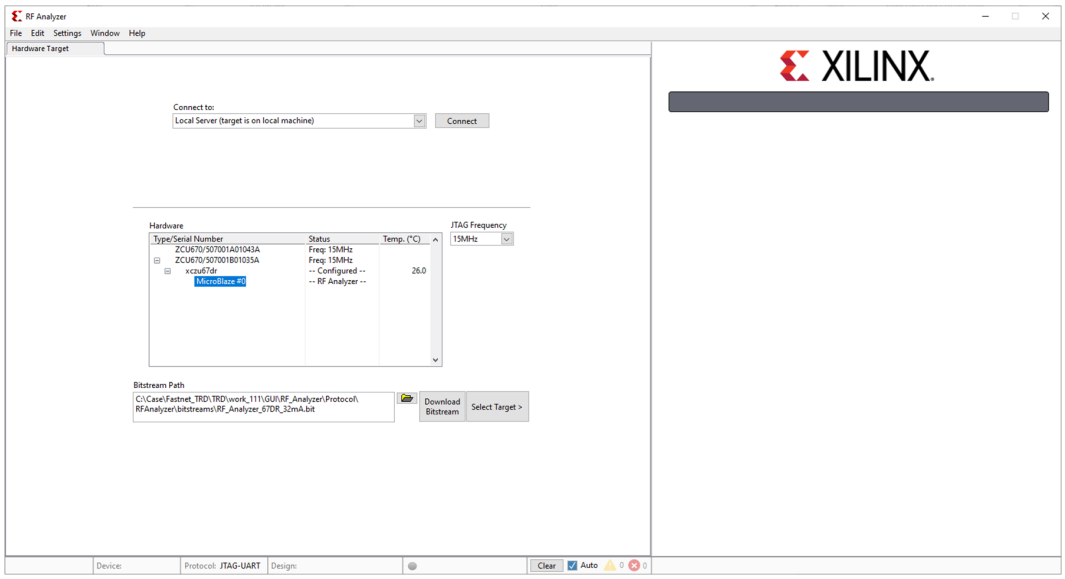
The proper values for the FIFO related clock configurations are set automatically based on user configuration in the clock distribution page and converter configurations. Generally, these values do not need to be changed.

System Monitor

The RF Analyzer can use some of the temperature functionalities of the system monitor.

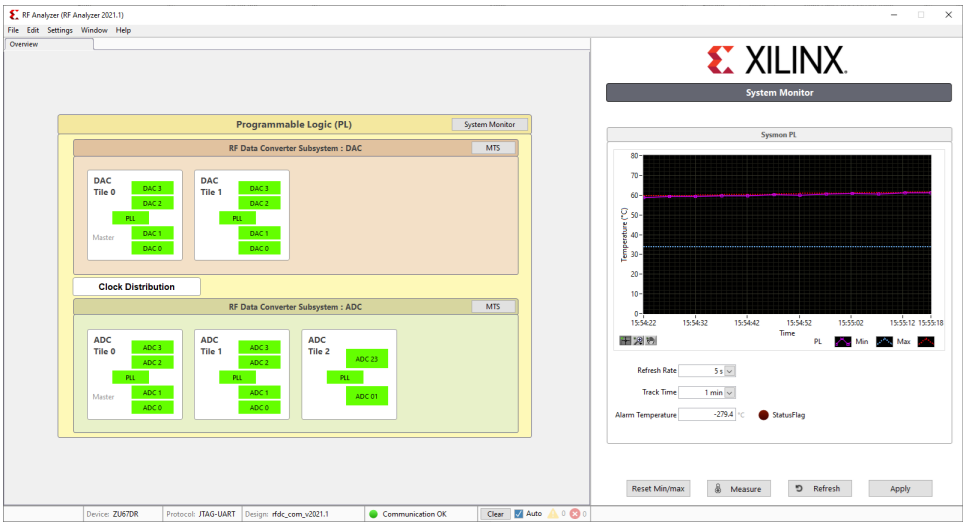
In the Hardware Target tab, the temperature is read and displayed when the Connect button is clicked, as shown in the following figure.

Figure 54: **Temperature Read When Connect Button Clicked**



The System Monitor window is accessible by clicking the System Monitor button on the Overview tab, as shown in the following figure.

Figure 55: **System Monitor**



The System Monitor window shows a graphical view of the current temperature for the period of time shown in the Track Time field. It also shows the maximum and minimum temperature since power up or since the last reset.

The refresh rate, track time, and alarm upper limit can be modified, and these changes are effective once the Apply button is clicked.

The alarm status flag turns on if the temperature is above the temperature displayed in the Alarm Temperature field. The flag turns off when the temperature goes below the temperature displayed in this field. The exception is when the alarm temperature has never been changed from start-up, and, in this case, the flag is disabled.

The Reset Min/Max option resets the temperature to the minimum and maximum without the need of a power cycle.

XILINX

Appendix A

LVM and TDMS File Format

LabVIEW Measurement (`.lvm`) is a text based file format. TDM Streaming (`.tdms`) is a stream based file format. For testing the Zynq® UltraScale+™ RFSoC with this evaluation software, Xilinx recommends the LVM file format for small patterns. For large patterns, such as a standard 4G/5G pattern, the TDMS file is recommended.

LVM File Format

The LabVIEW Measurement (`.lvm`) file is a native, text based file format of the LabVIEW software. This file format is used in this evaluation tool GUI for data input and output. The `.lvm` file contains a file header and column based data. Some items in the file header are required. An example `.lvm` file with the headers required by this evaluation tool GUI is shown in the following figure.

Figure 56: **LVM File Format**

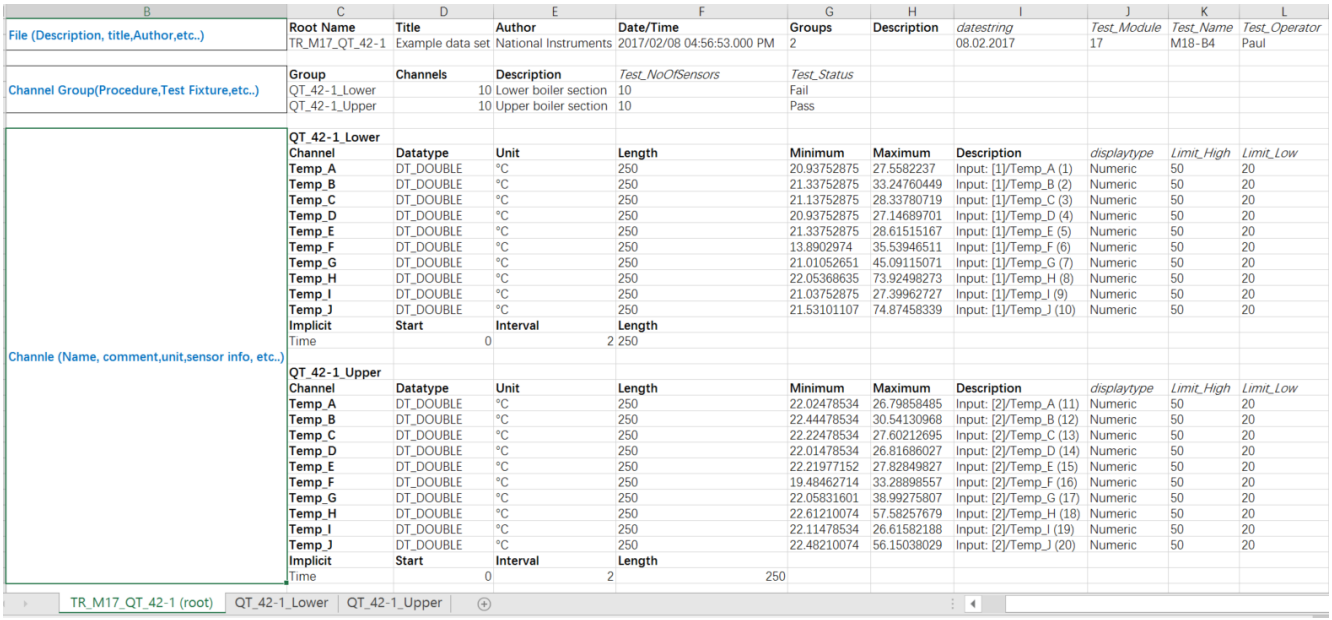
LabVIEW Measurement			
Writer_Version	2		
Reader_Version	2		
Separator	Tab		
Decimal_Separator	.		
Multi_Headings	No		
X_Columns	No		
Time_Pref	Relative		
Operator	xlnx		
Date	4/25/2018		
Time	36:46.7		
End_of_Header			
Start_Special			
Version	V1.0.0 Beta2		Help|about
Fs(MHz)	2000		
End_Special			
Channels	2		I/Q data channel
Samples	4	4	Rows of data below
Date	4/25/2018	4/25/2018	
Time	36:46.7	36:46.7	
X_Dimension	Time	Time	
X0	0	0	
Delta_X	5.00E-10	5.00E-10	
End_of_Header			
X_Value	I_vector	Q_vector	Comment
	9298	-6573	
	11280	-6	
	9133	6436	
	3720	10422	

For more information about the `.lvm` file format, see LabVIEW Measurement Files.

TDMS File Format

The TDMS file format targets the management and exchange of large and complex data sets. Unlike the text-based lvm format, the TDMS file is stream-based and thus, more difficult to generate and difficult to view in a simple text editor. National Instruments (NI) provides different tools such as a function library in MATLAB® and C/C++ that work with the TDMS file. NI also provides Excel add-ins for the TDMS file. The following figure shows a TDMS file open in Excel using the TDM Excel add-in.

Figure 57: **TDMS File Format**



File (Description, title,Author,etc..)	**Root Name**	**Title**	**Author**	**Date/Time**	**Groups**	**Description**	*datestring*	*Test_Module*	*Test_Name*	*Test_Operator*
	TR_M17_QT_42-1	Example data set	National Instruments	2017/02/08 04:56:53.000 PM	2		08.02.2017	17	M18-B4	Paul
Channel Group(Procedure,Test Fixture,etc..)	**Group**	**Channels**	**Description**	*Test_NoOfSensors*	*Test_Status*					
	QT_42-1_Lower	10	Lower boiler section	10	Fail					
	QT_42-1_Upper	10	Upper boiler section	10	Pass					
Channle (Name, comment,unit,sensor info, etc..)	**QT_42-1_Lower**									
	Channel	**Datatype**	**Unit**	**Length**	**Minimum**	**Maximum**	**Description**	*displaytype*	*Limit_High*	*Limit_Low*
	Temp_A	DT_DOUBLE	°C	250	20.93752875	27.5582237	Input: [1]/Temp_A (1)	Numeric	50	20
	Temp_B	DT_DOUBLE	°C	250	21.33752875	33.24760449	Input: [1]/Temp_B (2)	Numeric	50	20
	Temp_C	DT_DOUBLE	°C	250	21.13752875	28.33780719	Input: [1]/Temp_C (3)	Numeric	50	20
	Temp_D	DT_DOUBLE	°C	250	20.93752875	27.14689701	Input: [1]/Temp_D (4)	Numeric	50	20
	Temp_E	DT_DOUBLE	°C	250	21.33752875	28.61515167	Input: [1]/Temp_E (5)	Numeric	50	20
	Temp_F	DT_DOUBLE	°C	250	13.8902974	35.53946511	Input: [1]/Temp_F (6)	Numeric	50	20
	Temp_G	DT_DOUBLE	°C	250	21.01052651	45.09115071	Input: [1]/Temp_G (7)	Numeric	50	20
	Temp_H	DT_DOUBLE	°C	250	22.05368635	73.92498273	Input: [1]/Temp_H (8)	Numeric	50	20
	Temp_I	DT_DOUBLE	°C	250	21.03752875	27.39962727	Input: [1]/Temp_I (9)	Numeric	50	20
	Temp_J	DT_DOUBLE	°C	250	21.53101107	74.87458339	Input: [1]/Temp_J (10)	Numeric	50	20
	Implicit	**Start**	**Interval**	**Length**						
	Time	0	2	250						
	QT_42-1_Upper									
	Channel	**Datatype**	**Unit**	**Length**	**Minimum**	**Maximum**	**Description**	*displaytype*	*Limit_High*	*Limit_Low*
	Temp_A	DT_DOUBLE	°C	250	22.02478534	26.79858485	Input: [2]/Temp_A (11)	Numeric	50	20
	Temp_B	DT_DOUBLE	°C	250	22.44478534	30.54130968	Input: [2]/Temp_B (12)	Numeric	50	20
	Temp_C	DT_DOUBLE	°C	250	22.22478534	27.60212695	Input: [2]/Temp_C (13)	Numeric	50	20
	Temp_D	DT_DOUBLE	°C	250	22.01478534	26.81686027	Input: [2]/Temp_D (14)	Numeric	50	20
	Temp_E	DT_DOUBLE	°C	250	22.21977152	27.82849827	Input: [2]/Temp_E (15)	Numeric	50	20
	Temp_F	DT_DOUBLE	°C	250	19.48462714	33.28898557	Input: [2]/Temp_F (16)	Numeric	50	20
	Temp_G	DT_DOUBLE	°C	250	22.05831601	38.99275807	Input: [2]/Temp_G (17)	Numeric	50	20
	Temp_H	DT_DOUBLE	°C	250	22.61210074	57.58257679	Input: [2]/Temp_H (18)	Numeric	50	20
	Temp_I	DT_DOUBLE	°C	250	22.11478534	26.61582188	Input: [2]/Temp_I (19)	Numeric	50	20
	Temp_J	DT_DOUBLE	°C	250	22.48210074	56.15038029	Input: [2]/Temp_J (20)	Numeric	50	20
	Implicit	**Start**	**Interval**	**Length**						
	Time	0	2	250						

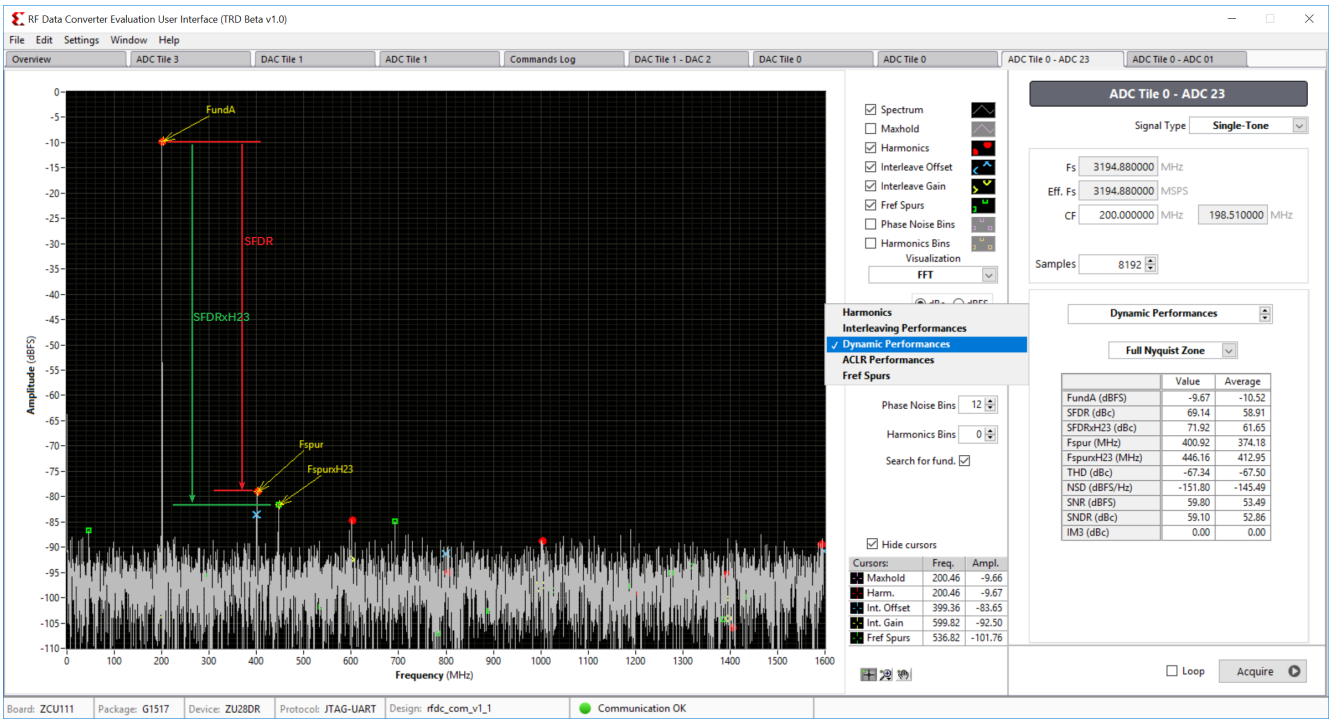
TR_M17_QT_42-1 (root) | QT_42-1_Lower | QT_42-1_Upper

For additional details, see The NI TDMS File Format.

FFT Metrics

There are many converter metrics on the RF-ADC FFT page. These metrics are listed and defined as follows.

Figure 58: **RF-ADC FFT Metrics**



- **dBFS:** dBFS is the full scale of the RF-ADC expressed in dB, normalized to 0. The corresponding dBm value of 0dBFS depends on the ADC's input full scale range, which is listed in the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926).
- **FundA:** RMS power level of fund signal expressed in dBFS.
- **SFDR:** Spurious-free dynamic range (SFDR) expressed in dBc. SFDR is the ratio of the RMS value of the signal to the RMS value of the peak spurious spectral component for the analog input that produces the worst result.
- **SFDRxH23:** SFDR excludes the second and third harmonic distortion in dBc. The location of harmonic distortions are predictable and hence can be handled separately in application. Therefore, a separate SFDRxH23 is listed for reference.

- **Fspur:** The frequency location of the worst spur in MHz in the first Nyquist band.
- **FspurxH23:** The frequency location of the worst spur excludes the second and third harmonic distortion in MHz in the first Nyquist band. This specification still includes ADC OIS, GTIS, and PLL reference spurs.
- **THD:** Total harmonic distortion (THD) in dBc. THD is the ratio of the RMS signal energy to the RMS value of the sum of the first six harmonics.
- **NSD:** Noise spectrum density (NSD) in dBFS/Hz. NSD is the RMS noise power per Hz normalized to full scale in the first Nyquist band. The noise power in this software indicates total other power except the power of the found signal.
- **SNR:** Signal to noise ratio (SNR) in dB. SNR is the ratio of the RMS signal amplitude to the RMS value of the sum of all the spectral components except the first six harmonics and dc. The unit in dBFS indicates the signal here and refers to full scale of RF-ADC.
- **SNDR:** Signal to noise and distortion ratio (SNDR) expressed in dBc. SNDR is the ratio of the RMS signal amplitude to the RMS value of the sum of all spectral components except fund signal. It is similar to SNR, but includes all the harmonics.
- **IM3:** Third-order inter-modulation (IM3) distortion products expressed in dBc. IM3 used in dual-tone testing, indicates the ratio of RMS signal amplitude to the maximum RMS amplitude of $2F_2 \pm F_1$ or $2F_1 \pm F_2$.
- **F_{ref} Spurs:** Spurs generated by the input reference (the frequency of phase-frequency-detector) of the PLL, including its harmonics. When using an external PLL for clocking the Zynq UltraScale+ RFSoC directly, you must indicate the reference frequency in the PLL tab for this evaluation tool GUI to calculate the F_{ref} spurs. The RF-ADC is built with interleaving technology. Spurs of offset interleaving and gain/timing interleaving are listed on the RF-ADC FFT tab by choosing Interleaving Performances.
- **Interleave Offset:** The frequency location and amplitude of offset interleaving spurs.
- **Interleave Gain:** The frequency location and amplitude of gain/timing interleaving spurs.

Appendix C

Appending Files

RF-DAC Data Pattern

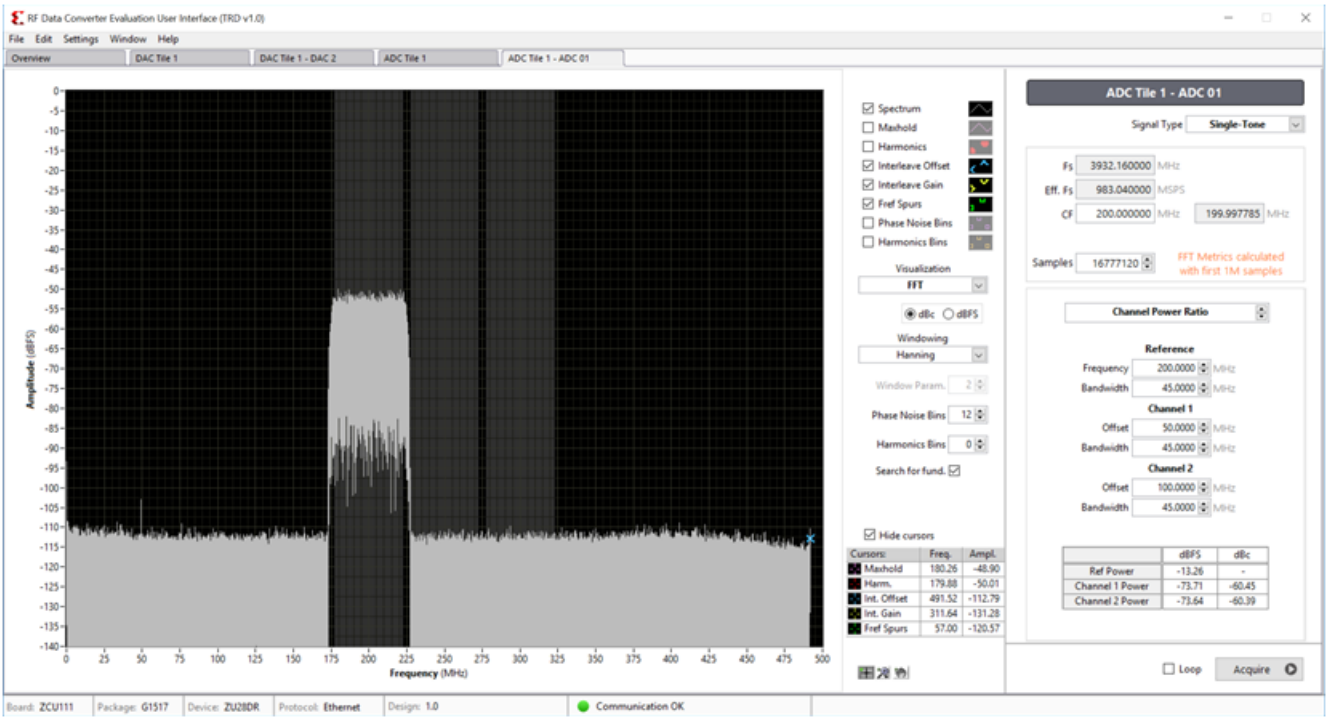
Data patterns with the TDMS or LVM file format are available for reference under `\Data\DAC\`. The content of these files are not intended to be compliant to any standard. The files are provided as example waveforms that can be used to create files for your application. The contents of these files can be easily identified from the file name. Here is an example of a file name, `IQ_1x_QAM256_RRC0p1_50M_BB491p52MHz_length_16M_-15dB.tdms`.

This file name means that the data pattern is in IQ (complex) format, there is one QAM256 modulated carrier, the RRC roll-off coefficient is 0.1, carrier bandwidth is 50 MHz, data sampling rate is 491.52 MHz, data length is around 16M samples, carrier amplitude is –15 dBFS, and the file format is TDMS. Configure RF-DAC in IQ mode at the digital side, set the RF-DAC sampling clock at 3932.16 MSPS, set the interpolation factor as 8 (491.52M * 8 = 3932.16 MHz), then load this file from the RF-DAC FFT page, and you will see the correct carrier.

***Note*:** For the ZCU111 board, the maximum number of samples that the block RAM can handle is 32K for IQ data and 64K for real data. For the ZCU208 and ZCU216 boards, the maximum number of samples that the block RAM can handle is 8K for IQ data and 16K for real data. Switch to the DDR mode (in Memory Type) for data sources if the number of samples is greater than this limitation.

The following figure illustrates the FFT plot of this carrier captured by RF-ADC with a loopback path using the ZCU111 board. In this example, the RF-DAC is set in 32 mA/3V mode and some digital gain has been used to increase the carrier amplitude seen by the RF-ADC.

Figure 59: **RF-DAC Test Pattern Example**



Note: If the DAC vector length is larger than 1M samples (e.g., being driven by DDR), the GUI tool rounds to this limit for display purposes only. This might lead to the impression that the signal is not coherent, due to rounding, but this is only a visual display artifact.

Configuration and Preferences

Configurations (`.cfg`) and preferences (`.prf`) are available under `\Config\`. Configurations and preferences are provided in pairs for easy evaluation. The major properties can be found from file name, for example, `RFDC_Example_BRAM_ADC_DAC_8X8_Loop_C2R_X8_3932P16M.cfg`. This configuration sets sampling frequencies of 3932.16 MHz for all eight RF-ADCs and RF-DACs with decimation and interpolation of 8× and the BRAM selected.

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Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *ZCU111 Evaluation Board User Guide* (UG1271)
2. *Zynq UltraScale+ RFSoC RF Data Converter Evaluation Tool (ZCU111) User Guide* (UG1287)
3. LabVIEW Run-Time Engine 2017 SP1
4. *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269)
5. *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
6. *ZCU111 System Controller – GUI Tutorial* (XTP517)
7. Texas Instruments Clocks and Synthesizers (TICS) Pro Software
8. LabVIEW Measurement Files
9. The NI TDMS File Format
10. *Zynq UltraScale+ RFSoC Product Tables and Product Selection Guide* (XMP105)
11. *ZCU216 Evaluation Board User Guide* (UG1390)
12. *ZCU208 Evaluation Board User Guide* (UG1410)
13. *Zynq UltraScale+ RFSoC ZCU208 and ZCU216 RF Data Converter Evaluation Tool User Guide* (UG1433)

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